HITACHI IC MEMORY DATA BOOK

HITACHI

ADE-403-001F

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Quick Reference Guide to Hitachi IC Memories

MOS RAM

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	16 k-bit	HM6116-2*2	CMOS	2048×8	120	120	24		●	●								119
		HM6116-3*2			150	150			●	●								119
		HM6116-4*2			200	200			●	●								119
		HM6116L-2*2			120	120			●	●								119
		HM6116L-3*2			150	150			●	●								119
		HM6116L-4*2			200	200			●	●								119
		HM6716-25	Bi-CMOS		25	25					●							120
		HM6716-30			30	30					●							120
		HM6268-25	CMOS	4096×4	25	25	20		●									125
		HM6268-35			35	35			●									125
		HM6268-45			45	45			●									125
		HM6268L-25			25	25			●									125
		HM6268L-35			35	35			●									125
		HM6268L-45			45	45			●									125
		HM6267-35		16384×1	35	35			●									130
		HM6267-45			45	45			●									130
		HM6267-55			55	55			●									130
		HM6267L-35			35	35			●									130
		HM6267L-45			45	45			●									130
		HM6267L-55			55	55			●									130
	18 k-bit	HM6719-25	Bi-CMOS	2048×9	25	25	24				●							120
		HM6719-30			30	30					●							120
	64 k-bit	HM6264A-10	CMOS	8192×8	100	100	28		●	●	●							135
		HM6264A-12			120	120			●	●	●							135
		HM6264A-15			150	150			●	●	●							135

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	64 k-bit	HM6264AL-10	CMOS	8192×8	100	100	28		●	●	●						135
		HM6264AL-12			120	120			●	●	●						135
		HM6264AL-15			150	150			●	●	●						135
		HM6264AL-10L			100	100			●	●	●						135
		HM6264AL-12L			120	120			●	●	●						135
		HM6264AL-15L			150	150			●	●	●						135
		HM6288-25		16384×4	25	25	22		●						●		142
		HM6288-35			35	35	24 (SOJ)		●						●		142
		HM6288L-25			25	25			●						●		142
		HM6288L-35			30	30			●						●		142
		HM6289-25			25	25									●		147
		HM6289-35			35	35									●		147
		HM6289L-25			25	25									●		147
		HM6289L-35			35	35									●		147
		HM6788-25	Bi-CMOS		25	25			●								156
		HM6788-30			30	30			●								156
		HM6788H-15			15	15			●								160
		HM6788H-20			20	20			●								160
		HM6789-25		16384×4 (with $\overline{OE}$)	25	25	24				●				●		164
		HM6789-30			30	30					●				●		164
		HM6789H-15			15	15			●						●		171
		HM6789H-20			20	20			●						●		171
		HM6287-45	CMOS	65536×1	45	45	22		●								178
		HM6287-55			55	55			●								178
		HM6287-70			70	70			●								178
		HM6287L-45			45	45			●								178
		HM6287L-55			55	55			●								178

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	64 k-bit	HM6287L-70	CMOS	65536×1	70	70	22		●								178
		HM6287H-25			25	25	22		●						●		183
		HM6287H-35			35	35	24 (SOJ)		●						●		183
		HM6287HL-25			25	25			●						●		183
		HM6287HL-35			35	35			●						●		183
		HM6787-25	Bi-CMOS		25	25	22		●				●				189
		HM6787-30			30	30			●				●				189
		HM6787H-15			15	15			●						●		194
		HM6787H-20			20	20			●						●		194
	256 k-bit	HM62256-8	CMOS	32768×8	85	85	28		●	●							199
		HM62256-10			100	100			●	●							199
		HM62256-12			120	120			●	●							199
		HM62256-15			150	150			●	●							199
		HM62256L-8			85	85			●	●							199
		HM62256L-10			100	100			●	●							199
		HM62256L-12			120	120			●	●							199
		HM62256L-15			150	150			●	●							199
		HM62256L-10SL			100	100			●	●							199
		HM62256L-12SL			120	120			●	●							199
		HM62256L-15SL			150	150			●	●							199
		HM62832-35			35	35			●						●		207
		HM62832-45			45	45			●						●		207
		HM62832L-35			35	35			●						●		207
		HM62832L-45			45	45			●						●		207
		HM62832H-25*3			25	25			●						●		216
		HM62832H-35*3			35	35			●						●		216
		HM62832HL-25*3			25	25			●						●		216

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	256 k-bit	HM62832HL-35*3	CMOS	32768×8	35	35	28		●						●		216
		HM62832UH-15*4			15	15			●					●			222
		HM62832UH-20*4			20	20			●					●			222
		HM62832UHL-15*4			15	15			●					●			222
		HM62832UHL-20*4			20	20			●					●			222
		HM6208-35		65536×4	35	35	24		●								223
		HM6208-45			45	45			●								223
		HM6208L-35			35	35			●								223
		HM6208L-45			45	45			●								223
		HM6208H-25			25	25			●						●		223
		HM6208H-35			35	35			●						●		223
		HM6208H-45			45	45			●						●		223
		HM6208HL-25			25	25			●						●		223
		HM6208HL-35			35	35			●						●		223
		HM6208HL-45			45	45			●						●		223
		HM6708-20*3	Bi-CMOS		20	20			●						●		229
		HM6708-25*3			25	25			●						●		229
		HM6207-35	CMOS	262144×1	35	35			●								243
		HM6207-45			45	45			●								243
		HM6207L-35			35	35			●								243
		HM6207L-45			45	45			●								243
		HM6207H-25			25	25			●						●		243
		HM6207H-35			35	35			●						●		243
		HM6207H-45			45	45			●						●		243
		HM6207HL-25			25	25			●						●		243
		HM6207HL-35			35	35			●						●		243

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	256 k-bit	HM6207HL-45	CMOS	262144×1	45	45	24		●						●		243
		HM6707-20*3	Bi-CMOS		20	20			●						●		249
		HM6707-25*3			25	25			●						●		249
		HM6709-20		65536×4	20	20	28							●			234
		HM6709-25			25	25								●			234
	1 M-bit	HM628128-7	CMOS	131072×8	70	70	32		●	●							254
		HM628128-8			85	85			●	●							254
		HM628128-10			100	100			●	●							254
		HM628128-12			120	120			●	●							254
		HM628128L-7			70	70			●	●							254
		HM628128L-8			85	85			●	●							254
		HM628128L-10			100	100			●	●							254
		HM628128L-12			120	120			●	●							254
		HM628128L-7SL			70	70			●	●							254
		HM628128L-8SL			85	85			●	●							254
		HM628128L-10SL			100	100			●	●							254
		HM628128L-12SL			120	120			●	●							254
		HM624256-35		262144×4	35	35	28		●						●		264
		HM624256-45			45	45			●						●		264
		HM624256L-35			35	35			●						●		264
		HM624256L-45			45	45			●						●		264
		HM624257-35			35	35	32								●		272
		HM624257-45			45	45									●		272
		HM624257L-35			35	35									●		272
		HM624257L-45			45	45									●		272
Static RAM Module	1 M-bit	HM66203-10		131072×8	100	100										●	281
		HM66203-12			120	120										●	281

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static RAM Module	1 M-bit	HM66203-15	CMOS	131072×8	150	150	32									●	281
		HM66203L-10			100	100										●	281
		HM66203L-12			120	120										●	281
		HM66203L-15			150	150										●	281
		HM66204-12		131072×8 (with decoder)	120	120										●	287
		HM66204-15			150	150										●	287
		HM66204L-12			120	120										●	287
		HM66204L-15			150	150										●	287
Pseudo static	256 k-bit	HM65256B-10		32768×8	100	160	28		●	●	●						295
		HM65256B-12			120	190			●	●	●						295
		HM65256B-15			150	235			●	●	●						295
		HM65256B-20			200	310			●	●	●						295
		HM65256BL-10			100	160			●	●	●						295
		HM65256BL-12			120	190			●	●	●						295
		HM65256BL-15			150	235			●	●	●						295
		HM65256BL-20			200	310			●	●	●						295
	1 M-bit	HM658128D-10		131072×8	100	180	32		●	●							302
		HM658128D-12			120	210			●	●							302
		HM658128D-15			150	250			●	●							302
		HM658128L-10			100	180			●	●							302
		HM658128L-12			120	210			●	●							302
		HM658128L-15			150	250			●	●							302
		HM658128AD-8			80	160			●	●							311
		HM658128AD-10			100	180			●	●							311
		HM658128AD-12			120	210			●	●							311
		HM658128AL-8			80	160			●	●							311
		HM658128AL-10			100	180			●	●							311

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Pin No.	Package*1 G	P	FP	SP	ZP	CG	CP	JP	M	Page
Pseudo static	1 M-bit	HM658128AL-12	CMOS	131072×8	120	210	32		●	●							311
		HM658128AL-8L			80	80			●	●							311
		HM658128AL-10L			100	100			●	●							311
		HM658128AL-12L			120	120			●	●							311
	4 M-bit	HM658512D-8*3		524288×8	80	160			●	●							315
		HM658512D-10*3			100	180			●	●							315
		HM658512D-12*3			120	210			●	●							315
		HM658512L-8*3			80	160			●	●							315
		HM658512L-10*3			100	180			●	●							315
		HM658512L-12*3			120	210			●	●							315
		HM658512L-8L*3			80	160			●	●							315
		HM658512L-10L*3			100	180			●	●							315
		HM658512L-12L*3			120	210			●	●							315
Application specific memory	16 k-bit	HM63021-28		2048×8 Line memory	20	28	28				●						327
		HM63021-34			25	34					●						327
		HM63021-45			30	45					●						327
	1 M-bit	HM53051-34		262144×4 Frame memory	30	34	18 28 (SOJ)		●	●							341
		HM53051-45			35	45			●	●							341
		HM53051-60			40	60			●	●							341
	256 k-bit	HM53461-10		65536×4 Multi port	100	190	24		●			●			●		352
		HM53461-12			120	220			●			●			●		352
		HM53461-15			150	260			●			●			●		352
		HM53462-10			100	190			●			●			●		365
		HM53462-12			120	220			●			●			●		365
		HM53462-15			150	260			●			●			●		365
	1 M-bit	HM534251-10		262144×4 Multi port	100	190	28					●			●		385
		HM534251-11			100	190						●			●		385

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	PGA	Page
Application specific memory	1 M-bit	HM534251-12	CMOS	262144×4 Multi port	120	220	28					●			●			385
		HM534251-15			150	260						●			●			385
		HM534252-10			100	190						●			●			405
		HM534252-11			100	190						●			●			405
		HM534252-12			120	220						●			●			405
		HM534252-15			150	260						●			●			405
FIFO	18 k-bit	HM63921-20*3		2 k×9	20	20			●						●			431
		HM63921-25*3			25	25			●						●			431
		HM63921-35*3			30	30			●						●			431
	36 k-bit	HM63941-25*4		4 k×9	25	25			●						●			440
		HM63941-35*4			35	35			●						●			448
		HM63941-45*4			45	45			●						●			448
TAGM	*	HM644332-25		512×98	25	50	64										●	451
		HM644332-30			30	50											●	451
Data RAM	128 k-bit	HM62A168-25		8192×16 4096×16 ×2-way	25	25	52							●				470
		HM62A168-35			35	35								●				470
		HM62A168-45			45	45								●				470
	144 k-bit	HM62A188-25		8192×18 4096×18 ×2-way	25	25								●				470
		HM62A188-35			35	35								●				470
		HM62A188-45			45	45								●				470
Dynamic	256 k-bit	HM50464-12	NMOS	65536×4	120	220	18		●					●				485
		HM50464-15			150	260			●					●				485
		HM50464-20			200	330			●					●				485
		HM50256-12		262144×1	120	220	16		●			●		●				493
		HM50256-15			150	260	18 (PLCC)		●			●		●				493
		HM50256-20			200	330			●			●		●				493

*: 512-entry × 4-way/1024-entry × 2-way

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Dynamic	256 k-bit	HM51256-8	CMOS	262144×1	85	155	16		●			●		●				501
		HM51256-10			100	180	18 (PLCC)		●			●		●				501
		HM51256-12			120	210			●			●		●				501
		HM51256-15			150	250			●			●		●				501
		HM51256L-8			85	155			●			●		●				501
		HM51256L-10			100	180			●			●		●				501
		HM51256L-12			120	210			●			●		●				501
		HM51256L-15			150	250			●			●		●				501
		HM51258-8			85	155	16		●									509
		HM51258-10			100	180			●									509
		HM51258-12			120	210			●									509
		HM51258-15			150	250			●									509
	1 M-bit	HM514256A-6		262144×4	60	120	20		●			●			●			518
		HM514256A-7			70	130			●			●			●			518
		HM514256A-8			80	160			●			●			●			518
		HM514256A-10			100	190			●			●			●			518
		HM514256A-12			120	220			●			●			●			518
		HM514256AL-6			60	120			●			●			●			518
		HM514256AL-7			70	130			●			●			●			518
		HM514256AL-8			80	160			●			●			●			518
		HM514256AL-10			100	190			●			●			●			518
		HM514256AL-12			120	220			●			●			●			518
		HM514256H-6			60	120			●			●			●			534
		HM514256H-7			70	130			●			●			●			534
		HM514258A-6			60	120			●			●			●			536
		HM514258A-7			70	130			●			●			●			536
		HM514258A-8			80	160			●			●			●			536

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Dynamic	1M-bit	HM514258A-10	CMOS	262144 ×4	100	190	20		●			●			●		536
		HM514258A-12			120	220			●			●			●		536
		HM514266A-6*3			60	120			●			●			●		550
		HM514266A-7*3			70	130			●			●			●		550
		HM514266A-8*3			80	160			●			●			●		550
		HM514266A-10*3			100	190			●			●			●		550
		HM514266A-12*3			120	220			●			●			●		550
		HM511000A-6		1048576 ×1	60	120	20		●			●			●		569
		HM511000A-7			70	130	18 (DIP)		●			●			●		569
		HM511000A-8			80	160			●			●			●		569
		HM511000A-10			100	190			●			●			●		569
		HM511000A-12			120	220			●			●			●		569
		HM511000AL-6			60	120			●			●			●		569
		HM511000AL-7			70	130			●			●			●		569
		HM511000AL-8			80	160			●			●			●		569
		HM511000AL-10			100	190			●			●			●		569
		HM511000AL-12			120	220			●			●			●		569
		HM511000H-6			60	120			●			●			●		581
		HM511000H-7			70	130			●			●			●		581
		HM511001A-6			60	120			●			●			●		583
		HM511001A-7			70	130			●			●			●		583
		HM511001A-8			80	160			●			●			●		583
		HM511001A-10			100	190			●			●			●		583
		HM511001A-12			120	220			●			●			●		583
		HM511002A-6			60	120			●			●			●		594
		HM511002A-7			70	130			●			●			●		594
		HM511002A-8			80	160			●			●			●		594

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Dynamic	1 M-bit	HM511002A-10	CMOS	1048576 ×1	100	190	20 18 (DIP)		●			●			●		594
		HM511002A-12			120	220			●			●			●		594
		HM571000-35R	Bi-CMOS		35	75	28								●		777
		HM571000-40			40	85									●		777
		HM571000-45			45	90									●		777
		HM574256-35R*3		262144 ×4	35	75									●		759
		HM574256-40*3			40	85									●		759
		HM574256-45*3			45	90									●		759
	4 M-bit	HM514100-8	CMOS	4194304 ×1	80	150	20					●			●		683
		HM514100-10			100	180						●			●		683
		HM514100-12			120	210						●			●		683
		HM514101-8			80	150						●			●		708
		HM514101-10			100	180						●			●		708
		HM514101-12			120	210						●			●		708
		HM514102-8			80	150						●			●		733
		HM514102-10			100	180						●			●		733
		HM514102-12			120	210						●			●		733
		HM514400-8		1048576 ×4	80	150						●			●		607
		HM514400-10			100	180						●			●		607
		HM514400-12			120	210						●			●		607
		HM514402-8			80	150						●			●		632
		HM514402-10			100	180						●			●		632
		HM514402-12			120	210						●			●		632
		HM514410-8*3			80	150						●			●		658
		HM514410-10*3			100	180						●			●		658
		HM514410-12*3			120	210						●			●		658

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Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Dynamic RAM module	256 k-bit ×9	HB561409-85	CMOS	262144 ×9	85	155	30									●	799
		HB561409-10			100	180										●	799
		HB56D25609-85A			85	160										●	803
		HB56D25609-10A			100	190										●	803
		HB56D25609-12A			120	220										●	803
	256 k-bit ×8	HB56D25608-6A		262144 ×8	60	125										●	818
		HB56D25608-7A			70	140										●	818
		HB56D25608-8A			80	160										●	818
		HB56D25608-10A			100	190										●	818
		HB56D25608-12A			120	220										●	818
	256 k-bit ×36	HB56D25636B-85		262144 ×36	85	160										●	828
		HB56D25636B-10			100	190										●	828
		HB56D25636B-12			120	220										●	828
	512 k-bit ×36	HB56D51236B-85		524288 ×36	85	160										●	838
		HB56D51236B-10			100	190										●	838
		HB56D51236B-12			120	220										●	838
	1 M-bit ×9	HB56A19-6A		1048576 ×9	60	120										●	848
		HB56A19-7A			70	130										●	848
		HB56A19-8A			80	160										●	848
		HB56A19-10A			100	190										●	848
		HB56A19-12A			120	220										●	848
	1 M-bit ×8	HB56A18-6A		1048576 ×8	60	120										●	855
		HB56A18-7A			70	130										●	855
		HB56A18-8A			80	160										●	855
		HB56A18-10A			100	190										●	855
		HB56A18-12A			120	220										●	855

(cont)

Mode	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns) max	Cycle time (ns) min	Package*1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Dynamic RAM module	2 M-bit ×4	HB56A24B-6A	CMOS	2097152 ×4	60	120	30									●	862
		HB56A24B-7A			70	130										●	862
		HB56A24B-8A			80	160										●	862
		HB56A24B-10A			100	190										●	862
		HB56A24B-12A			120	220										●	862
	1 M-bit ×9	HB56C19-8A		1048576 ×9	80	160										●	862
		HB56C19-10A			100	190										●	869
		HB56C19-12A			120	220										●	869
	1 M-bit ×8	HB56C18-8A		1048576 ×8	80	160										●	876
		HB56C18-10A			100	190										●	876
		HB56C18-12A			120	220										●	876
	1 M-bit ×36	HB56D136-8		1048576 ×36	80	160										●	883
		HB56D136-10			100	190										●	883
	2 M-bit ×36	HB56D236B-8		2097152 ×32	80	160										●	893
		HB56D236B-10			100	190										●	893
	4 M-bit ×9	HB56A49-8		4194304 ×9	80	150										●	899
		HB56A49-10			100	180										●	899
	4 M-bit ×8	HB56A48-8		4194304 ×8	80	150										●	906
		HB56A48-10			100	180										●	906

Notes: 1. The package codes of G to M are applied to the package materials as follows.
G: cerdip, P: plastic DIP, FP: plastic flat package (SOP), SP: skinny type plastic DIP, ZP: plastic ZIP, CG: ceramic leadless chip carrier, CP: plastic leaded chip carrier, JP: plastic small outline J-bend package, M: module, PGA: pin grid array
2. Maintenance only. This device is not available for new application.
3. Preliminary
4. Under development.

Quick Reference Guide to Hitachi IC Memories

MOS ROM

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns)max	Package*1 Pin No.	G	P	FP	TS	CC	CP	JP	Page
Mask	256 k-bit	HN623257	CMOS	32768×8	150	28		●	●					915
		HN623258			200			●	●					921
		HN623257Z			120			●	●					918
	1 M-bit	HN62331		131072×8	120			●	●					924
		HN62321			150			●	●					924
		HN62321B			200			●	●					924
		HN62331E			120			●	●					927
		HN62321E			200			●	●					927
		HN62331A			120	32		●	●					930
		HN62321A			150			●	●					930
	2 M-bit	HN62422		131072×16 or 262144×8	150	40/44		●	●					933
		HN62412			200			●	●					933
	4 M-bit	HN62424		262144×16 or 524288×8	150	40/44		●	●					937
		HN62404			200			●	●					937
		HN62324B		524288×8	150	32		●	●					941
		HN62304B			200			●	●					941
		HN62414-17*4		262144×16 or 524288×8	170	40		●	●					956
		HN62414-20*4			200	44		●	●					956
		HN62444*4			100	48		●	●					963
		HN62444B*4		262144×16	100	40		●						970
		HN62314B-17*4		524288×8	170	32		●	●					974
		HN62314B-20*4			200			●	●					974
		HN62344B*4			100			●	●					978
	8 M-bit	HN62408		524288×16 or 1048576×8	200	42/48		●	●					944
		HN62308B		1048576×8	200	32		●	●					952
	16 M-bit	HN624016		1048576×16 or 2097152×8	200	42/48		●						948

(cont)

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns)max	Package*1 Pin No.	G	P	FP	TS	CC	CP	JP	Page
Electrically erasable and programmable	64 k-bit	HN58C65-25	CMOS	8192×8	250	28		●	●					985
		HN58C66-25			250			●	●					995
	256 k-bit	HN58C256-20		32768×8	200	28		●	●					1005
		HN58C257-20*3			200	32				●				1019
	1 M-bit	HN29C101-12*3		131072×8	120			●		●				1034
		HN29C101-15*3			150			●		●				1034
		HN29C101-20*3			200			●		●				1034
UV erasable and electrically programmable	256 k-bit	HN27C256A-10		32768×8	100	28	●							1046
		HN27C256A-12			120		●							1046
		HN27C256A-15			150		●							1046
		HN27C256H-70			70		●							1054
		HN27C256H-85			85		●							1054
	512 k-bit	HN27512-25	NMOS	65536×8	250		●							1064
		HN27512-30			300		●							1064
		HN27C512-17			170		●							1071
		HN27C512-20			200		●							1071
	1 M-bit	HN27C1024H-85	CMOS	65536×16	85	40 44 (JLCC)	●				●			1080
		HN27C1024H-10			100		●				●			1080
		HN27C1024H-12			120		●				●			1080
		HN27C1024H-15			150		●				●			1080
		HN27C101-17		131072×8	170	32	●							1096
		HN27C101-20			200		●							1096
		HN27C101-25			250		●							1096
		HN27C101A-10			100		●							1104
		HN27C101A-12			120		●							1104
		HN27C101A-15			150		●							1104
		HN27C101A-17			170		●							1104

Quick Reference Guide to Hitachi IC Memories

(cont)

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns)max	Package*1 Pin No.	G	P	FP	TS	CC	CP	JP	Page
UV erasable and electrically programmable	1 M-bit	HN27C101A-20	CMOS	131072×8	200	32	●							1104
		HN27C101A-25			250		●							1104
		HN27C301-17			170		●							1118
		HN27C301-20			200		●							1118
		HN27C301-25			250		●							1118
		HN27C301A-10			100		●							1119
		HN27C301A-12			120		●							1119
		HN27C301A-15			150		●							1119
		HN27C301A-17			170		●							1119
		HN27C301A-20			200		●							1119
		HN27C301A-25			250		●							1119
	4 M-bit	HN27C4096-10*3		262144×16	100	40 44 (JLCC)	●				●			1122
		HN27C4096-12*3			120		●				●			1122
		HN27C4096-15*3			150		●				●			1122
		HN27C4001-10*4		524288×8	100	32	●							1140
		HN27C4001-12			120		●							1140
		HN27C4001-15			150		●							1140
One time electrically programmable	256 k-bit	HN27C256A-12*3		32768×8	120	28		●						1143
		HN27C256A-15*3			150			●						1143
	512 k-bit	HN27512-25	NMOS	65536×8	250			●						1151
		HN27512-30			300			●						1151
	1 M-bit	HN27C101-20	CMOS	131072×8	200	32		●	●					1158
		HN27C101-25			250			●	●					1158
		HN27C101A-12			120			●	●					1165
		HN27C101A-15			150			●	●					1165
		HN27C101A-20			200			●	●					1165
		HN27C101A-25			250			●	●					1165

(cont)

Program	Total bit	Type No.	Process	Organization (word×bit)	Access time (ns)max	Package*1 Pin No.	G	P	FP	TS	CC	CP	JP	Page
One time electrically programmable	1 M-bit	HN27C301-20	CMOS	131072×8	200	32		●	●					1179
		HN27C301-25			250			●	●					1179
		HN29C301A-12			120			●	●					1181
		HN27C301A-15			150			●	●					1181
		HN27C301A-20			200			●	●					1181
		HN27C301A-25			250			●	●					1181

Notes: 1. The package codes of G, P and FP are applied to the package material as follows.
G: cerdip, P: plastic DIP, FP: plastic flat package (QFP and SOP), TS: Thin Small Outline package, CC: ceramic leaded chip carrier, CP: plastic leaded chip carrier, JP: plastic small outline J-bend package
2. Maintenance only. This device is not available for new application.
3. Preliminary
4. Under development.

Quick Reference Guide to Hitachi IC Memories

ECL RAM

Level	Total bit	Type No.	Organization (word×bit)	Output	Access time (ns) max	Supply voltage (V)	Power dissipation (W)	Package*1 Pin No.	G	F	CG	JP	Page
ECL 10 k	64 k-bit	HM10490-10*3	65536×1	Open emitter	15	–5.2	0.42	22	●				1187
		HM10490-12			12				●				1187
		HM10494-10	16384×4		10		0.8	28	●	●			1204
		HM10494-12			12				●	●			1204
	256 k-bit	HM10504-10*3	65536×4		10		0.5	28		●			1193
		HM10504-12*3			12					●			1193
		HM10500-15*3	262144×1		15		0.52	24	●				1190
ECL 100 k	64 k-bit	HM100490-10*3	65536×1		10	–4.5	0.5	22	●				1195
		HM100490-12*3			12				●				1195
		HM101490-10			10		0.57		●				1199
		HM101490-12			12				●				1199
		HM100494-10	16384×4		10		0.65	24/38	●	●			1208
		HM100494-12			12				●	●			1208
		HM101494-10			10		0.73	28	●	●			1211
		HM101494-12			12				●	●			1211
	256 k-bit	HM100504-10	65536×4		10		0.5	28/32	●	●			1225
		HM100504-12			12				●	●			1225
		HM100500-18	262144×1		18			24/28	●	●	●		1216
		HM101500-15			15			24		●	●		1221
		HM100506LL-11			11		0.7	32				●	1227

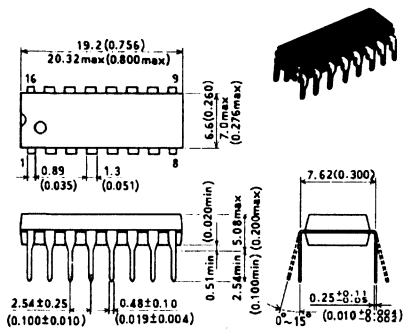
Notes: 1. The package codes of G, F and CG are applied to the package material as follows.
G: cerdip, f: flat package, CG: ceramic leadless chip carrier, JP: plastic small outline J-bend packge
2. Maintenance only. This device is not available for new application.
3. Preliminary
4. Under development.

Package Information

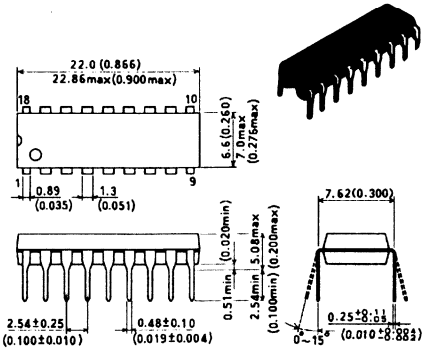
Dual-in-line Plastic

Unit: mm (inch)

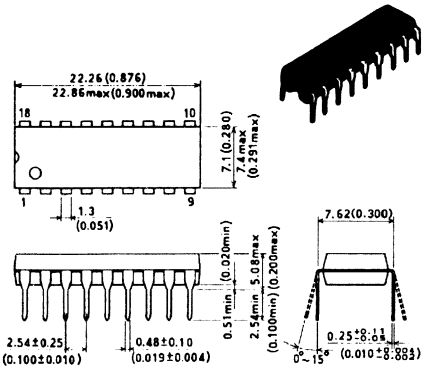
•DP-16B



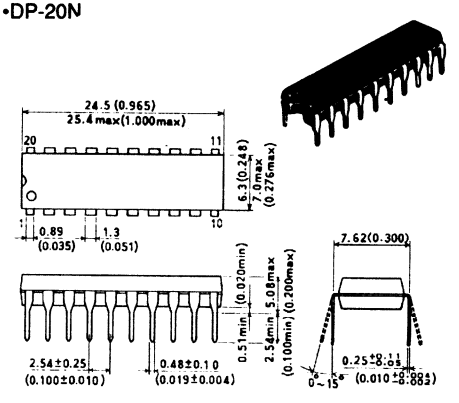
•DP-18B



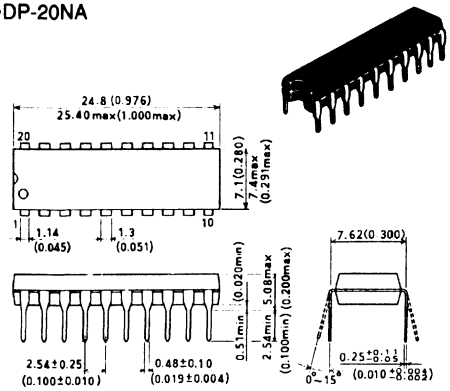
•DP-18C



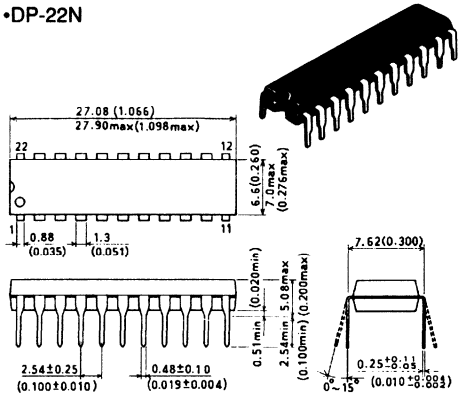
•DP-20N



•DP-20NA



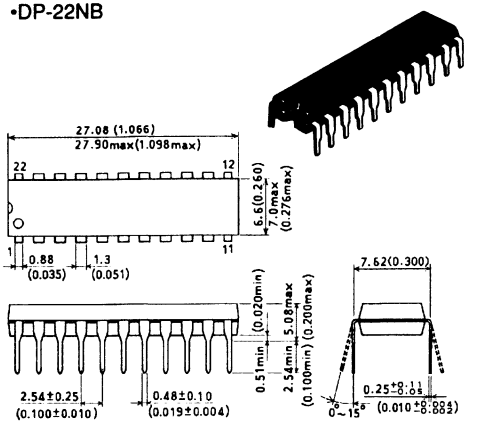
•DP-22N



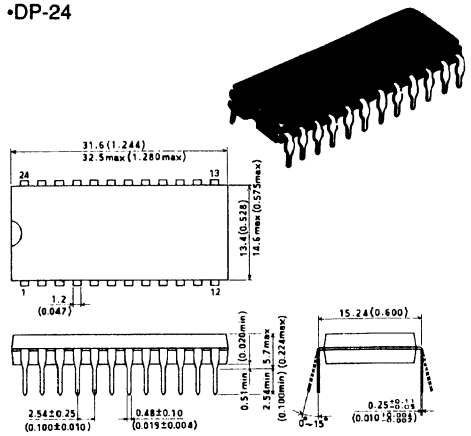
Package Information

Unit: mm (inch)

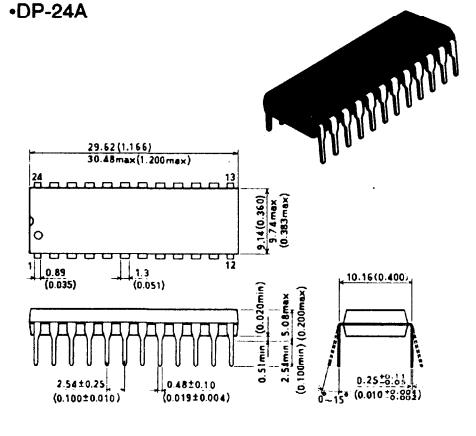
•DP-22NB



•DP-24



•DP-24A



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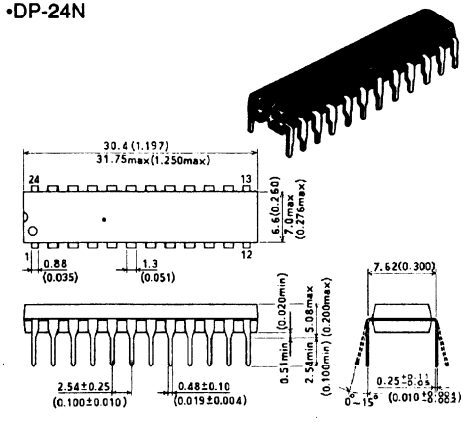
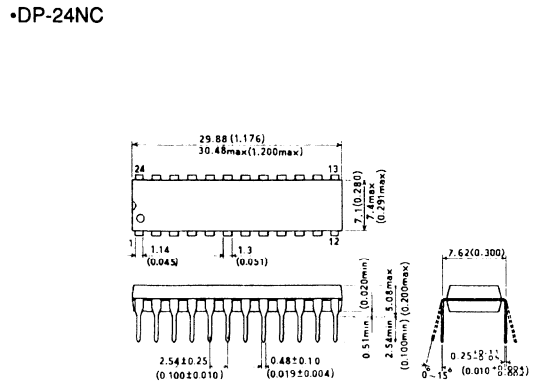
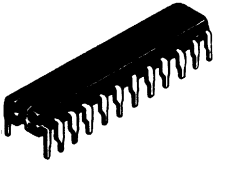


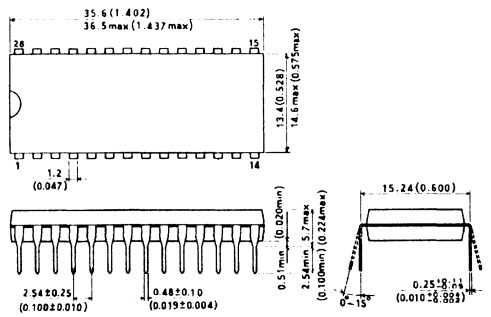
•DP-24NC

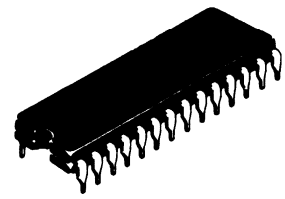




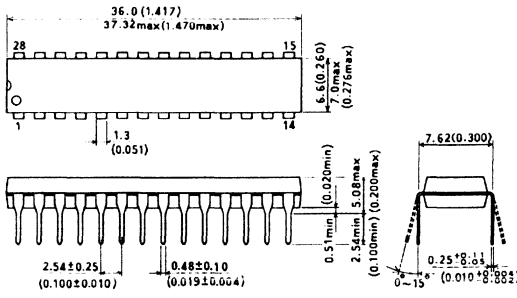
Unit: mm (inch)

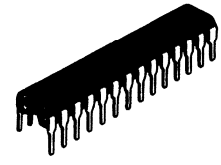
•DP-28



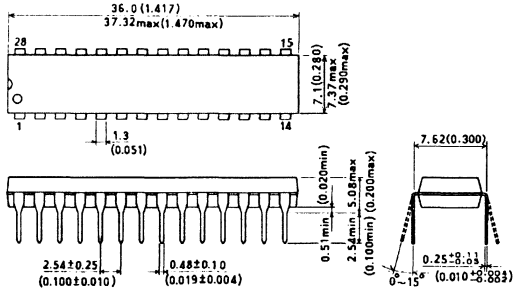


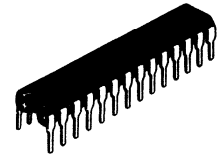
•DP-28N





•DP-28NA





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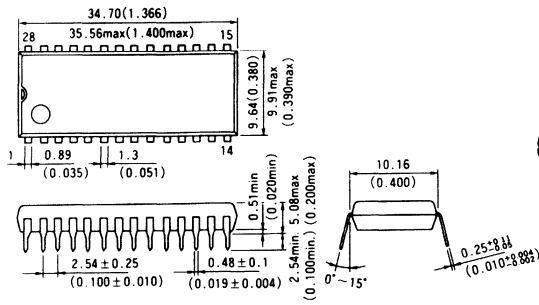
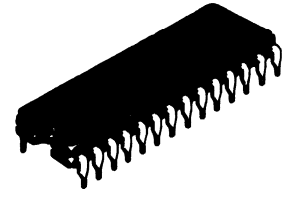
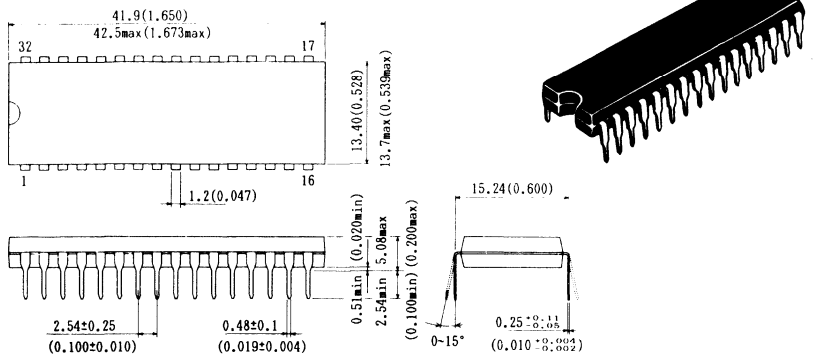




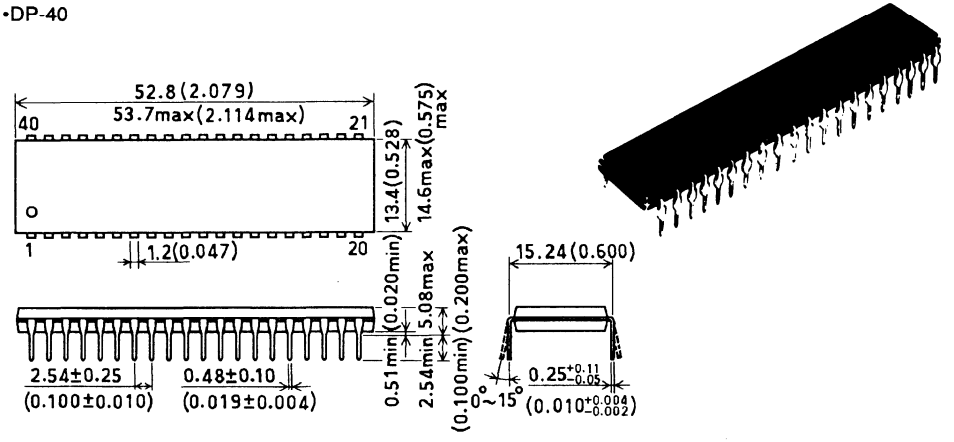
Package Information

Unit: mm (inch)

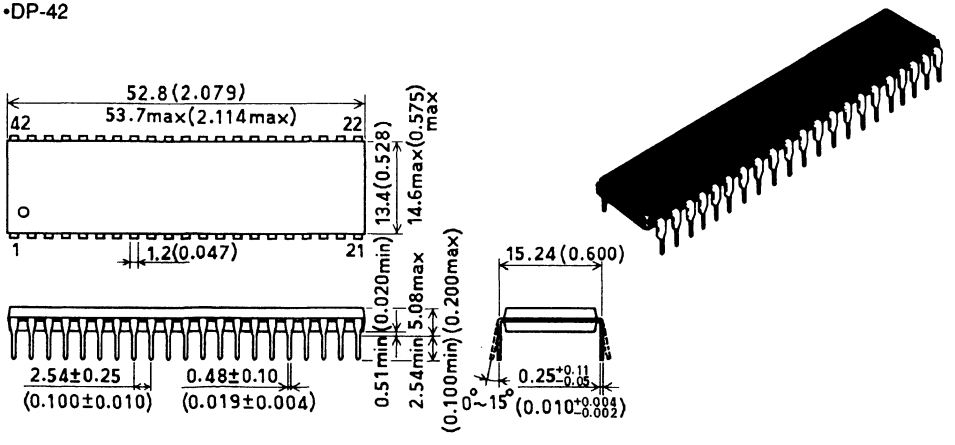
•DP-32



•DP-40



•DP-42



Applicable ICs

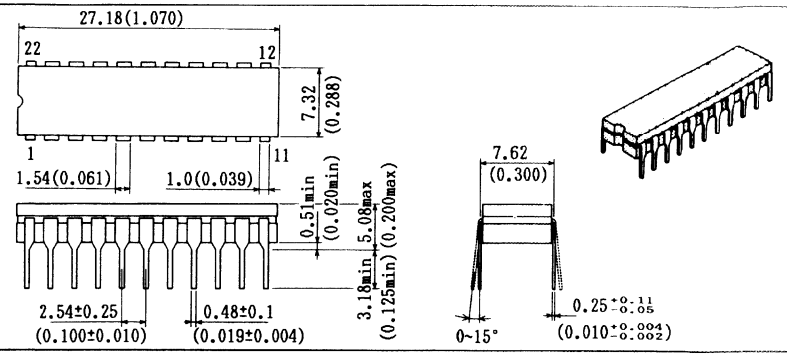
DP-16B	HM50256P Series, HM51256P Series, HM51256LP Series, HM51258P Series
DP-18B	HM50464P Series
DP-18C	HM53051P Series, HM511000AP Series, HM511000ALP Series, HM511000HP Series, HM511001AP Series, HM511002AP Series
DP-20N	HM6268P Series, HM6268LP Series, HM6267P Series, HM6267LP Series
DP-20NA	HM514256AP Series, HM514256ALP Series, HM514256HP Series, HM514258AP Series, HM514266A Series
DP-22N	HM6287P Series, HM6287LP Series
DP-22NB	HM6288P Series, HM6288LP Series, HM6788P Series, HM6788HP Series, HM6287HP Series, HM6287HLP Series, HM6787P Series, HM6787HP Series
DP-24	HM6116P Series, HM6116LP Series
DP-24A	HM53461P Series, HM53462P Series
DP-24NC	HM6716P Series, HM6719P Series, HM6789P Series, HM6208P Series, HM6208LP Series, HM6208HP Series, HM6208HLP Series, HM6708P Series, HM6207P Series, HM6207LP Series, HM6207HP Series, HM6207HLP Series, HM6707P Series, HM6789HP Series
DP-28	HM6264AP Series, HM6264ALP Series, HM6264ALP-L Series, HM62256P Series, HM62256LP Series, HM62256LP-SL Series, HM65256BP Series, HM65256BLP Series, HN623257P, HN623258P, HN62321P, HN62321BP, HN62331P, HN62321EP, HN62331EP, HN62321AP, HN62331AP, HN58C65P, HN58C66P, HN58C256P, HN27512P
DP-28N	HM6264ASP Series, HM6264ALSP Series, HM6264ALSP-L Series, HM65256BSP Series, HM65256BLSP Series, HM63021P Series
DP-28NA	HM62832P Series, HM62832LP Series, HM62832HP Series, HM62832HLP Series, HM63921 Series, HM63941 Series
DP-28C	HM624256P Series, HM624256LP Series
DP-32	HM628128P Series, HM628128LP Series, HM628128LP-SL Series, HM658128DP Series, HM658128LP Series, HN62304BP, HN62324BP, HN62321AP, HN62331AP, HN27C101P Series, HN27C101AP Series, HN27C301P Series, HN27C301AP Series, HM658512DP Series, HM658512LP Series, HM658512LP-L Series, HM658128ADP Series, HM658128ALP Series, HM658128ALP-L Series, HN62308BP, HN29C101P Series
DP-40	HN62412P, HN62422P, HN62404P, HN62424P
DP-42	HN62408P, HN624016P

Package Information

CERDIP

Unit: mm (inch)

•DG-22N



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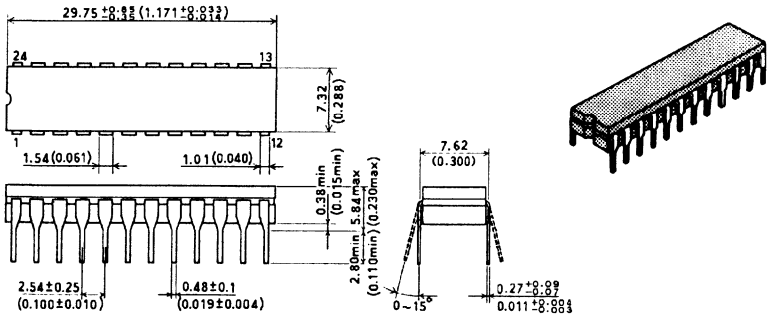
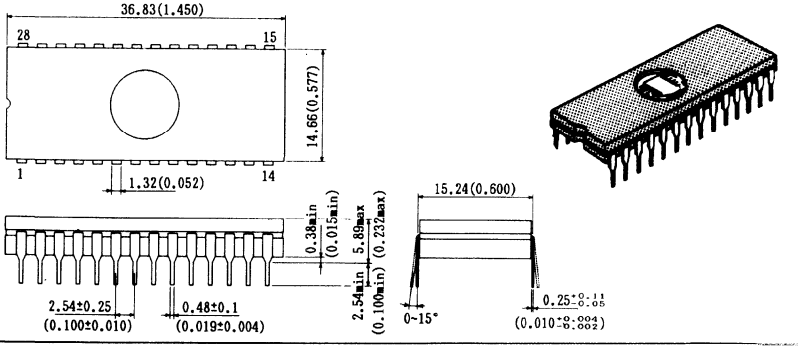


•DG-28



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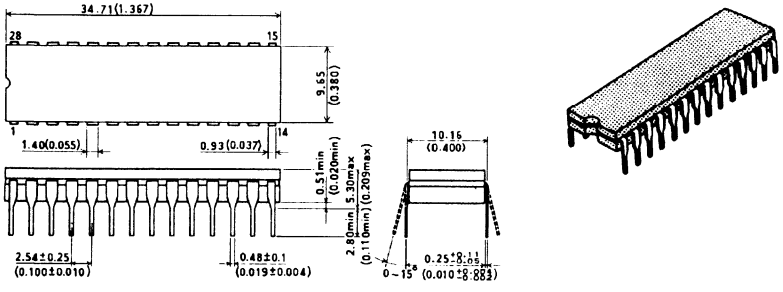
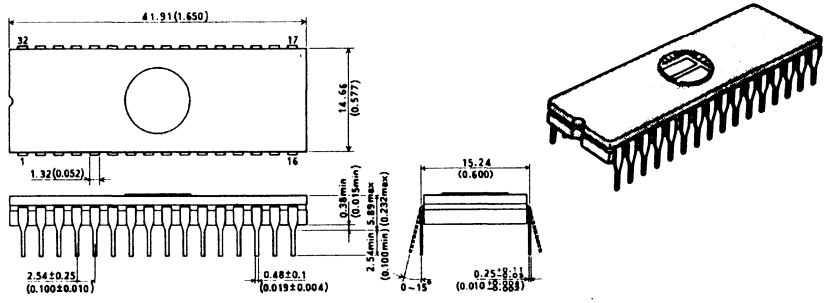
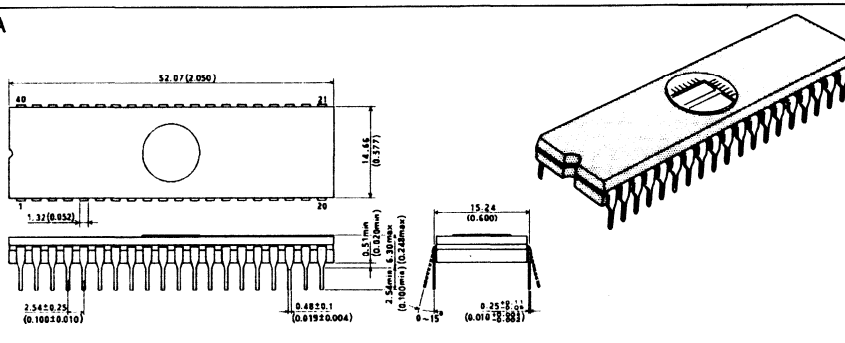


Unit: mm (inch)

•DG-32



•DG-40A



Applicable ICs

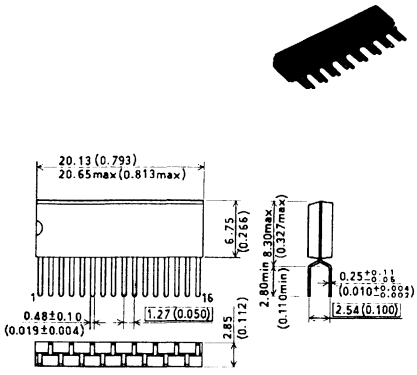
DG-22N	HM10490 Series, HM100490 Series, HM101490 Series
DG-24V	HM10500-15, HM100500-18
DG-28	HN27C256AG Series, HN27C256HG Series, HN27512G Series, HM10494G Series
DG-28N	HM100494G Series, HM101494G Series
DG-32	HN27C101G Series, HN27C301G Series, HN27C4001G Series, HN27C101AG Series, HN27C301AG Series
DG-40A	HN27C1024H Series, HN27C4096G Series

Package Information

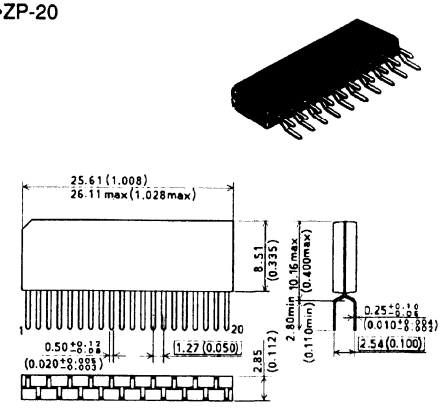
Zigzag-in-line Plastic

Unit: mm (inch)

•ZP-16



•ZP-20



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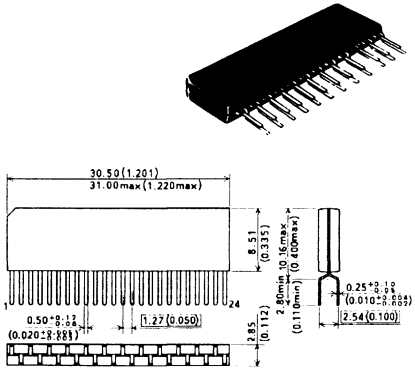
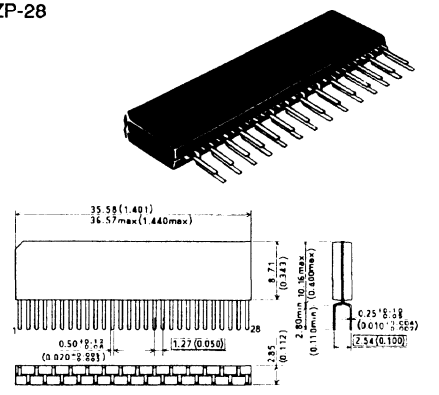


•ZP-28



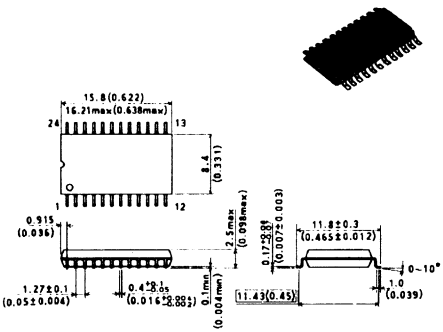
Applicable ICs

ZP-16	HM50256ZP Series, HM51256ZP Series, HM51256LZP Series
ZP-20	HM514256AZP Series, HM514256ALZP Series, HM514256HZP Series, HM514258AZP Series, HM514266A Series, HM511000AZP Seires, HM511000ALZP Series, HM511000HZP Series, HM511001AZP Series, HM511002AZP Series, HM514100ZP Series, HM514101ZP Series, HM514102ZP Series, HM514400ZP Series. HM514402ZP Series HM514410ZP Series
ZP-24	HM53461ZP Series, HM53462ZP Series
ZP-28	HM534251ZP Series, HM534252ZP Series

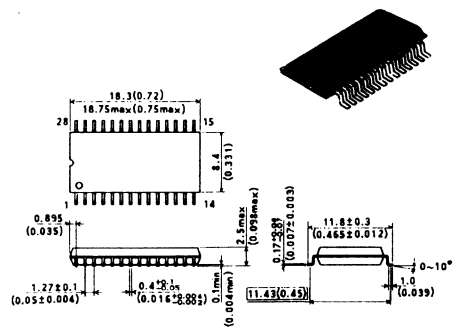
Flat Package

Unit: mm (inch)

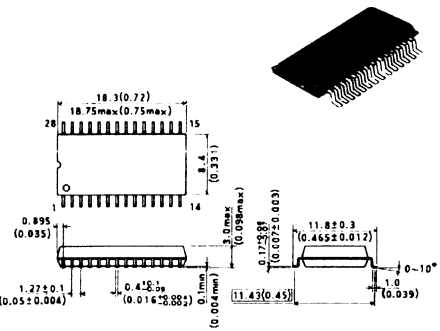
•FP-24D



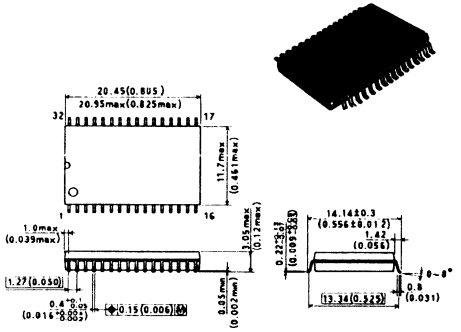
•FP-28D



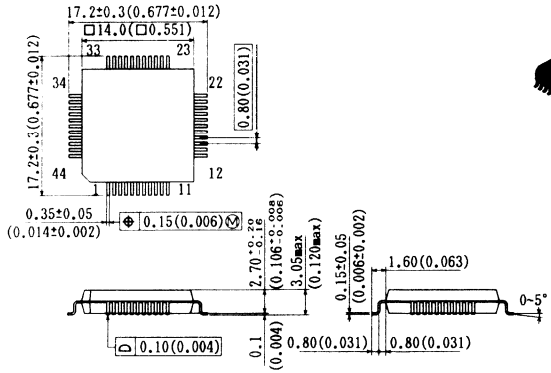
•FP-28DA



•FP-32D



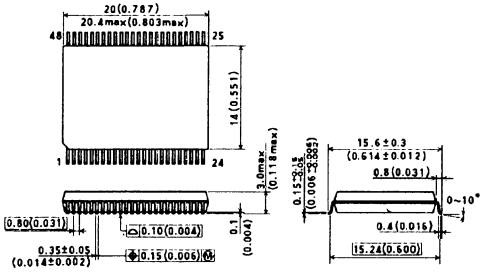
•FP-44A

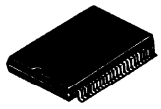


Package Information

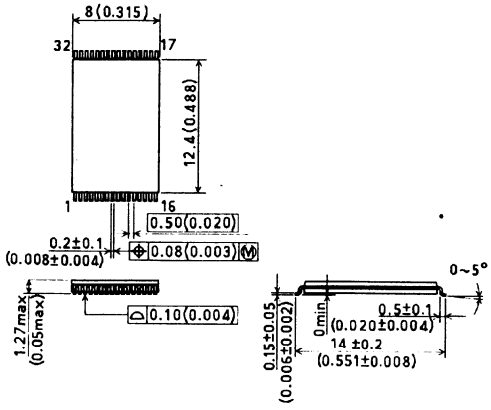
Unit: mm (inch)

•FP-48

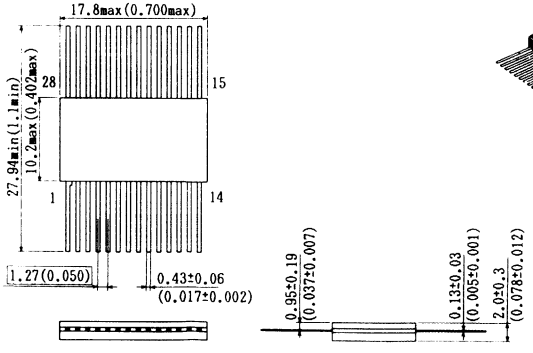


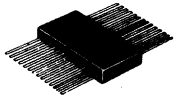


•TFP-32DA



•FG-28D





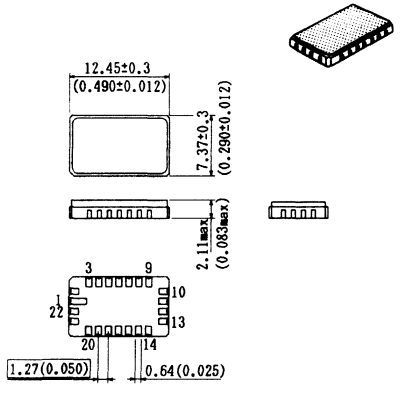
Applicable ICs

FP-24D	HM6116FP Series, HM6116LFP Series
FP-28D	HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series, HN58C65FP Series, HN58C66FP Seires, HN58C256FP Series
FP-28DA	HM6264AFP Series, HM6264ALFP Series, HM6264ALFP-L Series, HM62256FP Series, HM62256LFP Series, HM62256LFP-SL Series, HM65256BFP Series, HM65256BLFP Series, HM53051FP Series, HN623257F, HN623258F, HN62321F, HN62321BF, HN62331F, HN62321EF, HN62331EF, HN58C65FP, HN58C66FP, HN58C256FP, HN27C256AFP
FP-32D	HM628128FP Series, HM628128LFP Series, HM628128LFP-SL Series, HM658128DFP Series, HM658128LFP Series, HN62321AF, HN62331AF, HN62304BF, HN62324BF, HN27C101FP, HN27C101A Series, HN27C301FP, HN27C301AFP, HM658512DFP Series, HM658512LFP Series, HM658512LFP-L Series, HM658128ADFP Series, HM658128ALFP Series, HM658128ALFP-L Series, HN62308BF
FP-44A	HN62412FP, HN62422FP, HN62404FP, HN62424FP, HN62408FP
FP-48	HM62404F, HM62424F, HM62408F, HN624016F
TFP-32DA	HN58C257TS Series, HN29C101TS Series
FG-28D	HM10494F Series, HM100494F Series, HM10149F Series, HM10504 Series

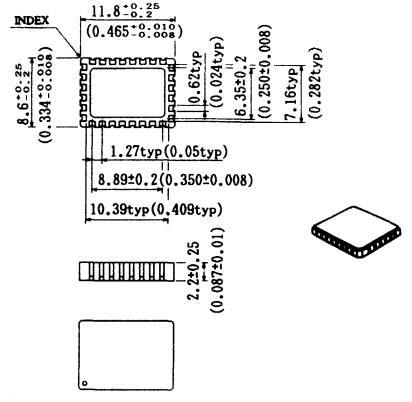
Chip Carrier

Unit: mm (inch)

•CG-22A



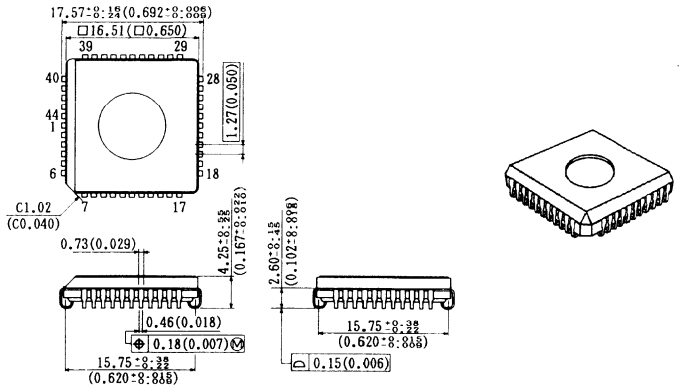
•CG-28



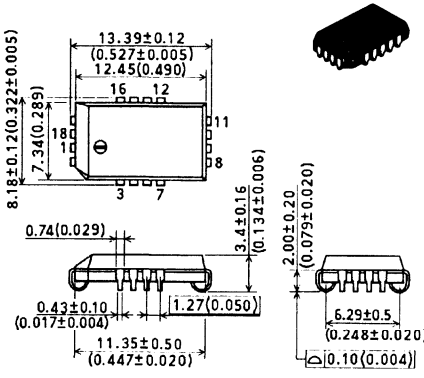
Package Information

Unit: mm (inch)

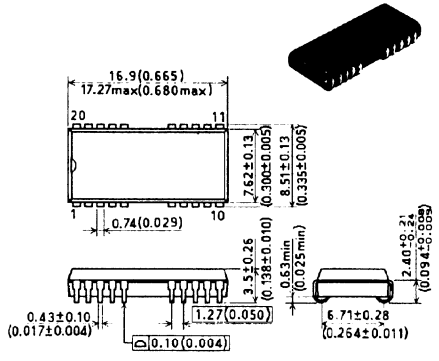
•CC-44



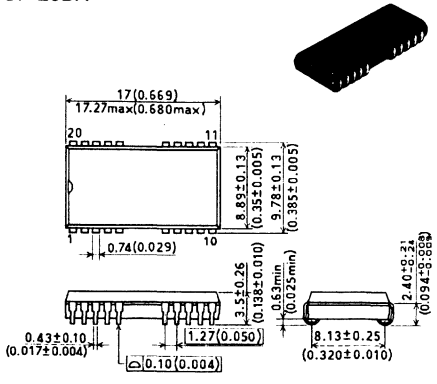
•CP-18



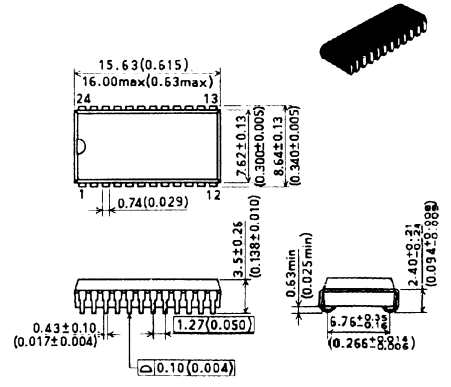
•CP-20D



•CP-20DA

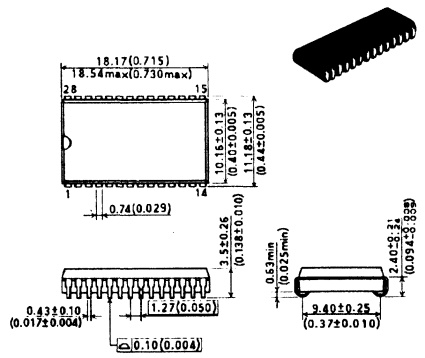


•CP-24D

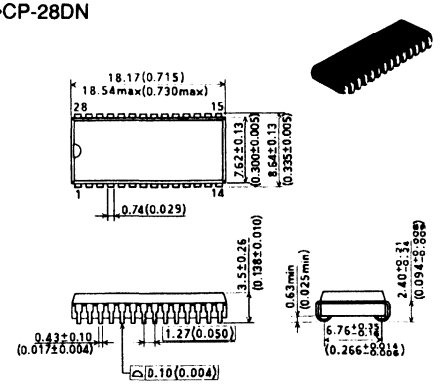


Unit: mm (inch)

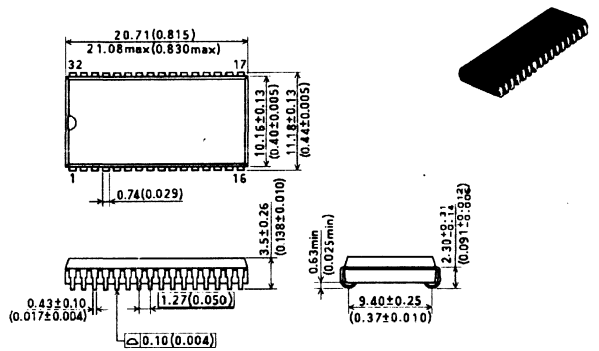
•CP-28D



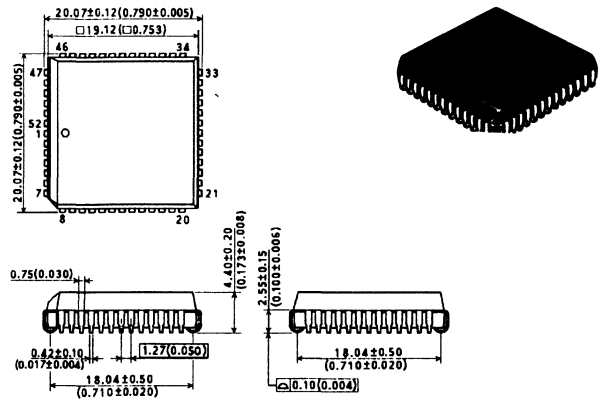
•CP-28DN



•CP-32D



•CP-52



Package Information

Applicable ICs

CG-28	HM100500 Series, HM101500 Series
CG-28B	HM100500CG-18 Series
CC-44	HM27C1024HCC Series, HN27C4096CC Series
CP-18	HM50464CP Series, HM50256CP Series, HM51256CP Series, HM51256LCP Series
CP-20D	HM514256AJP Series, HM514256ALJP Series, HM514256HJP Series, HM514258AJP Series, HM514266AJP Series, HM511000AJP Series, HM511000ALJP Series, HM511000HJP Series, HM511001AJP Series, HM511002AJP Series
CP-20DA	HM514100JP Series, HM514101JP Series, HM514102JP Series, HM514400JP Series, HM514402JP Series, HM514410JP Series
CP-24D	HM6288JP Series, HM6288LJP Series, HM6789JP Series, HM6789HJP Series, HM6287HJP Series, HM6287HLJP Series, HM6708JP Series, HM6787HJP Series, HM6707JP Series, HM100490JP Series, HM6289JP Series, HM6289LJP Series, HM6208HJP Series, HM6208HLJP Series, HM6207HJP Series, HM6207HLJP Series HM53461 Series, HM53462 Series
CP-28D	HM624256JP Series, HM624256LJP Series, HM534251JP Series, HM534252JP Series
CP-28DN	HM571000JP Series, HM62832JP Series, HM62832LJP Series, HM62832HJP Series, HM62832HJLP Series, HM62832UHP Series, HM62832UHL Series, HM63921 Series, HM63941 Series, HM574256JP Series, HM57100JP Series
CP-32D	HM624257JP Series, HM624257LJP Series, HM100506 Series
CP-52	HM62A168CP Series, HM62A188CP Series

1. Structure

IC memory devices are classified as MOS type: slow with large capacities. There are advantages to it's circuit design, layout pattern, degree of integration, and manufacturing process.

All Hitachi memories are produced using standardized design, manufacturing, and inspection techniques. Reliability, a key factor in Hitachi IC design and usage, is enhanced by Test Element Group (TEG) evaluation. This approach ensures the best possible application of our experience and knowledge at every step of IC development.

IC memories consist of memory cells which are circuit patterns arranged within a device at very high density. Examples of memory cell circuitry of MOS memories are shown in Table 1.

The dies of IC memories are encapsulated in various packages. The most common packages are plastic and cerdip. Plastic packages are widely used in many different types of equipment. Cerdip packaging is especially suitable in equipment requiring high reliability. Surface mount packages, such as the plastic leaded chip carrier (PLCC) and small outline package (SOP) have been developed for high density applications.

Hitachi has developed new techniques of IC packaging, thus achieving high levels of reliability. Hitachi plastic IC packages have been improved to match the performance of other hermetically sealed packages.

Table 2 illustrates the appearance and relative sizes of various Hitachi IC packages.

Table 1 Basic Memory Cell Circuit of IC Memories

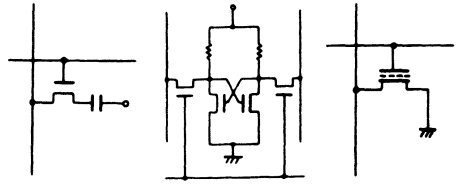
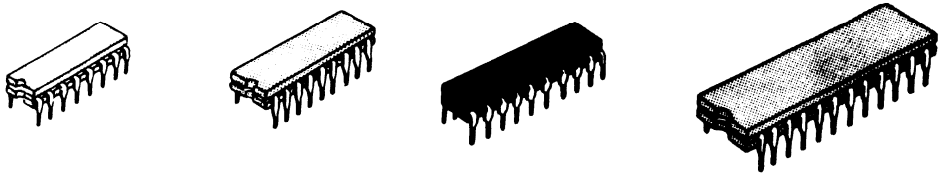
Classification	NMOS Memory (Dynamic RAM)	NMOS, CMOS Memories (Static RAM)	NMOS Memory (PROM)
Application	Main memory of computers from microcomputer to super computer		Microcomputer control use
Example of basic cell circuit			

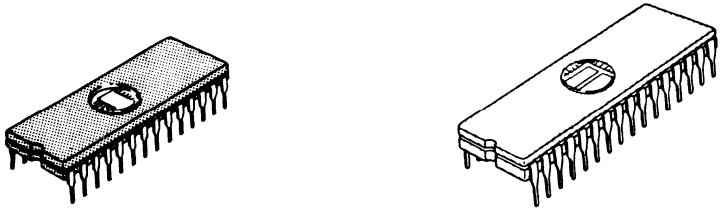
Table 2 IC Memory Package Outline

■ Cerdip

• 16 pin • 18 Pin • 20 Pin • 24 Pin

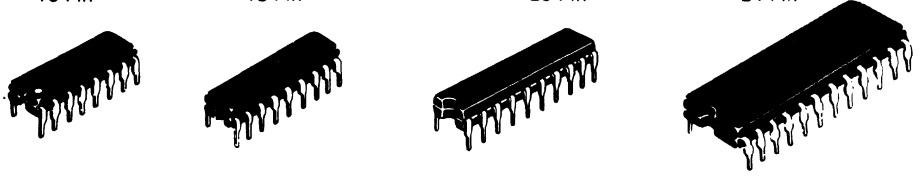


• 28 Pin with Lid • 32 Pin with Lid



■ Plastic DIP

• 16 Pin • 18 Pin • 20 Pin • 24 Pin



• 24 Pin • 28 Pin • 28 Pin

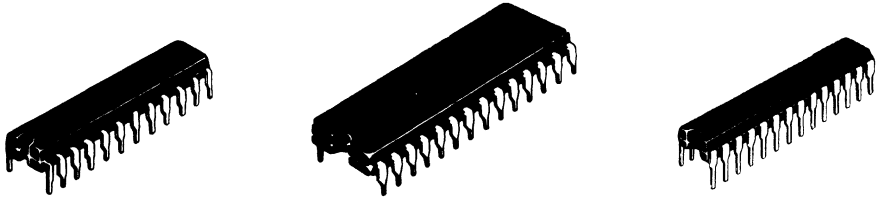
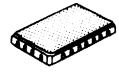


Table 2 IC Memory Package Outline (cont)

■ Leadless Chip Carrier

● 20 Pin

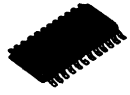
● 22 Pin



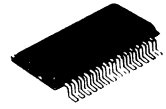
● 24 Pin

■ SOP

● 24 Pin



● 28/32 Pin

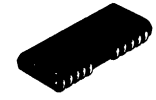


■ PLCC

● 18 Pin

■ SOJ

● 20/26/28/32 Pin



2. Reliability

Hitachi IC memory reliability test results are listed below.

2.1 Reliability Test Data of Hi-BiCMOS Memory

Hi-BiCMOS memory is a recently developed design, based on the latest fine process technologies. Hi-BiCMOS memory offers a combination of the best features of other, earlier devices—the low power consumption and high integrity of CMOS devices, plus the high speed and high drive capability of bipolar (ECL) circuits. Hi-BiCMOS memory also supports the input and output levels of both ECL and TTL devices, which allows interfacing with other devices.

The reliability test data for HM100500CG-18 (256k × 1 bit) and HM6788HP-15 (16k × 4 bits) is listed in Tables 3 and 4.

In normal use, Hi-BiCMOS memory reliability is affected by some limitations based on the circuit composition. Besides the normal constraints of CMOS and bipolar device design, Hi-BiCMOS memory should not be used in applications involving deformed or slow signal waveforms that may cause latch-up or other malfunctions. For further information, refer to the detailed specifications on the data sheet for each Hi-BiCMOS device.

Table 3 Results of Hi-BiCMOS Memory Reliability Tests (1)

	HM100500CG-18 (LCC)					HM6788HP-15 (Plastic)					
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate	Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate	Remarks
High-temperature pulse operation	Ta = 125°C V_{EE} = –4.5V	380	C.H. 3.8×10^5	0	1/h 2.4×10^{-6}	High-temperature pulse operation	Ta = 125°C V_{CC} = 7.0V	420	C.H. 4.2×10^5	1*	1/h 4.8×10^{-6}	* foreign matter
						Moisture endurance	85°C 85% RH 5V	210	2.1×10^5	0	4.8×10^{-6}	
High-temperature storage	Ta = 200°C	330	3.3×10^5	0	3.0×10^{-6}	Pressure cooker	121°C 100% RH	80	0.16×10^5	0	5.8×10^{-5}	

Table 4 Results of Hi-BiCMOS Memory Reliability Tests (2)

		HM100500CG-18 (LCC)		HM6788HP-15 (Plastic)	
Test Item	Test Condition	Samples	Failures	Samples	Failures
Temperature cycling	–55° to +150°C, 100 cycles	180	0	180	0
Soldering heat	260°C, 10 seconds	22	0	22	0
Thermal shock	0° to +100°C, 10 cycles	50	0	50	0
Mechanical shock	1500 G, 0.5 ms, three times each for X, Y and Z axes	22	0	—	—
Variable frequency vibration	100 to 200 Hz, 20 G, three times each for X, Y and Z axes	22	0	—	—
Constant acceleration	20000 G, 1 minute, each for X, Y and Z axes	22	0	—	—

2.2 Reliability Test Data of MOS Memory

2.2.1 MOS DRAM and SRAM Tests

Tables 5, 6 and 7 show the reliability test data on 1-Mbit DRAMs (HM511000, HM514256), 4-Mbit DRAMs (HM514100/HM514400), 256-kbit SRAM (HM62256), and 1-Mbit SRAM (HM628128FP). The life test is performed at high temperature and high voltage to evaluate product reliability using many samples. For all failures identified in the manufacturing process, the data is analyzed in great detail to improve the quality and reliability of both the process and the finished product.

Table 5 Reliability Data on 1M MOS DRAM

		HM511000P/HM514256P Series (DIP)				HM511000JP/HM514256JP Series (Plastic)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Remarks
High-temperature pulse operation	125°C/5.5 V	300	6.00×10^5	0	1.53×10^{-6}	200	4.00×10^5	0	2.30×10^{-6}	* Oxide film failure ×1
	125°C/7 V	1252	4.50×10^5	1*	4.48×10^{-6}	3186	9.34×10^5	0	9.85×10^{-7}	
	150°C/7 V	200	4.00×10^5	0	2.30×10^{-6}	200	4.00×10^5	0	2.30×10^{-6}	
Moisture endurance	85°C 85% RH 5.5 V	420	8.40×10^5	0	1.10×10^{-6}	682	1.36×10^6	0	6.74×10^{-7}	
Pressure cooker	121°C/100% RH	150	4.50×10^4	0	2.04×10^{-5}	200	6.00×10^4	0	1.53×10^{-5}	

Note: Confidence level 60%

Table 6 Reliability Data on 4M DRAM

		HM514100JP/HM514400JP Series (SOJ)				HM514100ZP/HM514400ZP Series (ZIP)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Remarks
High-temperature pulse operation	125°C/5.5 V	364	7.28×10^5	0	1.37×10^{-6}	—	—	—	—	* Foreign ×1
	125°C/7 V	307	6.14×10^5	0	1.63×10^{-6}	100	2×10^5	0	5×10^{-6}	
	150°C/7 V	153	3.06×10^5	1*	3.27×10^{-6}	100	2×10^5	0	5×10^{-6}	
Moisture endurance	85°C 85% RH 5.5 V	307	6.14×10^5	0	1.63×10^{-6}	250	5×10^5	0	2×10^{-6}	
Pressure cooker	121°C/100% RH	100	3×10^4	0	3.33×10^{-5}	100	3×10^4	0	3.33×10^{-5}	

Note: Confidence level 60%

Table 7 Reliability Data on 256K and 1M MOS SRAM

		HM62256FP (SOP)				HM628128FP (SOP)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Remarks
High-temperature pulse operation	125°C/5.5 V	3088	3.11×10^{6}	0	8.88×10^{-7}	1038	1.04×10^{6}	0	8.86×10^{-7}	*1
	125°C/7 V	455	4.55×10^{5}	0	2.02×10^{-6}	951	5.33×10^{5}	1*1	3.79×10^{-6}	Foreign ×2
	150°C/7 V	103	1.00×10^{5}	1*1	2.02×10^{-5}	80	1.60×10^{5}	0	5.75×10^{-6}	
Moisture endurance	85°C/85% RH 7 V	680	6.80×10^{5}	0	1.35×10^{-6}	127	2.54×10^{5}	0	3.62×10^{-6}	*2 Leak ×1
Pressure cooker	121°C/100% RH	320	6.40×10^{4}	1*2	3.16×10^{-5}	90	2.70×10^{4}	0	3.41×10^{-5}	

Note: Confidence level 60%

2.2.2 Reliability Test Data on EPROM

There are two types of EPROM: the conventional EPROM with a transparent window over the active device area; and the one-time-programmable ROM (OTPROM) packaged in plastic. Table 8 shows the reliability test data on EPROM types 512 kbit (HN27512, HN27512P) and 1 Mbit (HN27C101, HN27C301).

The high temperature failures shown in Table 8 are due to data dissipation in the memory cells. By absorbing thermal energy, the electrons in the floating gates are activated and dissipated. In actual usage, however, this is not a significant problem since this phenomenon is highly dependent on temperatures (about 1.0 eV of activated energy) that should not appear during normal operation.

The moisture resistance of the OTPROM is satisfactory.

Table 9 shows an example of PROM derating. The primary derating parameter is generally temperature since other operating parameters are specified. The maintaining of low junction temperature during device mounting is especially important for a stable application operation (relative to access time, refresh time, and other characteristics).

Table 8 Reliability Data on 512-kbit and 1-Mbit MOS EPROMs

		HN27512 (Cerdip/Plastic)				HN27C101/HN27C301				
Test Item	Test Condition	Samples	Total Test Time*	Failures	Failure Rate[Note] (1/hr)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Remarks
High-temperature pulse operation	125°C/5.5 V	200	3.72×10^5	0	2.47×10^{-6}	180	3.24×10^5	0	2.84×10^{-6}	* Data dissipation×49
	125°C/7 V	530	7.95×10^5	0	1.16×10^{-6}	327	6.54×10^5	0	1.41×10^{-6}	
High-temperature bake	175°C	260	4.91×10^5	0	1.87×10^{-6}	150	7.5×10^5	0	1.23×10^{-6}	
	200°C	240	3.72×10^5	1*	5.43×10^{-6}	130	6.49×10^5	1*	3.11×10^{-6}	
	250°C	180	1.89×10^5	7*	4.44×10^{-5}	110	3.07×10^5	40*	1.30×10^{-4}	
Moisture endurance	85°C/85% RH 5.5 V	290	5.22×10^5	0	1.76×10^{-6}	—	—	—	—	Data of 512K OTPROM
Pressure cooker	121°C/100% RH	50	0.10×10^5	0	9.20×10^{-5}	—	—	—	—	

Note: Confidence level 60%

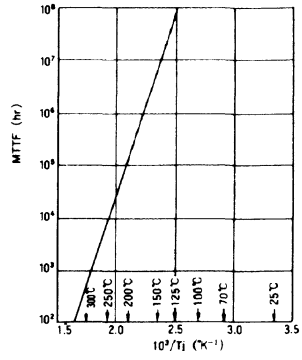
2.2.3 Reliability Test Data on MASK ROM

Table 10 shows the reliability test data for the 8-Mbit and 4-Mbit MASK ROMs. The MASK ROM is patterned in the manufacturing process, so data dissipation is not generated during high temperature operations, unlike EPROM and EEPROM devices.

Table 9 Example of HN27C101/HN27C301 Derating

Factor	Temperature
Failure criteria	Electrical characteristics, function test
Failure mechanism	Increase of leakage current, and others

Results:
The result of high temperature baking of the PROM is shown in the figure at right.



Note: As shown in the figure, decreasing junction temperature will improve reliability. The junction temperature can be calculated by the formula: $Tj = Ta + \theta ja \cdot Pd$ where θja is about 100°C/W with no air flow and about 60° to 70°C/W with 2.5 m/s air flow.

Table 10 Reliability Data on 2-Mbit and 4-Mbit MASK ROMs

		HN62408P (Plastic)				HN62404P (Plastic)				
Test Item	Test Condition	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Samples	Total Test Time	Failures	Failure Rate[Note] (1/hr)	Remarks
High-temperature pulse operation	125°C/5.5 V	—	—	—	—	200	4.0×10^5	0	2.3×10^{-6}	
	125°C/7 V	130	1.3×10^5	0	7.08×10^{-6}	300	3.0×10^5	0	3.0×10^{-6}	
Moisture endurance	85°C/85% RH 5.5 V	150	1.5×10^5	0	6.13×10^{-6}	120	1.20×10^5	0	7.67×10^{-6}	
Pressure cooker	121°C/100% RH	90	4.5×10^4	0	2.0×10^{-5}	45	2.3×10^4	0	4.1×10^{-5}	

Note: Confidence level 60%

2.2.4 Reliability Test Data on MOS Memory (environmental testing)

Tables 11 and 12 list MOS memory environmental test data, showing excellent results without any failures, even in severe environments.

In MOS transistor operations, VTH is a basic process parameter. While in use, MOS memory exhibits almost no change in VTH, largely due to designed-in surface stabilization technology and extremely clean production processes.

Figure 3 shows examples of time changes for minimum VDD and access time tRAC for 1-Mbit DRAM under high temperature pulse test conditions.

2.3 Change of Electrical Characteristics on IC Memories

The degradation of I_{CBO} and h_{FE} are the main factors of performance degradation for inner cell transistors in bipolar memory. The actual element design, however, specifies the operation in a range at which no degradation occurs. In this normal situation, no changes in the operating characteristics, including access time, will arise. Time dependencies in the access time for the HM100500 and HM6788H are shown in Figures 1 and 2.

Table 11 Reliability Data on MOS Memory (1)

		HM511000P (DIP)		HM511000JP (SOJ)		HM62256FP (SOP)		HM628128FP (SOP)		EPROM (Cerdip)		
Test Item	Test Condition	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	Remarks
Temperature cycling	–55° to 150°C 10 cycles	3755	0	2786	0	3328	0	710	0	2790	0	
Temperature cycling	–55° to 150°C 500 cycles	150	0	200	0	482	0	105	0	450	0	
Thermal shock	–65° to 150°C 15 cycles	77	0	100	0	76	0	77	0	80	0	
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	22	0	22	0	
Mechanical shock	1500 G, 0.5 ms	—	—	—	—	—	—	—	—	38	0	
Variable frequency vibration	100 to 2000 Hz 20 G	—	—	—	—	—	—	—	—	38	0	
Constant acceleration	6000 G	—	—	—	—	—	—	—	—	38	0	6000 G

Table 12 Reliability Data on MOS Memory (2)

Test Item	Test Condition	HM514400JP (SOJ) Samples	HM514400JP (SOJ) Failures	HM154400ZP (ZIP) Samples	HM154400ZP (ZIP) Failures	HN62408P (DIP) Samples	HN62408P (DIP) Failures	HN62404P (DIP) Samples	HN62404P (DIP) Failures	Remarks
Temperature cycling	–55° to 150°C 10 cycles	949	0	450	0	205	0	329	0	
Temperature cycling	–55° to 150°C 500 cycles	100	0	100	0	45	0	45	0	
Thermal shock	–65° to 150°C 15 cycles	30	0	22	0	22	0	22	0	
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	22	0	

Example	
Device name	HM100500
Test condition	Ta = 125°C, V_{EE} = –4.5 V all bit scanning
Failure criteria	t_{AA} = 15 ns
Failure mechanism	Surface degradation
Results: Access time is stabilized.	

Example of Time Change in Access Time for HI-BI CMOS Memory

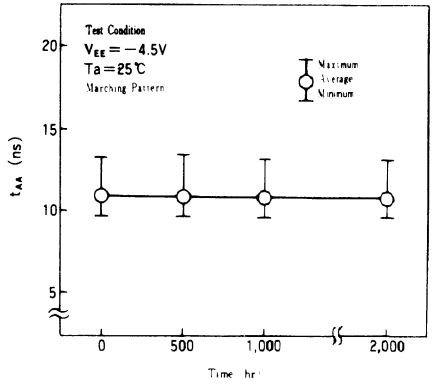


Figure 1 Time Change in Access Time for Hi-BiCMOS Memory

Example	
Device name	HM6788HP-25
Test condition	Ta = 125°C, V_{CC} = 5.0 V all bit scanning
Failure criteria	V_{CC} = 4.5 V, t_{AA} = 25 ns
Failure mechanism	Surface degradation

Results:
Both of V_{CC} (min) and t_{AA} are stabilized.

Examples of Time Change in V_{CC} min and t_{AA} for Hi-Bi CMOS Memory

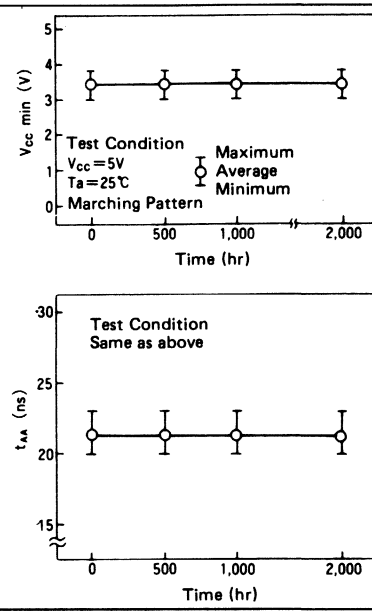


Figure 2 Time Change in Minimum V_{CC} and t_{AA} for Hi-BiCMOS Memory

Example	
Device name	HM511000P
Test condition	Ta = 125°C, V_{CC} = 7 V all bit scanning
Failure criteria	V_{DD} = 4.5 V, ΔV_{DD} = 1.0 V
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Note: Test accuracy is 0.2 V, 2 ns.

Example of Time Change in V_{DD} min and t_{RAC} for MOS Memory

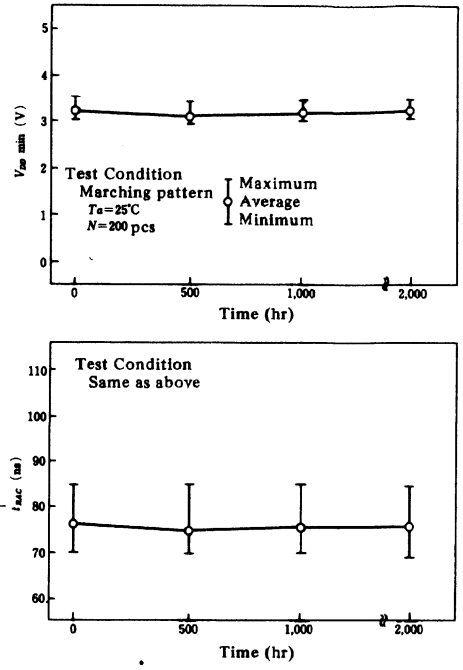


Figure 3 Time Change in Minimum V_{CC} and t_{RAC} for MOS Memory

2.4 Failure Mode Rate

Figures 4 and 5 show examples of failure modes identified in user applications. Since IC memories require the finest pattern process technology, the percentage of failures due to factors such as pinholes, photoresist defects, and foreign materials tends to increase along with product complexity. Hitachi has continued to improve it's fabrication process technology, and perform 100% high temperature "burn-in" screening as a standard part of manufacturing.

Hitachi collects and analyzes customer usage data as part of a program designed to achieve higher product reliability. This analysis is a very useful feature of the program.

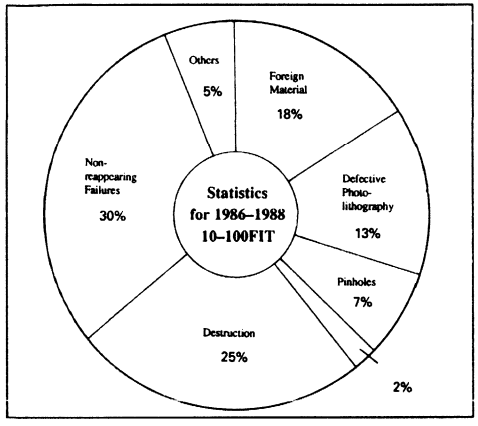


Figure 4 Failure Mode Rates for Bipolar Memory

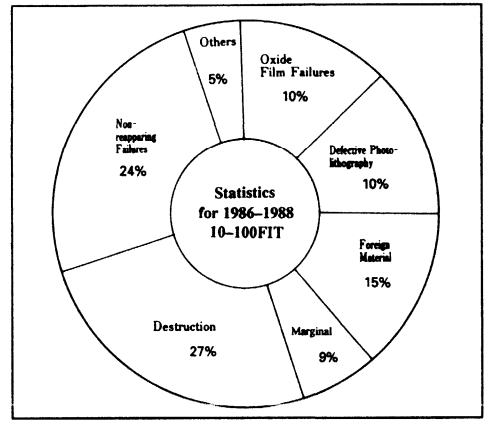


Figure 5 Failure Mode Rates for MOS Memory

3. Reliability of Semiconductor Devices

3.1 Reliability Characteristics for Semiconductor Devices

Hitachi semiconductor devices are designed, manufactured, and inspected, so as to achieve a high level of reliability. System reliability is improved by combining highly reliable components with the proper environmental conditions. This section describes the reliability characteristics, failure types and their mechanisms in terms of devices. First, the semiconductor device characteristics are examined in light of their reliability.

1. Semiconductor devices are essentially structure sensitive as seen in surface phenomena. Fabricating devices requires precise control of a large number of process steps.

2. Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

3. Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin-film surfaces sometimes exhibit different physical characteristics from the bulk quantities of identical materials.

4. Semiconductor device technology advances very quickly, therefore many new devices have been developed using new processes over a short period of time. Hence, conventional device reliability data cannot always be used for comparisons.

5. Semiconductor devices are characterized by volume production. Therefore, manufacturing variation is an important consideration.

6. Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially semipermanently operable. However, failures caused by worn or aged materials and migration should also be reviewed when electrode and package materials are not suited for particular environmental conditions.

7. Component reliability may depend on the device mounting, conditions used, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength. Device reliability is generally represented by a failure rate. "Failure" implies that a device has lost its function, and includes intermittent degradation or complete destruction.

   Generally, the failure rate of electrical components and equipment is represented by the "bathtub" curve as shown in Figure 6. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which indicates an initial failure type. Such devices ensure a long lifetime unless extreme environ-mental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be represented physically as well as statistically. Both failure aspects have been thoroughly analyzed to establish a high level of reliability.

3.2 Failure Types and Their Mechanisms

3.2.1 Failure Physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering." It is used to examine the physical mechanism of failures, in terms of atoms and molecules, to improve device reliability. This physical approach was introduced to the reliability field to answer the demand for minimized developmental cost and time. These conditions were derived from the development of solid-state physics (semiconductor physics) since the 1940's and associated the device development. Failure physics have been employed to:

1. Detect failed devices as soon as possible
2. Establish models and equations used for failure prediction
3. Evaluate the reliability in short time periods by accelerated life testing

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage, and usage, by including physics as a basic technology to conventional experimental and statistical approaches.

3.2.2 Failure Types and Their Mechanisms

The physical aspects of device failures are covered in this section. Semiconductor device failures are basically categorized as disconnection, short circuit, deterioration, and miscellaneous failures. These failures and their causes are summarized in Table 13. Typical failure mechanisms are as follows:

1. Surface deterioration
   The pn junction has a charge density of 10^{14} to 10^{20} cm^{-3}. If charges exceeding the above density are accumulated on the pn junction surface, the electrical characteristics of the junction will tend to vary. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by the surface channels still exists. Surface deterioration depends heavily on the applied temperature and voltage and is often handled by the reaction model.
   An example of a recent failure is the surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS}, thus raising the internal voltage and establishing a strong electric field near the drain of the MOS device. This may be a result from reduced device geometry (from 2 μm to 0.8 μm) as technological advances have occurred in production methods. Generated hot carriers may affect the surface boundary characteristics on a section of the gate oxide film, resulting in the degradation of the threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have consistently employed improved designs and process techniques to prevent these problems. However, as processes become even finer, surface deterioration may become a serious problem.

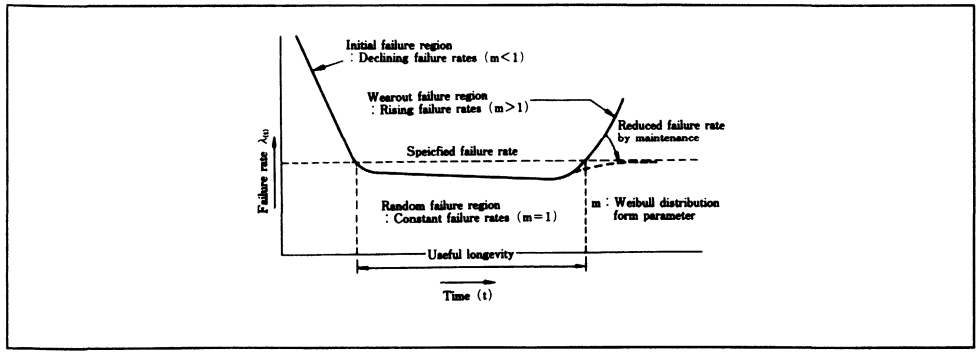


Figure 6 Typical Failure Rate Curve

2. Electrode-related failures

The concern for electrode-related failures has increased as multilayer wiring has become more complex. Noticeable failures include electromigration and Al wiring corrosion in plastic sealed packages.

a. Electromigration

This phenomenon takes place when metal atoms are moved by a large current of about 10^6 A/cm^2 that is supplied to the metal. When ionized atoms collide with the current of electrons, an "electron wind" is produced. This wind moves the metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at the opposite side. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause short circuits in multimetal lines.

b. Multimetal line related failures

Major failures associated with multimetal lines include increased leakage currents, short circuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

c. Al line corrosion and disconnection

When plastic encapsulated devices are subjected to high temperatures, high humidity, or a bias-applied condition, the Al electrodes in the devices can cause corrosion or disconnection (Figure 7). Under high temperature and high humidity, corrosion is randomly generated over the element surface.

However, after an extended period of time, such corrosion does not significantly increase. This type of failure is possibly due to initial failures associated with manufacturing variances. It is also known that such failures can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-applied, high temperature, high humidity condition, on the other hand, pit corrosion is generated in higher potential areas while in lower potential areas, intergranular corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Figure 8.

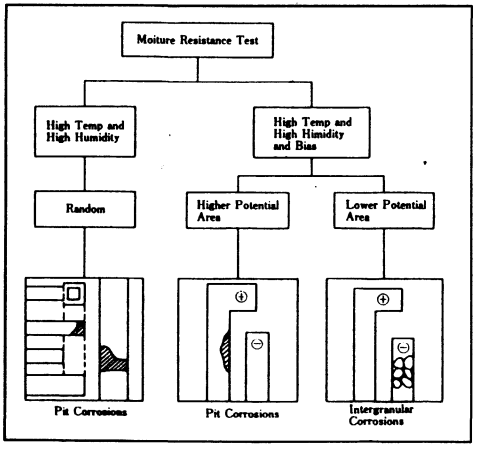


Figure 7 Categorized Al Corrosions

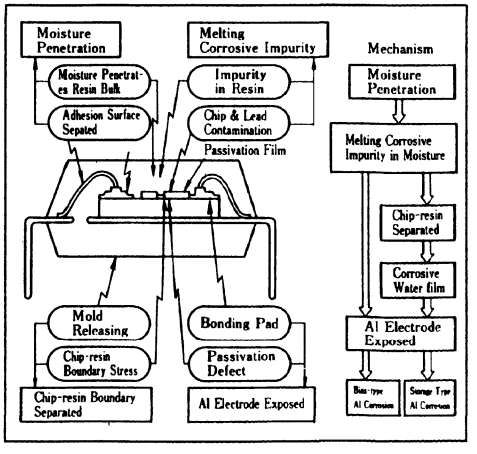


Figure 8 Plastic Package Cross Section and Al Corrosion Mechanism

3. Bonding related failures

   a. Degradation caused by intermetallic formation
   Bonding strength degradation and contact resistance increase are caused by compounds formed in the connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

   b. Wire creep
   Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introduced to the intergranular system. Bonding under usual conditions with no loop configuration failures does not cause this failure, unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

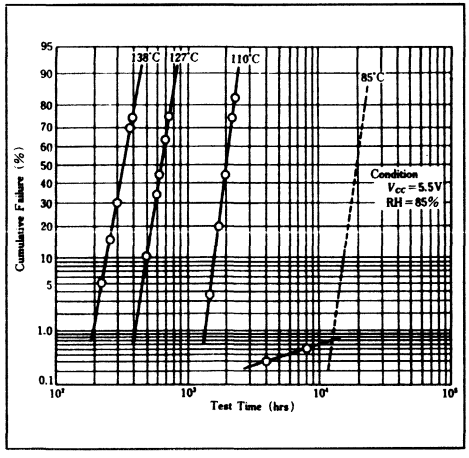


Figure 9 An Example of Moisture Resistance by High Temperature, High Humidity, and High Bias

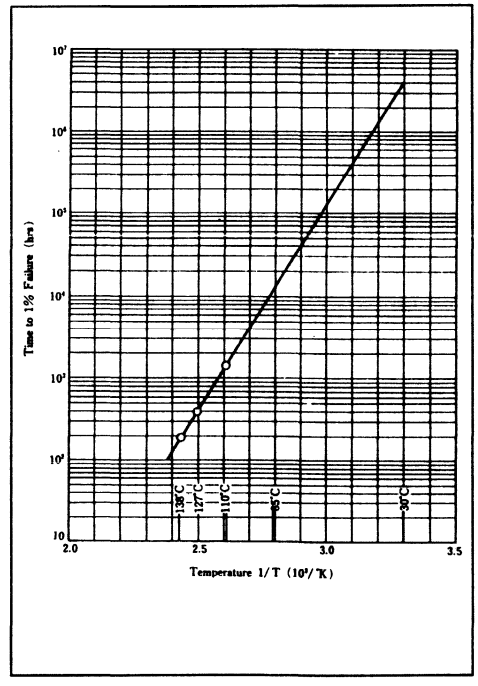


Figure 10 Relationship Between Temperature and Time to 1% Failure (RH = 85%)

c. Chip crack
With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

d. Reduced maximum power dissipation
For power devices, heat fatigue due to thermal expansion coefficient mismatches among different materials deteriorates thermal resistance. This results in decreased maximum power dissipation.

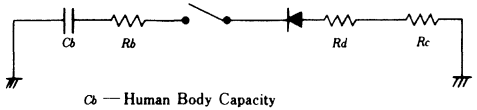
4. Sealing related failures
Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

— Al line corrosion on the chip surface due to slight moisture and reactions between different ionized materials.
— Intermittent moving foreign metals causing short circuiting.
— Al line corrosion due to extraneous H_2O caused by hermetic failure.

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parasitic effects and metal shorts. The foreign matter detection method is specified by the MIL-STD-883C, PIND (particle impact noise detection) test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying it.

5. Disturbance

a. Electrostatic discharge destruction
Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure: the human body model, a charged device model, and a field induced model.
The human body is easily charged. A person just walking across a carpet can be charged up to 15,000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Figure 11. The human body's capacitance C_b and resistance R_b are 100 to



Cb — Human Body Capacity
Rb — Human Body Resistance
Rd — Device Resistance
Rc — Resistance Between Device and Ground

$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} J$

Figure 11 Equivalent Circuit of the Human Body Model

200 pF and 1000 to 2000 Ω, respectively. Assuming a body is charged with 2000 V, the dissipated energy is obtained as follows: With a time constant of 10^{-7}s, the dissipated energy is 2 kW, which is enough to destroy a small area of a chip.

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Figure 12. Device size and device position relative to ground are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by nearby high voltage. Since the capacitors or leads of a device act like antennas, the following cases will possibly cause it's destruction.

— A device is incorporated into a high electric field such as a CRT,
— a device is left under a high-frequency electric field, and
— a device is moved within a container charged at high voltage, such as a tube.

b. Latch-up

Latch-up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, and unregulated power supply, or noise is applied, or when a device is operated from two sources having different setup voltages. These cases can cause input or output current to flow in the opposite direction from the usual flow, which triggers parasitic thyristors. This results in an excessive current flowing between a power supply and ground. This phenomenon continues until the power is removed or the current flow is reduced to a certain level. Once latch-up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch-up. Input or output currents that trigger latch-up start to flow under the following conditions.

$V_{in} > V_{CC}$ or $V_{in} < GND$ for input level
$V_{out} > V_{CC}$ or $V_{out} < GND$ for input level

Circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

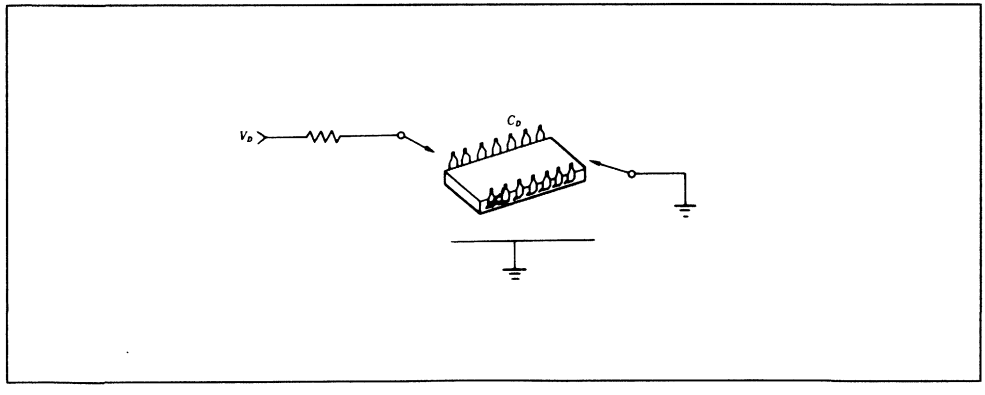


Figure 12 Equivalent Circuit of a Charged Model

c. Soft errors

When α-particles are generated from uranium or thorium on or near the silicon surface of an LSI chip and bombard the Si substrate, electron-hole pairs are formed. They act as noise to memory cell nodes and data lines, which results in data errors. This type of error occurs temporarily and is called a soft error. This phenomenon is shown in Figure 13. Only electrons from among the electron-hole pairs are collected into a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, an organic material, PIQ, is applied to the surface of the device.

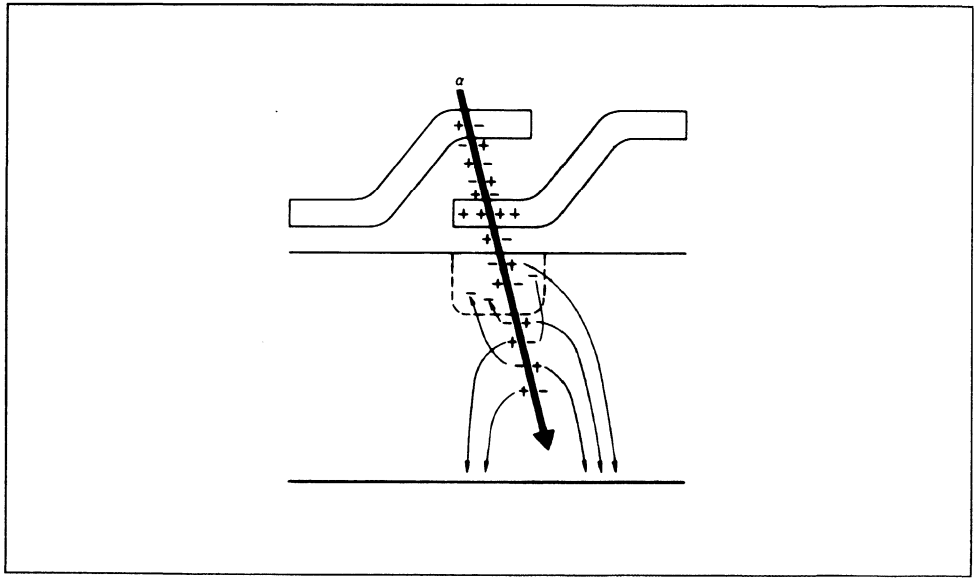


Figure 13 Soft Errors Caused by α-Particles in Dynamic Memory

Table 13 Failure Causes and Mechanisms

Failure Related Causes		Failure Mechanisms	Failure Modes
Passivation	Surface oxide film, insulating film between wires	Pin hole, crack, uneven thickness, contamination, surface inversion, hot carrier injected	Withstanding voltage reduced, short, leak current increased, h_{FE} degrated, threshold voltage variation, noise
Metallization	Interconnection, contact, through hole	Flaw, void, mechanical damage, break due to uneven surface, non-ohmic contact, insufficient adhesion strength, improper thickness, electromigration, corrosion	Open, short, resistance increased
Connection	Wire bonding, ball bonding	Bonding runout, compounds between metals, bonding position mismatch, bonding damaged	Open, short resistance increased
Wire lead	Internal connection	Disconnection, sagging, short	Open, short
Diffusion, junction	Junction diffusion, isolation	Crystal defect, crystallized impurity, photo resist mismatching	Withstanding voltage reduced, short
Die bonding	Connection between die and package	Peeling chip, crack	Open, short, unstable operation, thermal resistance increased
Package sealing	Package, hermetic seal, lead plating, hermetic package and plastic package, filler gas	Integrity, moisture ingress, impurity gas, high temperature, surface contamination, lead rust, lead bend, break	Short, leakage current increased, open, corrosion disconnection, soldering failure
Foreign matter	Foreign matter in package	Dirt, conducting foreign matter, organic carbide	Short, leakage current increased
Input/output pin	Electrostatistics, excessive voltage, surge	Electron destroyed	Short, open, fusing
Disturbance	α particle	Electron hole generated	Soft error
	High electric field	Surface inversion	Leakage current increased

6. Fine Geometry Related Problems
   As computer component and memory designs have required greater functionality and integration, LSI circuit geometry has been reduced up to 0.8 μm, and further reductions are expected.

However, while transmission line dimensions have undergone this substantial reduction in size, power supplies have not been correspondingly adjusted for 5 V use. Problems associated with finer geometries are shown in Table 14.

Table 14 Finer Geometry Related Problems

Item	Problems	Countermeasure
5 V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Guttering • Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical and horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

1. Views on Quality and Reliability

Hitachi products should always meet individual users' purposes and required quality levels, maintaining satisfactory performance for general applications. Hitachi works continuously to assure high reliability standards for our IC memories in actual usage. To meet user needs and to cover expanding applications, Hitachi has defined these goals:

1. Establish reliability by design during new product development.
2. Establish quality at all steps in the manufacturing process.
3. Strengthen the inspection process at all points.
4. Improve product quality based on user data.

Furthermore, to reach the highest quality and performance levels, development and production teams cooperate very closely with Hitachi research laboratories. All these methods together make it possible for Hitachi to meet and exceed user requirements.

2. Reliability Design of Semiconductor Devices

2.1 Reliability Targets

The establishment of reliability targets is important in manufacturing and marketing, as well as in determining function and price. Practically, the reliability targets cannot be determined from failure rates produced by any single common test condition; they are based on many factors such as equipment characteristics, target system purposes, derating applied during design, operating conditions, and maintenance requirements.

2.2 Reliability Design Factors

Timely analysis and execution are essential to achieve performance based on reliability targets. The primary design items of interest are design standardization, device process and structural design, design review, and reliability testing.

1. Design standardization
   Design standardization requires the establishment of design rules and the specification of parts, materials, and processes. When design rules are being established for the circuit, cell, and layout designs, critical quality and reliability features should also be examined. By doing this effectively, the use of standardized processes or materials, even in newly developed products, should generate much higher reliability (with the possible exception of special requirements or functions).

2. Device process and structural design
   It is important during device design to consider the total balance of process design, structural design, and circuit and layout design. Especially in the case of applying new processes or new materials, at Hitachi we study the technology in depth prior to any detailed device development.

3. Reliability testing by test site
   The test site is also called the test pattern. It is a useful method for evaluating the reliability of complex ICs and complicated functions.

   a. The purposes for the test site are:
   — To make clear definitions about fundamental failure modes
   — To analyze relationships between failure modes and manufacturing processes and/or conditions
   — To analyze failure mechanisms
   — To establish QC points in manufacturing

   b. The effects of the test site are:
   — Evaluation of common fundamental failure modes and failure mechanisms
   — Determination of predominant failure modes, and comparisons with field experiences
   — Analysis of relationships between failure causes and manufacturing factors
   — Simplification of testing

2.3 Design Review

Design review is a method to systematically confirm whether or not a design satisfies the performance required by users, whether it meets all specifications, and whether the technical items accumulated in test data and application data are effectively utilized.

In addition, from the standpoint of comparisons to competitive products, a major focus of the design review is to insure the quality and reliability of the product. At Hitachi, the design review is performed as a part of new product development, and when changing existing products.

The following items are considered in design review.

1. Describe the product based on specified design documents.
2. Plan and execute each product function and program (such as calculations) by considering the product and its documentation from the standpoint of each participant. Experiments and further investigations are indicated if any results are not exactly as expected.
3. Determine the contents and methods of reliability testing based on design documents and drawings.
4. Check manufacturing process ability to achieve design goals.
5. Arrange preparations for production.
6. Plan and execute each product function and program of all design changes proposed by individual specialists. Generate tests, experiments, and calculations as needed to confirm the results of each design change.
7. Refer to past performance and failure experiences with similar devices. Confirm the prevention of any repetition of such experience, and plan and execute a test program to prove this level of performance.

At Hitachi, design reviews including these steps of analysis and decision are made using individual check lists according to each objective.

3. Quality Assurance System of Semiconductor Devices

3.1 Activity of Quality Assurance

At Hitachi, these are the general purposes of quality assurance:

1. Problems are resolved within each step, so that by the final stage of production even very small potential failure factors will be removed.
2. Information developed at every step is used in other steps, as indicated, to improve quality in the entire production sequence, and therefore achieve satisfactory levels of reliability and performance.

3.2 Qualification

For maximum product quality and reliability, qualification tests are done at each stage of trial production and mass production, based on design reliability as described in Section 2 "Reliability Design of Semiconductor Devices."

These are the purposes of qualification at Hitachi.

1. Qualify the product objectively from a customer standpoint (as by a third party).
2. Consider the failure experiences and data provided by customers.
3. Qualify every change in design and process.
4. Qualify, with special emphasis, all final choices of parts, materials, and processes.
5. Establish control points within the production procedure by considering the process ability and factors of manufacturing variance.

Figure 1 shows the general outline of design qualification at Hitachi.

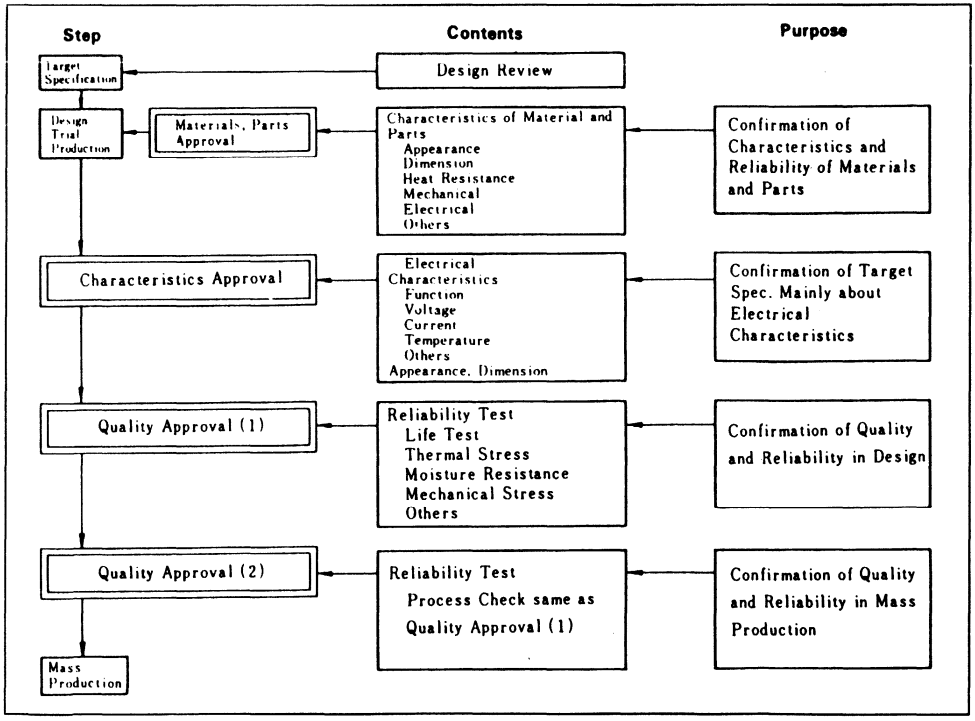


Figure 1 Flowchart of Device Design Qualification

3.3 Quality and Reliability Control in Mass Production

In mass production, quality is the functional responsibility of each department, primarily as defined by the manufacturing department and the quality assurance department. The total function flow is shown in Figure 2.

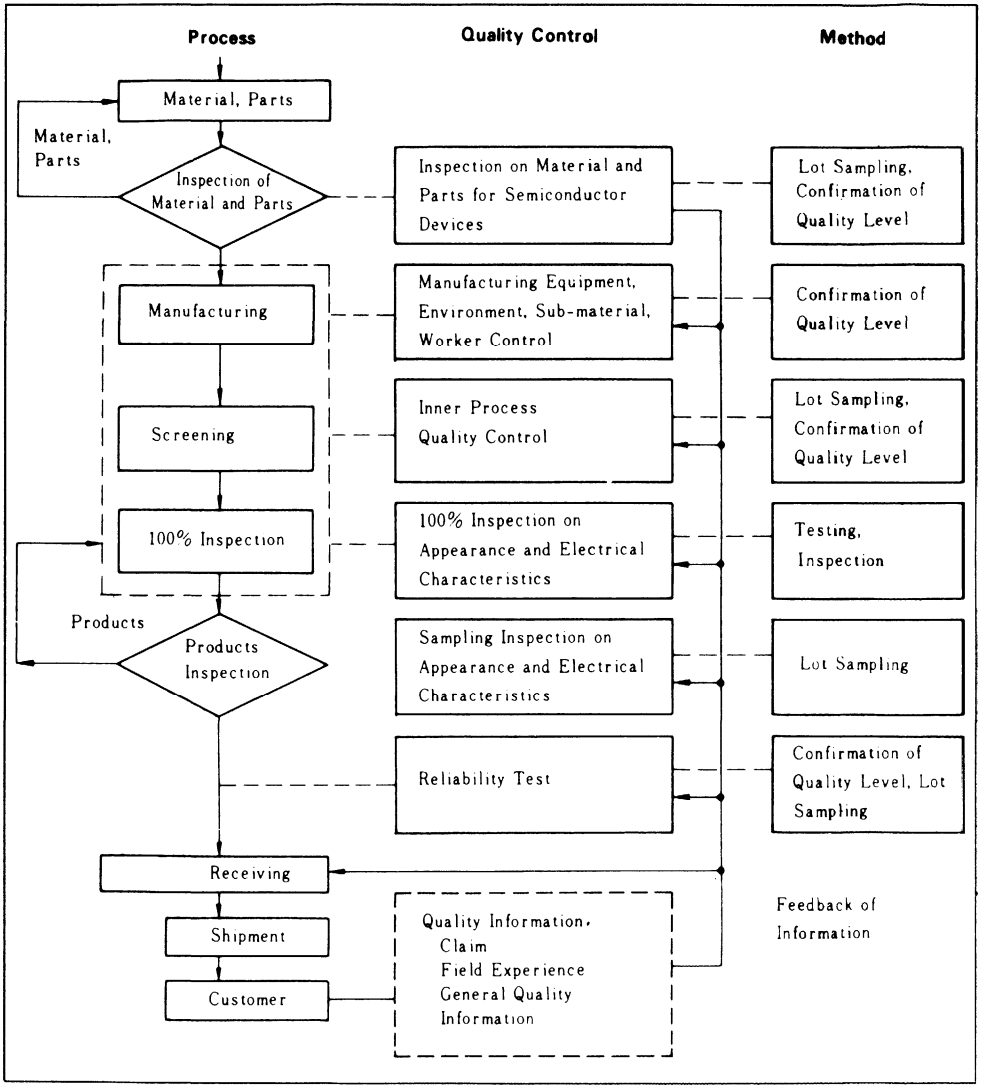


Figure 2 Flowchart of Quality Control in the Manufacturing Process

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, the quality control of parts and materials becomes more important. Items such as crystals, lead frames, fine wire for wire bonding, packages and materials required in manufacturing processes like mask patterns and chemicals, are all subject to inspection and control.

Besides the qualification of parts and materials as stated in Section 3.2, the quality control of parts and materials begins at incoming inspection, which is performed based on purchase specifications, drawings and (mainly) sampling tests based on MIL-STD-105D. Other activities related to quality assurance are as follows.

1. Technology meetings with vendors.
2. Approval and guidance of vendors.
3. Analysis and test of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

Table 1 Quality Control Check Points of Parts and Material (example)

Meterial parts	Important control items	Check points
Water	Appearance	Damage and contamination on surface
	Dimension	Flatness
	Sheet resistance	Resistance
	Defect density	Defect numbers
	Crystal axis	
Mask	Appearance	Defect numbers, scratches
	Dimension	Dimension level
	Resistoration	
	Gradation	Uniformity of gradation
Fine wire for wire bonding	Appearance	Contamination, scratches, bend, twist
	Dimension	
	Purity	Purity level
	Elongation ratio	Mechanical strength
Frame	Appearance	Contamination, scratches
	Dimension	Dimension level
	Processing accuracy	
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
Ceramic package	Appearance	Contamination, scratches
	Dimension	Dimension level
	Leakage resistance	Airtightness
	Plating	Bondability, solderability
	Mounting characteristics	Heat resistance
	Electrical characteristics	
	Mechanical strength	Mechnical strength
Plastic	Composition	Characteristics of plastic material
	Electrical charactristics	
	Thermal characteristics	
	Molding performance	Molding performance
	Mounting characteristics	Mounting characteristics

3.3.2 Process Quality Control

Control of process quality is extremely significant in the overall process of device quality assurance. Quality control functions at every stage of production are described below. Figure 3 lists specific process quality control factors.

1. Quality control of products in every stage of production
   Potential device failure factors should be removed as soon as possible in the manufacturing process. To do this, check points are set up within each process so as not to move products exhibiting failure factors on to any following process. Especially for devices designed for high reliability, manufacturing lines are rigidly monitored to control process quality. Additionally, we perform very stringent checks on some processes and/or lots, and even 100% inspections in certain critical processes to remove potentially failing items related to unavoidable manufacturing variances. Screening based on high temperature aging or temperature cycling are also part of quality assurance procedures. Controlling quality during processing includes these items:

   a. Control of conditions of equipment and workers
   b. Sampling test of uncompleted products
   c. Proposal and implementation of improvements in working conditions
   d. Continuous worker education
   e. Maintenance and improvement of yields
   f. Identification of quality problems, and implementation of countermeasures to eliminate them
   g. Communication of quality-related information

2. Quality control of manufacturing facilities and measuring equipment
   Manufacturing facilities have been developed to answer the need for higher device performance and automated production. It is also important to define and accurately measure quality and reliability.

   At Hitachi, automated manufacturing is used to reduce manufacturing variances. The operation of high performance equipment requires automated control to function properly.

   Maintenance inspections are carried out daily to ensure proper quality control, and in some instances at other more frequent intervals according to specifications, at every check point.

   The adjustment and maintenance of measuring equipment is done according to specifications and past experience, and is vigorously monitored to maintain and improve the quality of our products.

3. Quality control of the manufacturing environment and submaterial
   Final quality and reliability of devices are especially affected by manufacturing processes. We therefore thoroughly control factors of the manufacturing environment, such as gases or pure water.

   Dust control is critical to achieve higher integration and higher device reliability. To maintain and improve the cleanliness of the manufacturing site, we take great care to keep buildings, facilities, air-conditioning systems, materials, clothes, and all possible elements associated with production as clean and dust-free as we can. We extend this effort to periodically check the ambient air in the manufacturing facility for floating dust, and we check for any minute amounts which might have accumulated on the floor, other surfaces, or on any equipment.

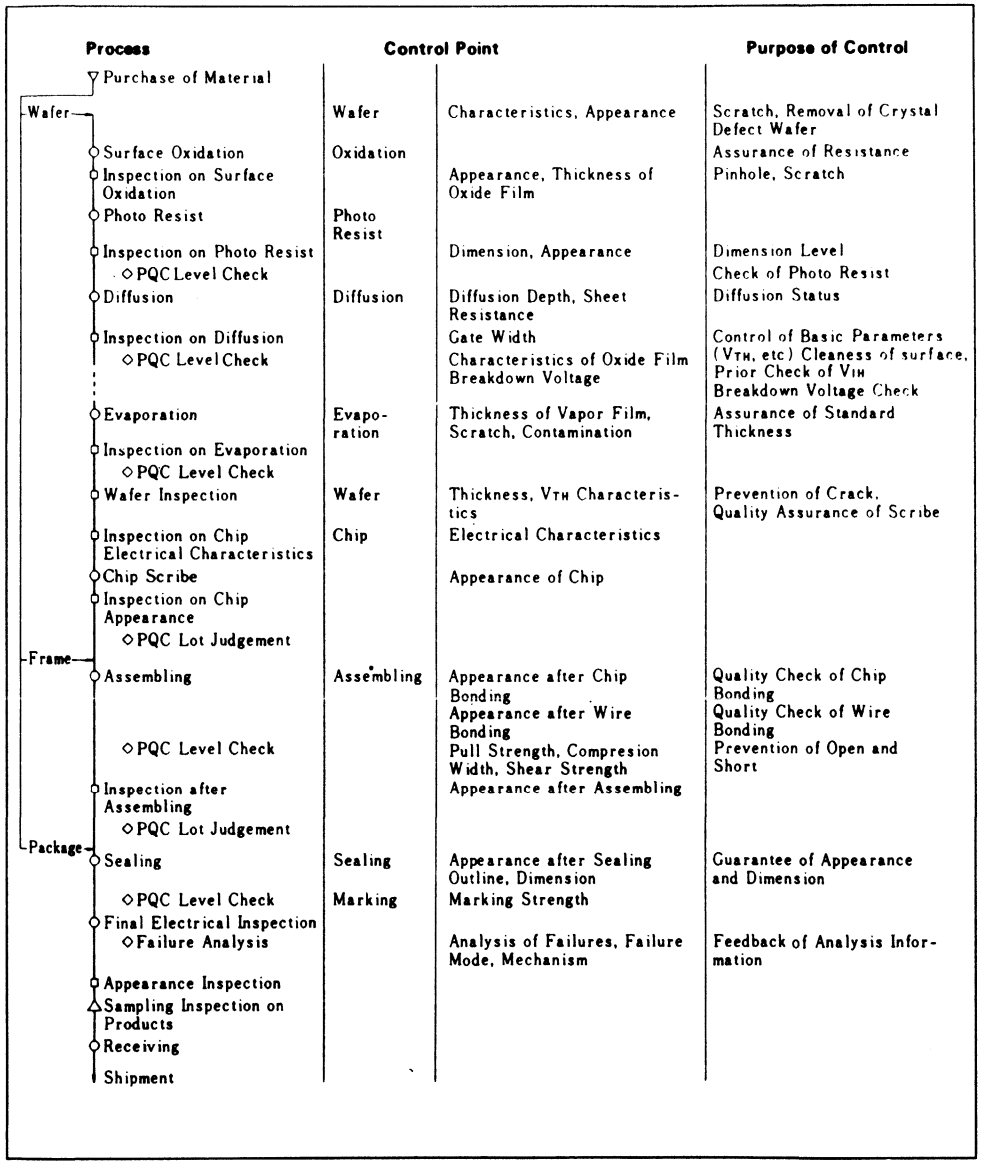


Figure 3 Example of Process Quality Control Factors

3.3.3 Final Tests and Reliability Assurance Tests

1. Final tests
   Lot inspection is done by the quality assurance department for products already passed in 100% testing during the manufacturing process. Although 100% performance is expected, sample lot inspection is also carried out to prevent any possible accidental mixture of failed products with regular, satisfactory devices.
   The extra lot inspection not only confirms that all products meet all user requirements, but considers any other potential factors. Our lot inspection is based on MIL-STD-105D.

2. Reliability assurance tests
   To assure reliability, appropriate tests are performed periodically on each manufacturing lot if the user requires such a high level of examination.

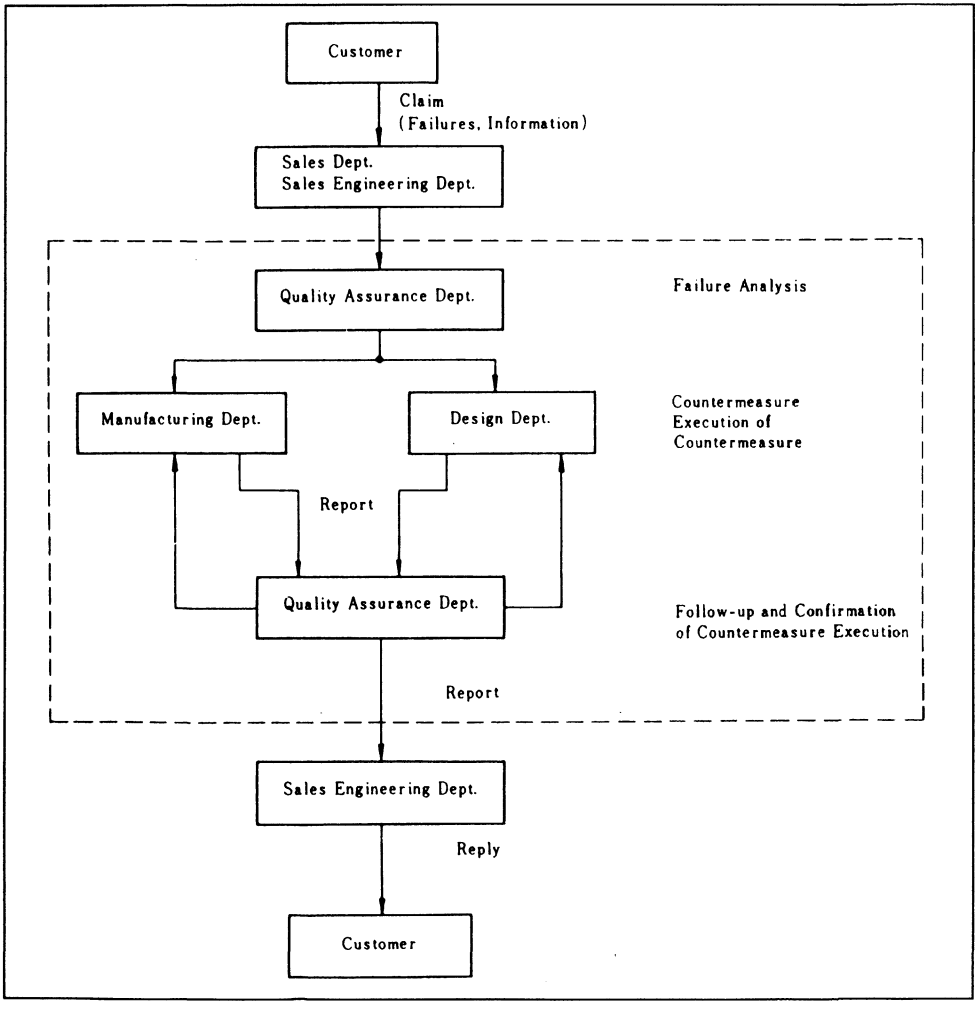


Figure 4 Process Flowchart for Customer-Reported Failure

1. Inspection Method

In memory IC inspection, the quality cannot be judged solely by a dc test on the external pins. The number of elements such as transistors which can be judged in a dc test is very small parts of all elements. The proposed address patterns listed below inspect whether internal circuits are functioning correctly.

1. All low, all high
2. Checker flag
3. Stripe pattern
4. Marching pattern
5. Galloping
6. Walking
7. Ping-pong

These are only a few representative samples of the testing options. There are also patterns to check the mutual interference of bits and the maximum power dissipation. Among the listing, 1 through 4 are called N patterns, which can check one sequence of N-bit IC memory with several consecutive cycles of N patterns. 5 through 7 are called N^2 patterns, which need several cycles of N^2 patterns to check one sequence of N-bit IC memory. Serious problems arise using N^2 patterns in large-capacity memory. For example, the inspection of 1-Mbit memory with the galloping pattern takes considerable time—about 120 houres. 1, 2, and 3 are rather simple and effective methods, but these patterns will not find all the failures in decoder circuits. Marching is the most simple and powerful pattern to check the functions of IC memories.

2. Marching Pattern

The marching pattern, as its name indicates, is a pattern in which 1s sequentially replace 0s throughout the device. The 1s "march" into all bits of 0. For example, a simple addressing of 16-bit memory is described below.

1. Clear all bits (see Figure 1 a).
2. Read 0 from the 0th address and check that read data is 0. Hereafter, to read means "checking and judging data."
3. Write 1 on the 0th address (see Figure 1 b).
4. Read 0 from the 1st address.
5. Write 1 on the 1st address.

   .
   .
   .
6. Read 0 from the nth address.
7. Write 1 on the nth address (see Figure 1 c).
8. Repeat 6 and 7 to the last address. Finally all data will be 1.
9. After all data has become 1, repeat from 2 through 8 replacing 0 with 1.

In this method, 5N address patterns are necessary for the N-bit memory.

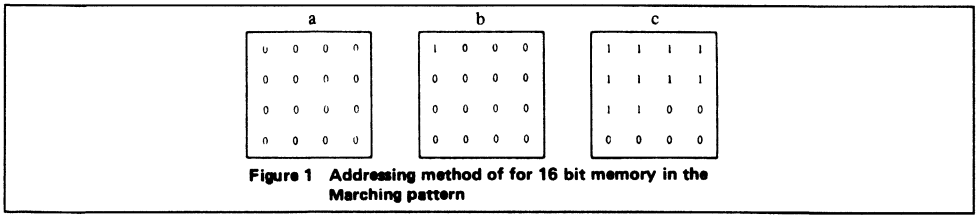


Figure 1 Addressing method of for 16 bit memory in the Marching pattern

Figure 1 Addressing Method of 16-Bit Memory in the Marching Pattern

Application

1. Static RAM

1.1 Static RAM Memory Cell

The static RAM memory cell consists of flip-flops organized as 4 NMOS transistors and 2 load resistors as shown in Figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

1.2 Data Retention Mode and Battery Backup System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. This enables a battery backup system to retain the data during power failure.

Data Retention Mode: The important point in designing a battery backup system is the timing relationship between the memory power supply and the chip select signal during a change from the ordinal power source and battery power. If proper timing for the change is missed, memory data might be destroyed.

Figure 1-2 shows the timing for switching the power supply. The definitions for the technical terms related to the data retention mode are as follows.

Data retention mode: The period during which the supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS}$ = V_{DR} – 0.2 V).

t_{CDR} (time from chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (operation recovery time): The minimum time needed to change from data retention mode to operating mode.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally the minimum supply voltage needed to retain memory data is 2 V.

I_{CCDR} (data retention current): The current consumption in the data retention mode depends on the memory power supply voltage and ambient temperature. It is specified as supply voltage, V_{DR} = 3.0 V.

Battery Backup System: The sequence of activities required to switch to battery backup is as follows.

1. External circuit detects a failure in the system power supply.

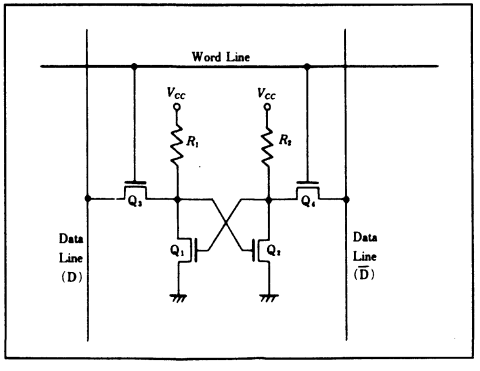


Figure 1-1 Static RAM Memory Cell

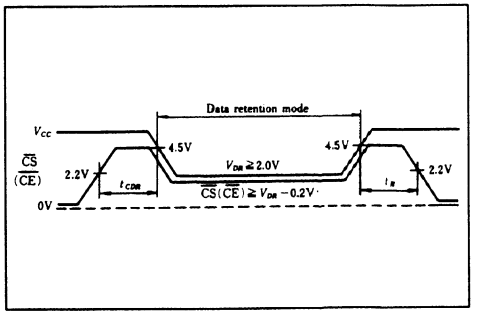


Figure 1-2 Timing for Battery Backup Application

2. External circuit switches the RAM to standby mode.
3. External circuit separates the RAM from the system power supply.
4. External circuit switches to the backup power supply.

The control circuit detects the power failure and disconnects the power source after switching memory to the standby mode. On recovery, it confirms the power supply availability and, after some delay, returns memory to the operating mode. Memory control signals depend on the types of memory used in the system.

1. Using memory with only one $\overline{CS}$:
   The NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. Since the level of $\overline{CS}$ in the data retention mode must be higher than V_{DR} – 0.2 V, the power supply for this NAND gate must either be shared with the memory power supply or be pulled up to the memory power supply.
2. Using memory with two $\overline{CS}$:
   Basically, the signals are the same as above. In general use, two pins should be used for the control signal and the chip select signal, respectively. When the $\overline{CS}$ intercepts the current path of other pins in the input buffers, it is used as control signal input for the data retention mode.
3. Using memory with $\overline{CS}$ and CS:
   As CS selects the chips at high level, it is preferable to use CS than $\overline{CS}$ as a control signal input for the data retention mode. As soon as power down is detected, the signals should be brought low. Therefore, a pull-up to the memory power supply level is not needed, thus simplifying the circuit organization.

Figure 1-4 shows an example of a battery backup system circuit. Hitachi recommends using CMOS logic for gate G1 in a control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch the regulating circuit from system power supply to backup power supply.

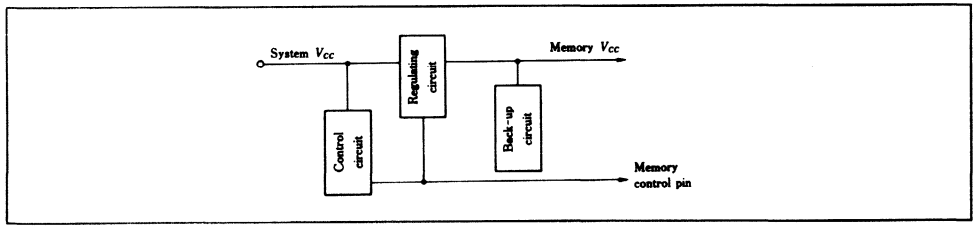


Figure 1-3 Example of Battery Backup System

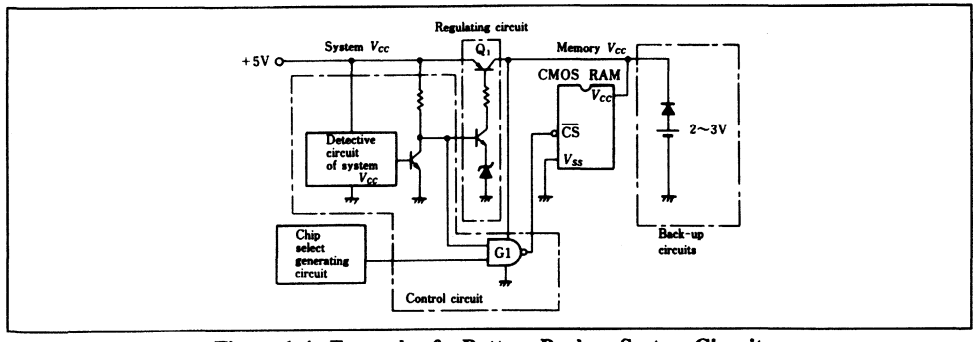


Figure 1-4 Example of a Battery Backup System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

A new type of memory, pseudo-static RAM, has been developed that provides the advantages of dynamic RAM (low cost, high density), and static RAM (easy usage). IC memory consists of memory cells for data storage, and input/output circuits for interfacing to the external circuits. PSRAM provides the memory cell and peripheral circuits of DRAM and the external control circuits, which includes a part of the refresh control circuits not provided by dynamic RAM, and interface circuits similar to those of static RAM, on a single chip as shown in Table 2-1. The address input is not multiplexed, and data input/output is byte-wide like the standard static RAM. With PSRAM × 8 organization, a medium density memory system can be easily designed. PSRAM provides address refresh, automatic refresh, and self-refresh, which simplifies the support circuit requirements. Using PSRAM, the circuits interfacing the CPU to DRAM can be drastically reduced. Figure 2-1 shows examples of system design using PSRAM and DRAM. Figure 2-2 shows a block diagram of the pseudo static RAM.

2.2 1-Mbit Pseudo-Static RAM Function

Read/Write Cycle: Figures 2-3 and 2-4 show the timing chart for the read/write cycle of the 1-Mbit pseudo-static RAM HM658128A. The HM658128A can perform two types of access in a read cycle, $\overline{CE}$ access (Figure 2-3 a) and $\overline{OE}$ access (Figure 2-3 b). It writes the data at the rising edge of $\overline{WE}$ (Figure 2-4 a) or at the rising edge of $\overline{CE}$ (Figure 2- 4 b). The $\overline{CS}$ pin should be brought high when the address is latched at the falling edge of $\overline{CE}$ in the read/write cycle. The HM658128A has no $\overline{OE}$ specification at the falling edge of $\overline{CE}$ as it provides both the $\overline{OE}$ pin and the $\overline{RFSH}$ pin.

Table 2-1 PSRAM Features

	SRAM	PSRAM	DRAM
Memory cell	4 Tr + 2 R	1 Tr + 1 C	1 Tr + 1 C
Address	Single address	Single address	Multiplexed address
Refresh	Not necessary	Necessary	Necessary
External circuits	Simple ◄——————►		Complex

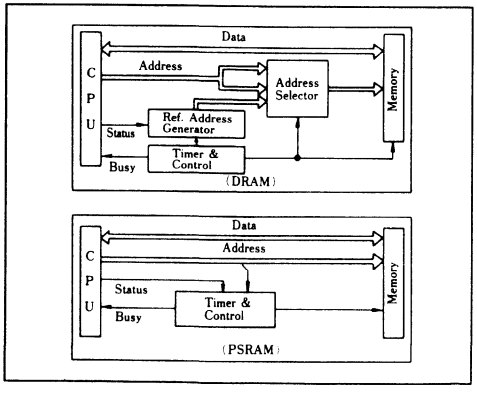


Figure 2-1 System Organization

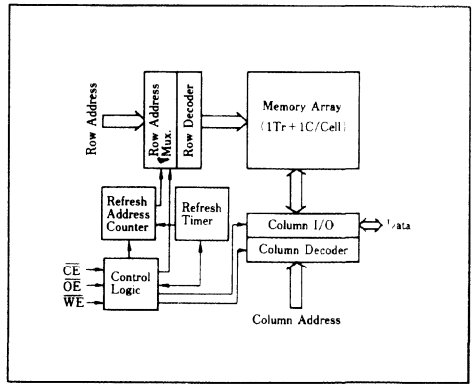


Figure 2-2 Block Diagram (PSRAM)

CS Standby Mode: The HM658128A enters the CS standby mode for one cycle if CS goes low at the falling edge of $\overline{CE}$ (Figure 2-5).

Address Refresh: Address refresh mode performs refresh by access to row address (A0–A8) 0–511 sequentially within 8 ms as shown in Figure 2-6 (in the distributed mode). In this mode, CS should be high at the falling edge of $\overline{CE}$.

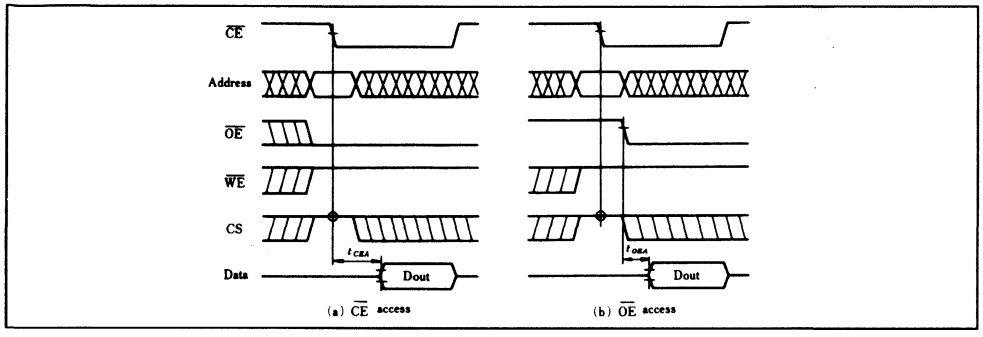


Figure 2-3 Read Cycle

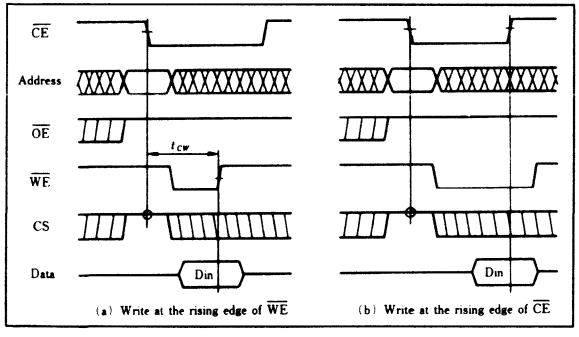


Figure 2-4 Write Cycle

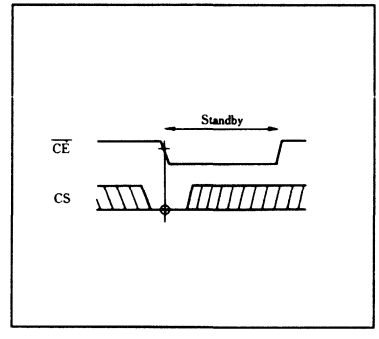


Figure 2-5 CS Standby Mode

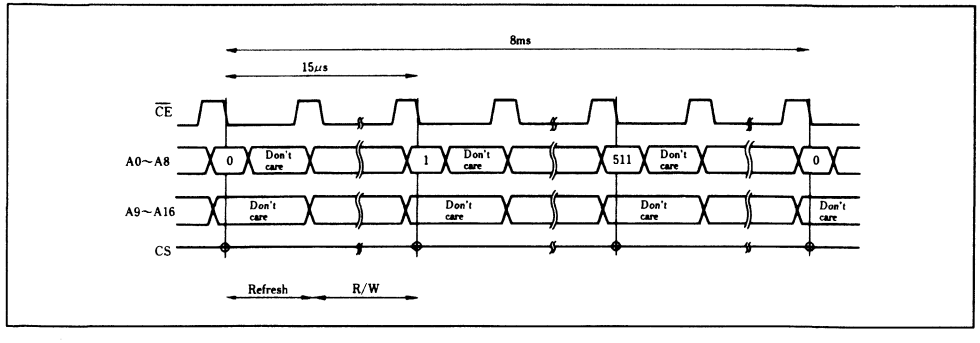


Figure 2-6 Address Refresh

Application

Automatic Refresh: The HM658128A goes to automatic refresh mode, while $\overline{CE}$ is high, if $\overline{RFSH}$ falls and is kept low for more than t_{FAP}.

It is not required to input the refresh address from address pins A0–A8, as it is generated internally. Figure 2-7 shows the timing chart for distributed refresh. In the automatic refresh mode, the timing for only $\overline{CE}$ and $\overline{RFSH}$ are specified.

Self-Refresh: Self-refresh mode performs refresh at an internally determined interval. The HM658128A enters this mode when the internal refresh timer is enabled by keeping $\overline{CE}$ high and $\overline{RFSH}$ low for more than 8 µs (Figure 2-8).

Considerations for Using the HM658128A: The following should be considered when using the HM658128A.

- Data retention:
  The HM658128A can retain data on battery power. The HM658128AL, a low power version, offers a typical self-refresh or standby current of 100 µA.
  A 1-Mbyte system (using eight HM658128Ls) can retain the data for about 1.5 months with a battery supplying 1000 mAh current. V_{CC} = 5 V ±10% must be maintained for data retention.

- Power on:
  Start HM658128A operation by executing more than eight initial cycles (dummy cycles) for more than 100 µs after the power voltage reaches 4.5 to 5.5 V following power on.

- Bypass capacitor:
  Hitachi recommends inserting one bypass capacitor per RAM device.

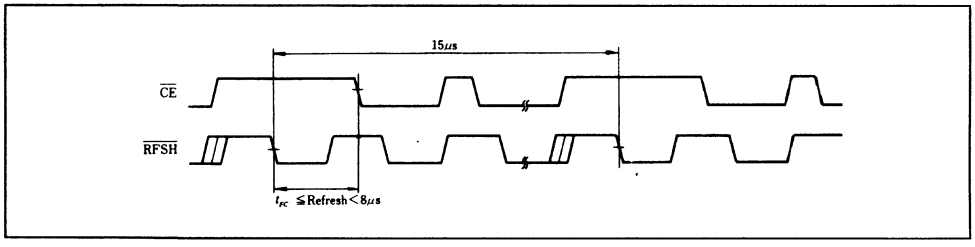


Figure 2-7 Automatic Refresh

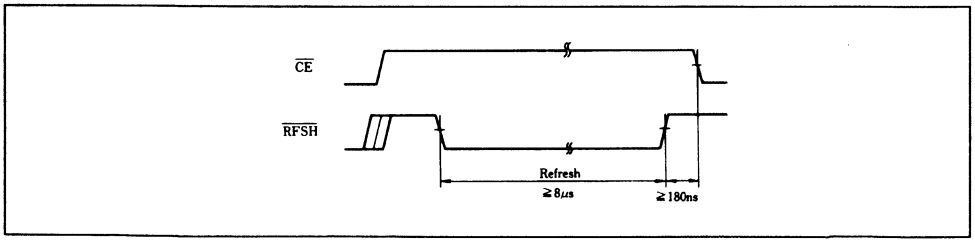


Figure 2-8 Self-Refresh

2.3 Pseudo-Static RAM Data Retention

PSRAM with self-refresh retains data when $\overline{CE}$ and $\overline{OE}$ are fixed for more than a defined period.

PSRAM cannot retain data at low supply voltages.

PSRAM uses a MOS-type memory cell as shown in Figure 2-9. The charge is stored on the capacitor C as memory data. The high data, written at low supply voltage, cannot be read as 1 at high supply voltages.

Figure 2-10 indicates the operation voltage for self-refresh and subsequent read of PSRAM. If the data is read out at more than 5 V of V_{CC}, for example, after self-refresh is performed at V_{CC} = 3.7 V, it will be destroyed.

PSRAM must be used at supply voltages from 4.5 V to 5.5 V.

The self-refresh current increases at low supply voltages.

PSRAM provides a voltage level detector circuit to reduce self-refresh current. However, it should be noted that the circuit increases the current with a low supply voltage during self-refresh (Figure 2-11). The self-refresh current also increases at low temperatures (Figure 2-12).

PSRAM should be used within the recommended operation range (V_{CC}, more than 4.5 V, temperature more than 0°C) for data retention, especially when using a battery.

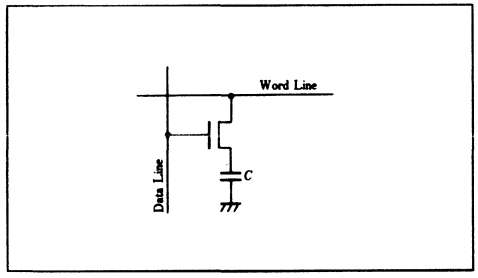


Figure 2-9 A Memory Cell of PSRAM

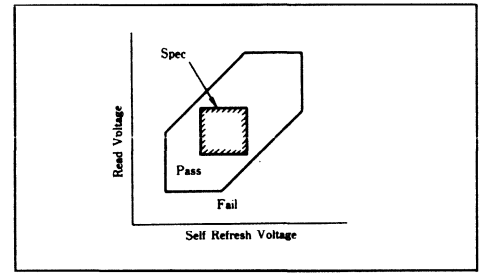


Figure 2-10 PSRAM Operating Voltage

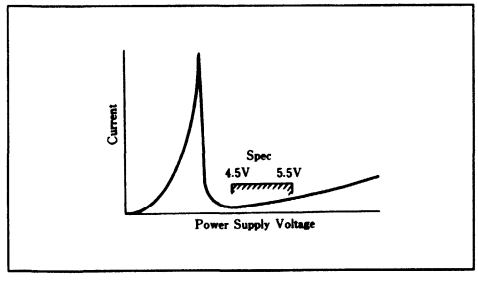


Figure 2-11 Self-Refresh Current vs Voltage

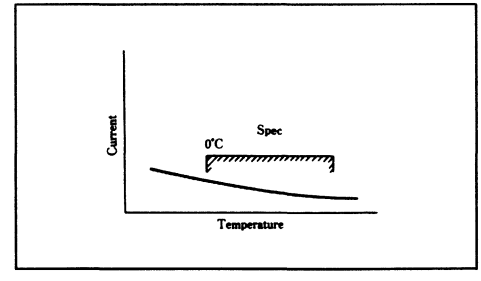


Figure 2-12 Self-Refresh Current vs Temperature

3. Specific Memories for Graphic/ Video Applications

3.1 Multiport Video RAM

Figure 3-1 shows the general concept of video RAM. A multiport video RAM provides an internal data register (SAM) with memory (RAM). Both can be accessed asynchronously. Effective graphic display memory can be developed by using the random port of the RAM component for graphic processor drawing, and the serial port of the SAM component for CRT display.

Figure 3-2 shows the block diagram of the 256-k/1-Mbit multiport video RAM HM53461/ HM534251, and Table 3-1 shows the operation modes of the HM53461/HM534251.

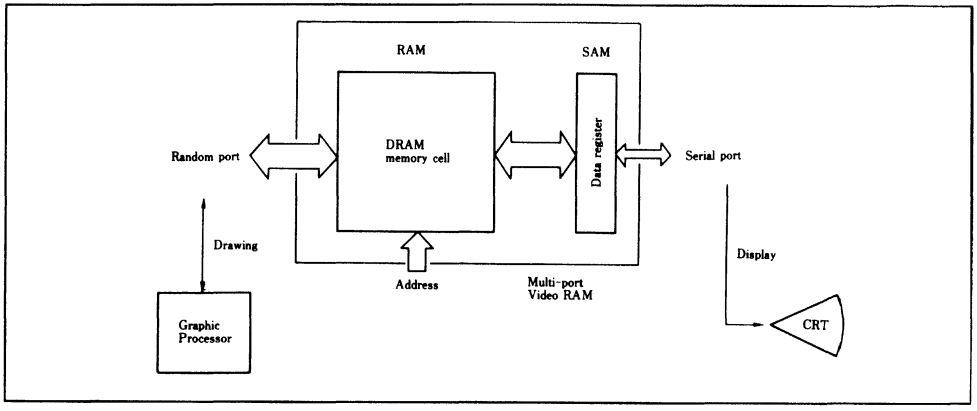


Figure 3-1 A General Concept of Multiport Video RAM

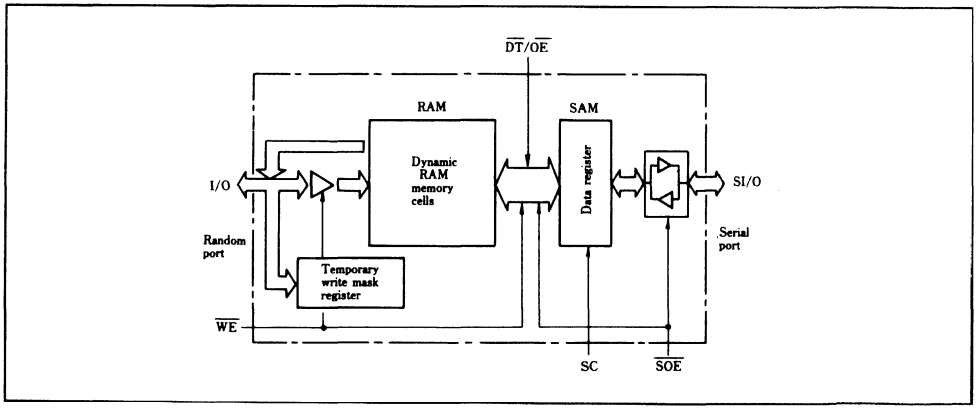


Figure 3-2 Block Diagram of HM53461/HM534251

The operation modes shown in Table 3-1 are described as follows.

Read/Write Operation: Read/write is performed on the random port in the same sequence as a dynamic RAM (Figure 3-3). The HM53461/HM534251 starts the read operation with $\overline{WE}$ high and the write operation at the falling edge of $\overline{WE}$.

Temporary Write Mask Set and Temporary Masked Write Operation: The HM53461/HM534251provides a temporary masked write operation which inhibits writing data bit-by-bit (write mask) during one $\overline{RAS}$ cycle. The temporary write mask set function defines the bits to be inhibited (Figure 3-4). This operation puts the data on I/O1–I/O4 into the internal temporary write mask register. When 0 is programmed to the register, writing to the corresponding bit is inhibited.

The temporary write mask register is reset at the rising edge of $\overline{RAS}$.

Table 3-1 Operation Modes of HM53461/HM534251

At the Falling Edge of $\overline{RAS}$					SAM Modes	
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SOE}/\overline{SE}$	RAM Modes	SI/O direction	Notes
H	H	H	X	Read/write	S_{in}/S_{out}	1, 2, 3
H	H	L	X	Temporary write mask data program	S_{in}/S_{out}	1, 2, 3
H	L	H	X	Read transfer	S_{out}	2
H	L	L	L	Write transfer	S_{in}	
H	L	L	H	Pseudo transfer	S_{in}	
L	X	X	X	CBR refresh	S_{in}/S_{out}	1, 2

H: High, L: Low, X: Don't care

Notes:

1. The transfer cycle executed previously defines SI/O direction.
2. SI/O is in a high impedance state with $\overline{SOE}$ high, even if the direction is S_{out}.
3. The HM53461/HM534251 starts write operation if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of $\overline{RAS}$.

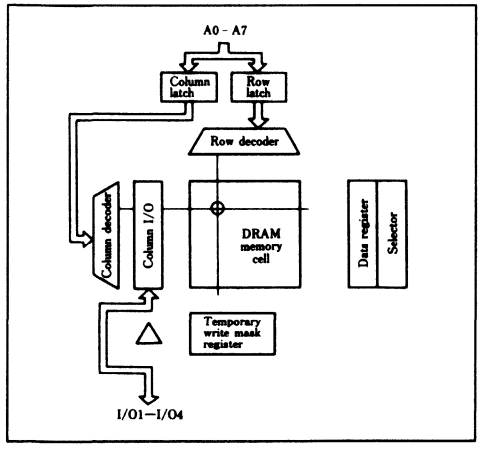


Figure 3-3 Read/Write Operation

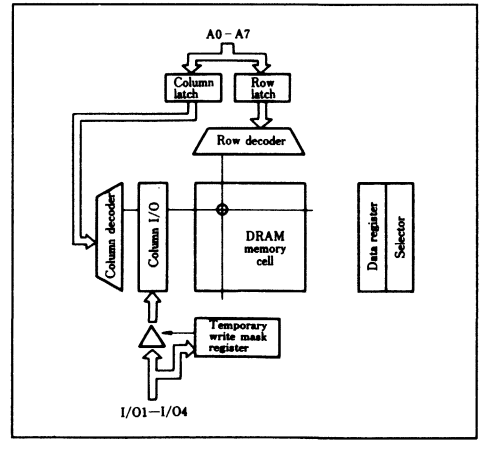


Figure 3-4 Temporary Masked Write Operation

Read Transfer Operation: In this cycle, the HM53461/HM534251 transfers the data of one row in RAM (1024 bits), at the address specified by the falling edge of $\overline{RAS}$, to SAM (Figure 3-5). The start address in SAM can be programmed at the falling edge of $\overline{CAS}$ in this cycle. After data transfer, the serial port is set to the serial read mode at the rising edge of $\overline{DT/OE}$.

Write Transfer Operation: In this cycle, the HM53461/HM534251 transfers the data in the SAM data register (1024 bits) to one row in RAM, at the address specified by the falling edge of $\overline{RAS}$ (Figure 3-6). The start address in SAM can be programmed in this cycle. After data transfer, the serial port is set to serial write mode.

Pseudo Transfer Operation: This operation switches the serial port to serial write mode (Figure 3-7). It does not perform data transfer between RAM and SAM. The SAM start address can be programmed in this cycle.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Operation: The HM53461/HM534251 performs refresh by using the internal address counter in this operation (Figure 3-8).

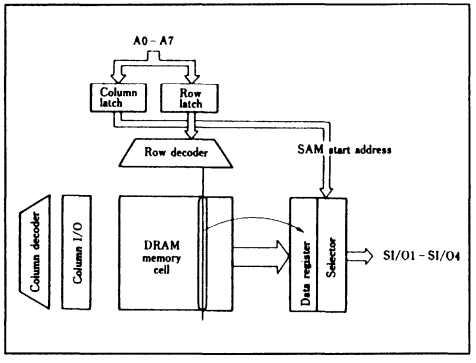


Figure 3-5 Read Transfer Operation

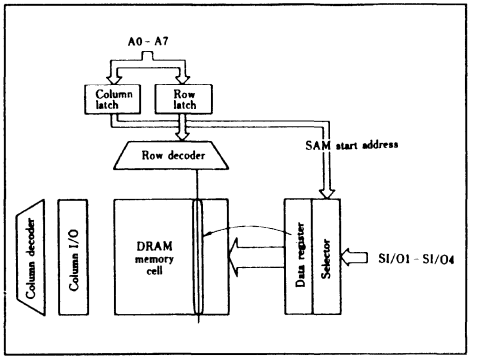


Figure 3-6 Write Transfer Operation

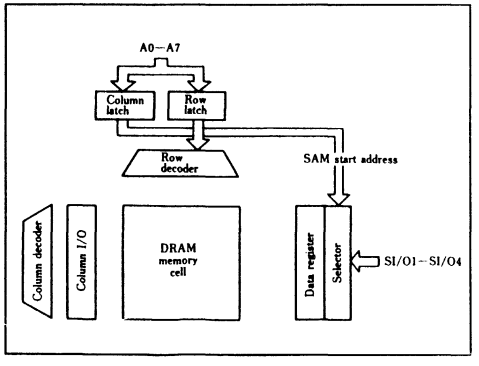


Figure 3-7 Pseudo Transfer Operation

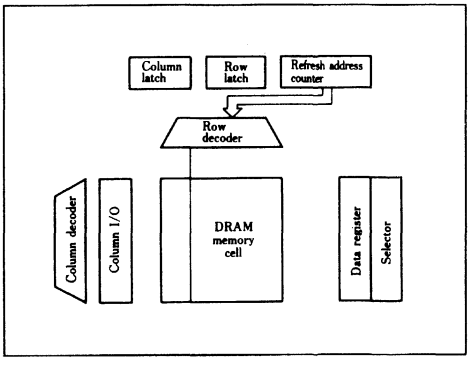


Figure 3-8 $\overline{CAS}$-Before-$\overline{RAS}$ Refresh

Serial Read/Write Operation: The HM53461/HM534251 reads/writes the contents of the SAM data register in serial mode at the rising edge of SC (serial clock input) (Figure 3-9). The address for serial access is generated by the internal address pointer, independent of the random port operation. It should be considered that serial access is restricted in transfer cycles. The SAM, employing static-type data registers, requires no refresh.

The HM53462/HM534252 is a multiport video RAM with logic operation capabilities advantageous in the HM53461/HM534251.

Figure 3-10 shows the block diagram of the HM53462/HM534252. Table 3-2 describes the operation modes.

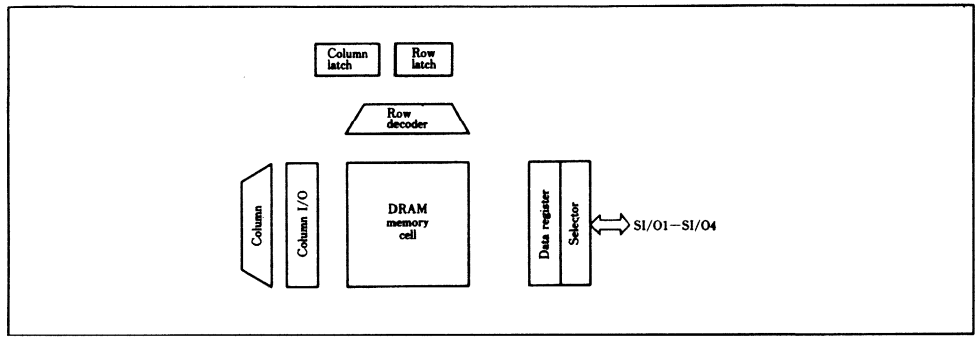


Figure 3-9 Serial Read/Write Operation

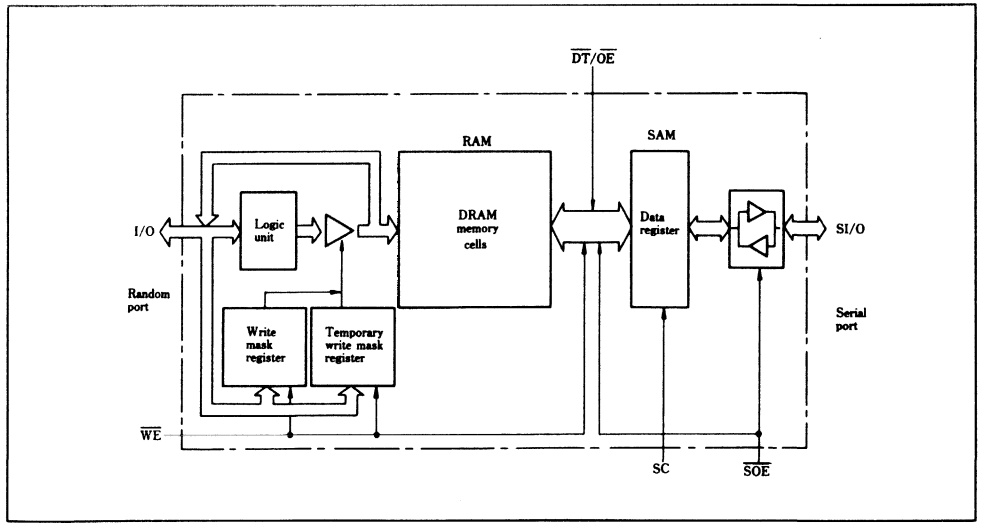


Figure 3-10 Block Diagram of HM53462/HM534252

Logic Operation Programming: This function programs a logic operation (Figure 3-11). The logic operation is available until the device is reprogrammed or reset. In the logic operation mode, the HM53462/HM534252 performs read-modify-write internally when data is written into the random port. The result of the logic operation between memory data and written data is placed into the address from which the memory data is transferred.

In the logic operation programming cycle, the mask register, which differs from the temporary mask register, is also programmed. It is available until reprogrammed.

Notes: Notes on using HM53461/HM534251/ HM53462/HM534252 are as follows.

- Dummy $\overline{RAS}$ cycle
  Devices should be initialized by eight dummy $\overline{RAS}$ cycles (minimum) before accessing the random port. The refresh cycle can be inserted for initialization. It is recommended that the system be initialized by a dummy $\overline{RAS}$ cycle in the automatic reset time of the processor.

- Bypass capacitor
  One bypass capacitor should be inserted between V_{CC} and V_{SS} to each device. The V_{CC} pin should be connected to the capacitor by the shortest path. A capacitor of several μF is suitable.

- Negative voltage input
  A negative polarity input level to an input pin or I/O pin should be above –1 V. In this range, it has no effect on the device characteristics or RAM/SAM data retention.

- Initialization of logic operation mode (HM53462/HM534252)
  The logic operation programming cycle should be executed before accessing the random port to initialize the logic operation mode after power on. At this time, the operation codes (0101) and all 1 write mask data are recommended.

Table 3-2 Operation Modes of HM53462/HM534252

At the Falling Edge of $\overline{RAS}$					SAM Modes	
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SOE}/\overline{SE}$	RAM Modes	SI/O Direction	Notes
H	H	H	X	Read/write	S_{in}/S_{out}	1, 2, 3
H	H	L	X	Temporary masked write	S_{in}/S_{out}	1, 2, 3
H	L	H	X	Read transfer	S_{out}	2
H	L	L	L	Write transfer	S_{in}	
H	L	L	H	Pseudo transfer	S_{in}	
L	X	X	X	$\overline{CAS}$-before-$\overline{RAS}$ refresh	S_{in}/S_{out}	1, 2
L	X	L	X	Logic operation program (CBR Refresh)	S_{in}/S_{out}	1, 2

H: High, L: Low X: Don't care

Notes:

1. The transfer cycle previously executed defines SI/O direction.
2. SI/O is in high impedance with $\overline{SOE}$ high, even if the direction is S_{out}.
3. The HM53462/HM534252 writes if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of $\overline{RAS}$.

3.2 Line Memory

Hitachi has produced a line memory for video line buffers with simple circuits providing specific functions as described below.

The line buffer can improve picture quality by storing one horizontal line of data. It has the following features.

- Capacity to store one horizontal line data.
- High speed operation matching the sampling speed of PAL TV signal (4 f_{sc}/8 f_{sc}) or NTSC TV signal (4 f_{sc}/8 f_{sc}).
- Separate data inputs/outputs and capability of serial data inputs and outputs.

The conventional line buffer, composed of high speed static RAM, requires separate input/output capabilities for a double buffered organization. It also requires interleaving for high speed operation, matching 4 f_{sc}/8 f_{SC}, where f_{SC} is the subcarrier frequency. In addition, external circuits are needed for serial address scan.

The line memory provides all of these functions. Figure 3-12 shows the standard organization of a conventional memory buffer, and Figure 3-13 shows the block diagram of line memory.

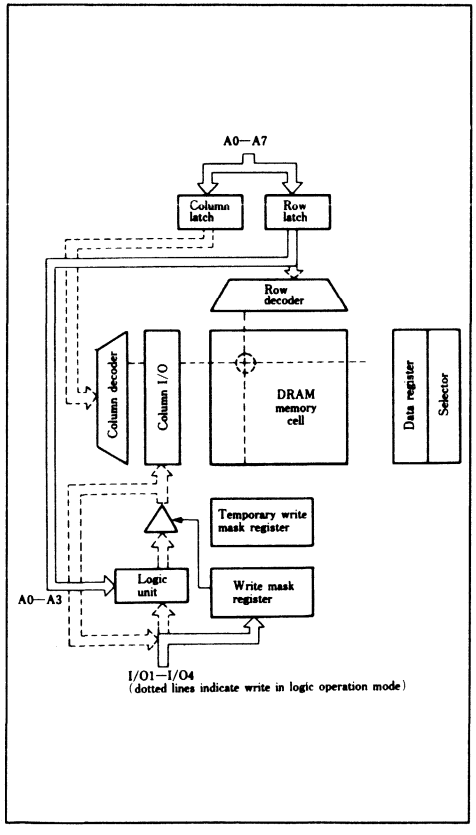


Figure 3-11 Logic Operation Programming

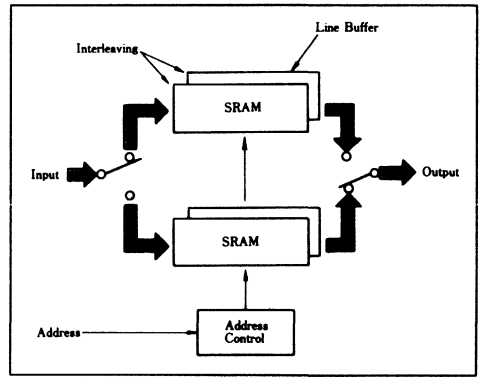


Figure 3-12 Standard Organization of Conventional Line Buffer

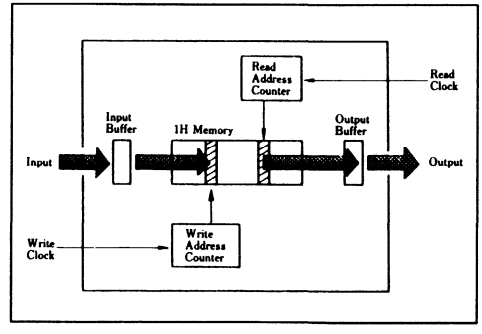


Figure 3-13 Block Diagram of Line Memory

Application

The Hitachi HM63021 is a 2048 word × 8-bit line memory storing two horizontal lines of data.

It has five different modes for various video graphic system applications. It realizes high speed operations for PAL and NTSC TV signals, and dissipates little power, employing 1.3 μm CMOS technology and static-type memory cells.

The features of the HM63021 are described as follows.

- Five modes for various video graphic system applications
  - — Delay line mode
  - — Alternate 1H/2H delay mode
  - — TBC (Time-Base Corrector) mode
  - — Double speed conversion mode
  - — Time-base compression/expansion mode
- High speed cycle time
  - — HM63021-45: 45 ns min
  - — HM63021-34: 34 ns min (corresponds to 8 f_{SC} of NTSC TV signal)
  - — HM63021-28: 28 ns min (corresponds to 8 f_{SC} of PAL TV signal)

The line memory in a system using digital signal processing technologies offers the following features.

- — Comb filter
- — Double-speed conversion (non-interlace)
- — Compression/expansion of graphics (picture-in-picture)
- — Dropout canceller
- — Time-base corrector
- — Noise reducer

4. Dynamic RAM (4-Mbit DRAM)

4.1 Dynamic RAM Memory Cell

The dynamic RAM memory cell consists of 1 MOS transistor and 1 capacitor, as shown in Figure 4-1. It detects the data in the cell (1 or 0) by the charge stored in the capacitor. Dynamic RAM offers a higher density than static RAM because it uses fewer components per chip.

However, dynamic RAM data must be rewritten (this is called refresh) in a defined cycle, because the charge stored in the capacitor leaks.

4.2 Power On Procedure

After turning on the power to set the internal memory circuitry, delay for more than 100 µs, then apply eight or more dummy cycles before operation. The dummy cycle must be either $\overline{\text{RAS}}$-only refresh or $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. When using an internal refresh counter, eight or more $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles are required as dummy cycles.

4.3 Address Multiplexing

Dynamic RAM devices are used to increase capacity because of their smaller cell area. In using dynamic RAM in systems, however, it is desirable to increase memory density by using even smaller packages. To reduce the number of pins and the package size, address multiplexing is used.

Using a 4-Mbit dynamic RAM, 22 address signals are necessary to select one of 4,194,304 memory cells. Address multiplexing allows address signals to be applied to each address pin. Thus only 11 address input pins are required to select one of 4,194,304 addresses. The multiplexed address inputs are latched as follows: $\overline{\text{RAS}}$ (row address strobe) selects one word line according to the row address signal, and one column decoder is selected by $\overline{\text{CAS}}$ (column address strobe) following a column address signal. Although two extra signals, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$, are required, the number of address pins is reduced to half. Figure 4-2 shows the pin arrangement, address latch waveform, and the block diagram of address-multiplexed 4-Mbit dynamic RAM. Systems require an address multiplexer in order to latch the multiplexed address signals into the device.

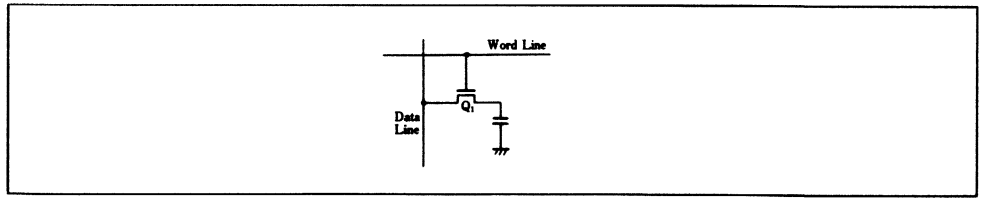
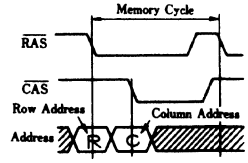


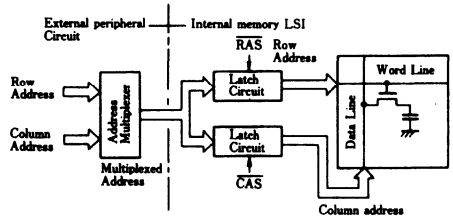
Figure 4-1 Memory Cell of Dynamic RAM

A_0 to A_{10}	Address input
$\overline{CAS}$	Column address strobe
D_{in}	Data in
D_{out}	Data out
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/write input
V_{CC}	Power (+5 V)
V_{SS}	Ground
A_0 to A_9	Refresh address inputs

(a) Pin Arrangement



(b) Address Latch



(c) Block diagram of Address Multiplexing

Figure 4-2 Address Multiplexing of Dynamic RAMs

4.4 Dynamic RAM Function

Figure 4-3 shows the normal function of the dynamic RAM.

Read Cycle: In the read cycle, a row address is latched at the falling edge of $\overline{RAS}$, and a column address is latched at the falling edge of $\overline{CAS}$ after the $\overline{RAS}$ falling edge. If $\overline{WE}$ is high, the data is read out from D_{out} with the access time of t_{CAC} (access time from $\overline{CAS}$) or t_{RAC} (access time from $\overline{RAS}$).

The t_{RCD} maximum ($\overline{RAS}$ to $\overline{CAS}$ delay time) is specified only to guarantee the specified minimum values of other timings such as the cycle time, $\overline{RAS}/\overline{CAS}$ pulse width. Therefore, when using these timings with more than the specified minimum value, there is no need to limit the t_{RCD} to the specified maximum value.

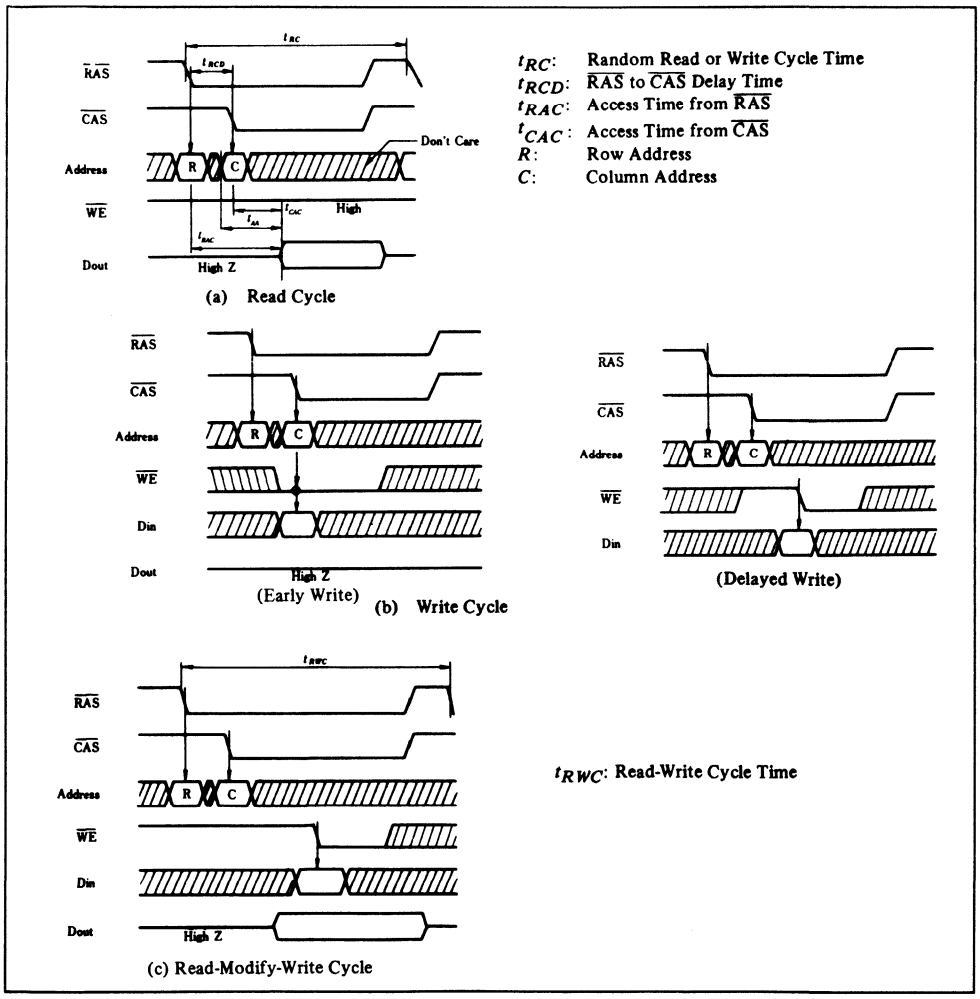


Figure 4-3 Normal Function of Dynamic RAM

Write Cycle: The dynamic RAM provides two write cycle modes: early write cycle and delayed write cycle. In the early write cycle, when $\overline{WE}$ is low, data is written into D_{in} at the falling edge of $\overline{CAS}$. In the delayed write cycle, data is written into D_{in} at the falling edge of $\overline{WE}$ after $\overline{CAS}$ falls.

Read-Modify-Write Cycle: The read-modify-write cycle is initiated by setting $\overline{WE}$ high. Data is read out from D_{out} at the falling edge of $\overline{CAS}$ with $\overline{WE}$ high. Then, if $\overline{WE}$ goes low, data is written into the same address from D_{in} in the same cycle.

The cycle time in the read-modify-write mode (t_{RWC}) is longer than the cycle time in read/write mode (t_{RC}).

4.5 High Speed Access Mode

The dynamic RAM access time is typically longer than that of static RAMs. To realize a higher speed operation, high speed access modes are implemented. The read operation in the dynamic RAM is performed as follows:

When a word line is selected by the row address, all data in the memory cells connected to the selected word line are transferred to sense amplifiers. One of these sense amplifiers is then selected by the column address, and its contents are output.

Data output from other sense amplifiers are controlled only by the column address.

Access controlled only by the column address, with the row address fixed, is called the high speed access mode. Table 4-1 compares each mode.

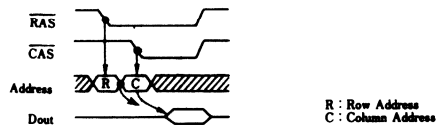
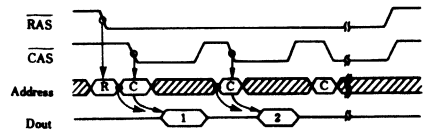
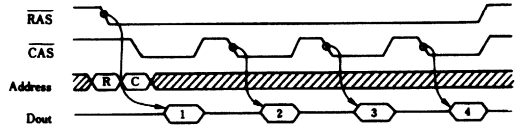
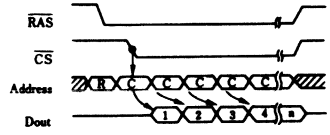
Fast Page Mode: This is the most typical access mode in dynamic RAM. The column address is switched synchronously with the $\overline{CAS}$ rising edge.

Nibble Mode: In a nibble mode dynamic RAM, data from four sequential addresses is stored in the 4-bit output latch circuits. The output is provided by the $\overline{CAS}$ signal which controls the latch circuits.

When four addresses are accessed sequentially, the row addresses on and after the second bit need not be selected. This facilitates timing design. In nibble mode, the operation is limited to four addresses, however, it enables a faster access (t_{NAC}) than page mode.

Static Column Mode: In the static column mode, the column address is switched without the synchronized signal by high speed static RAM technology in the peripheral circuits.

Table 4-1 Comparison of Dynamic RAM High Speed Access Modes

Normal mode	
Fast Page mode	
Nibble mode	
Static column mode	

4.6 Refresh

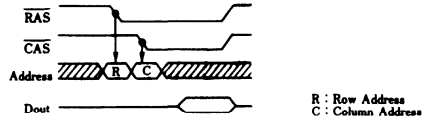
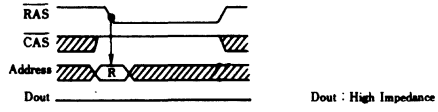
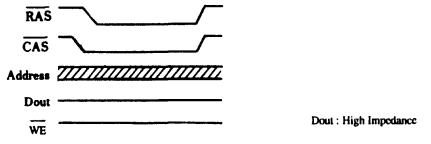
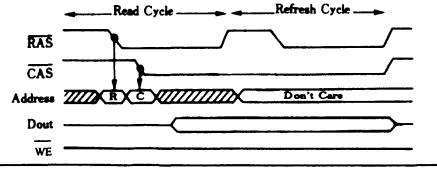
The refresh operation is performed by accessing every word line within the specified time (refresh cycle). Table 4-2 compares the following refresh modes in dynamic RAM.

$\overline{\text{RAS}}$-Only Refresh: In the $\overline{\text{RAS}}$-only refresh mode, refresh can be completed by selecting only row addresses synchronized with $\overline{\text{RAS}}$.

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh: This mode refreshes by the $\overline{\text{CAS}}$ falling edge before $\overline{\text{RAS}}$ in the period defined by the internal refresh address generator. This mode simplifies the external address multiplexer.

Hidden Refresh: In the hidden refresh mode, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is performed while output data is valid.

Table 4-2 Comparison of Dynamic RAM Refresh Modes

Read	
$\overline{\text{RAS}}$-only refresh	
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh	
Hidden refresh	

▨: Don't care

5. EEPROM

5.1 EEPROM Memory Cell

An EEPROM is an electrically erasable and programmable ROM which can be erased or written remotely while the system is in operation.

Hitachi EEPROM memory cells are MNOS-type (Metal Nitride Oxide Semiconductor) as shown is Figure 5-1.

A MNOS memory cell consists of two layers of oxide film and nitride film. The thickness of the oxide film is about 20 Å and the nitride film is 300 to 500 Å. There are traps in the boundary of the oxide and nitride films to catch electrons. The electrons move by the tunneling phenomenon between the substrate and traps.

5.2 64-kbit CMOS EEPROM Function

Page Write Function: The 64-kbit HN58C65 can latch 32 bytes (max.) and write them in one write cycle. The write cycle time is specified as 10 ms (max.). The effective byte write speed of HN58C65 in page write mode is 10 ms/32 bytes = 0.31 ms/byte.

Thus it takes only 2.56 seconds to write the entire HN58C65. Figure 5.2 shows the internal operation. The following describes the operation sequence:

1. The 32-byte memory cell data at the row address selected by address pins A5–A12 are latched.
2. Latched data at the column address specified by address pins A0–A4 are altered with write data, which is put into the D_{in} buffer from I/O pins I/O0–I/O7.
   The 32 bytes (max.) of latched data are altered by repeating this operation 32 times.
3. 32 bytes of memory cell data in the selected row 1 are erased (set to all 1).
4. Latched data is written into the selected row 3.
5. CPU acknowledges completion of the write cycle based on the internal timer. The HN58C65 provides RDY/$\overline{BUSY}$ and $\overline{DATA}$ polling to indicate the write completion.

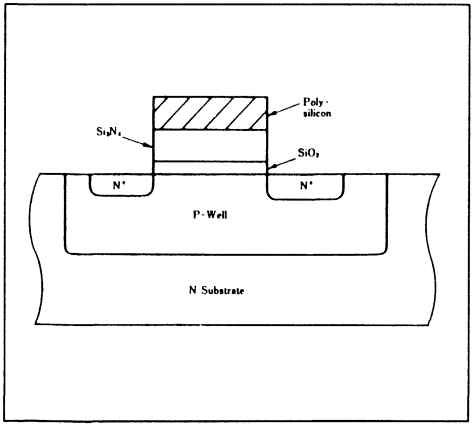


Figure 5-1 MNOS-Type Memory Transistor

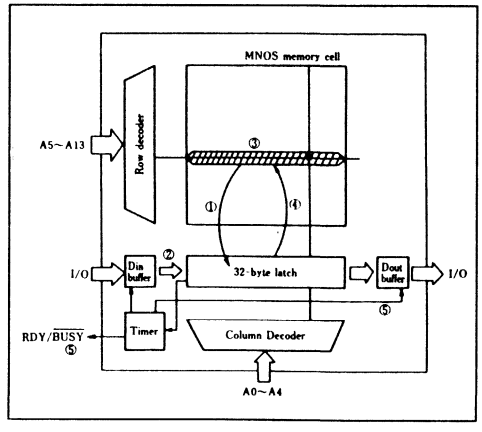


Figure 5-2 HN58C65 Page Write

Application

Internal Timer: The HN58C65 indicates the completion of data write to the CPU by using an internal timer. The HN58C65 enters the next cycle as soon as the completion of the write is detected. This function offers a high system throughput as the CPU can access other devices during a write cycle. The HN58C65 has two functions, RDY/$\overline{\text{BUSY}}$ and $\overline{\text{DATA}}$ polling, to indicate the completion of data write.

The RDY/$\overline{\text{BUSY}}$ approach indicates the completion of data write by using pin 1. It is low when the HN58C65 is in data write operation ($\overline{\text{BUSY}}$) and turns to the high impedance state at the end of data write (RDY). The RDY/$\overline{\text{BUSY}}$ pin should be pulled up as it uses open drain output. The RDY/$\overline{\text{BUSY}}$ pins can be OR-wired when using several HN58C65's.

The $\overline{\text{DATA}}$ polling approach, implemented in software, indicates the completion of data write through pin 19 (I/O7). While the data write is not completed, I/O7 shows an inverted version of what was written in the last cycle. In using this approach, the RDY/$\overline{\text{BUSY}}$ pin should be opened or grounded. The $\overline{\text{DATA}}$ polling approach can acknowledge the completion of data write in an individual HN58C65, even if several HN58C65's are used in the system.

Data Protection: The EEPROM performs data write with a higher voltage (V_{PP}) than the power supply voltage (V_{CC}). The HN58C65 internally generates V_{PP} by a high voltage generator with the combination of control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$). It supports the following functions to avoid accidental data write (data protection).

1. Data protection against noise on the control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during operation.
2. Data protection against noise at power on/off.

6. EPROM/OTPROM

6.1 EPROM Programming

Figure 6-1 shows the sectional structure of an EPROM memory cell. The upper gate, one of the gates made of two-layered polycrystalline silicon, is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected. This memory cell is programmed as follows.

With the substrate and source grounded, apply a high voltage between the drain and control gate. An electrical potential incline will occur between the source and drain so that the intensity of the electric field will become high near the drain. Because of this electric field, electrons are accelerated and the so-called hot electrons will be generated, which jump over the energy barrier of SiO_2 film. The hot electrons are pulled by the electric potential of the control gate and poured into the floating gate. Electrons stored in the floating gate remain stable as they fall into a well surrounded by an energy barrier of SiO_2 film. Therefore, it is evident that the quality of the SiO_2 film surrounding the floating gate is essential for good data retention characteristics. To keep data retention in the 5- or 10-year range, high quality SiO_2 film is needed.

Figure 6-2 shows the fundamental characteristics of the EPROM transistor. While I_D in a non-programmed transistor begins to flow with V_G of about 1 V, the current in a programmed transistor does not flow until V_G rises to 7 to 10 V. Therefore, if the voltage of the word line applied to the control gate is about 5 V in the readout, a non-programmed memory transistor will be on, and the programmed memory transistor will be off. This means that the data can be read out by means of the same structure as a NOR-type mask ROM.

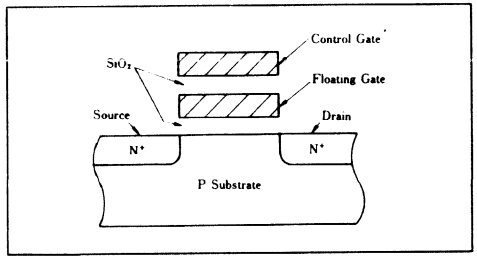


Figure 6-1 Cross Section of a EPROM Memory Cell

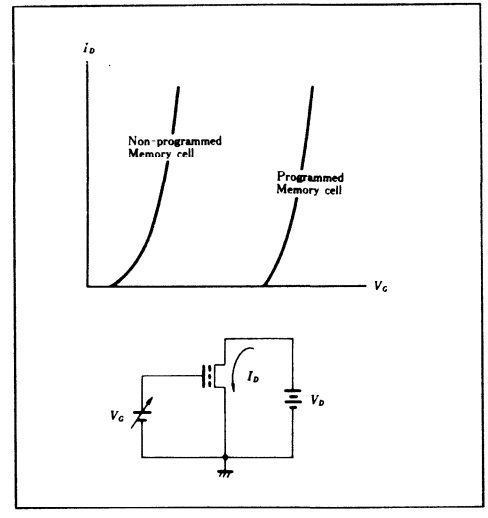


Figure 6-2 Fundamental Characteristic of a EPROM Memory Cell

6.2 Erasing EPROM

When shipped, all bits of the EPROM are at logic 1 with all electrons in the floating gate released (erased). Changing the logic 1 to logic 0, through the application of the specified waveform and voltage, programs the necessary information. The higher the V_{PP} voltage and the longer the program pulse width t_{PW}, the more electrons can be programmed in as shown in Figure 6-3. If V_{PP} exceeds the rated value, such as by overshoot, the pn junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and reduce the yield voltage. Hitachi's EPROMs can usually be written and erased more than 100 times.

EPROMs are erased by ultraviolet light exposure through a transparent window on the package. Electrons in the floating gate get energy from photons and become hot electrons again with enough energy to go over the energy barrier of SiO_2 film. The hot electrons go through to the control gate or the substrate and erasure is completed. Therefore, light with enough energy to get the electrons over the energy barrier of SiO_2 film is needed for erasure. Light energy is proportional to its frequency, and described as $E = h\nu$. E is the energy of light, h is Planck's constant, and ν is light frequency. Erasure is not caused by light over certain wavelengths and under certain wavelengths. However, the erasure time depends upon the quantity of photons, therefore the erasure time cannot be shortened by using a shorter wavelength. Figure 6-4 shows the relation between wavelength and erasure effectiveness. Erasure starts at about 4000 Å and is saturated at about 3000 Å.

For erasure, the wavelength and minimum irradiation rate of ultraviolet light must be 2537 Å and 15 W·s/cm^2 respectively. These conditions can be met by placing the device 2 to 3 cm below a 12,000 W/cm^2 UV lamp for about 20 minutes.

The UV transmittance of the transparent lid materials is about 70%. However, it is influenced by contamination or foreign materials on the lid surface. The contamination or foreign materials should be removed with a solvent such as alcohol that does not damage the package.

Figure 6-5 shows the EPROM standard erasure characteristics.

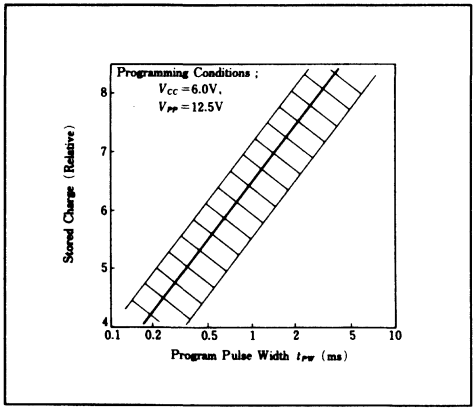


Figure 6-3 Standard Programming Characteristics of EPROMs

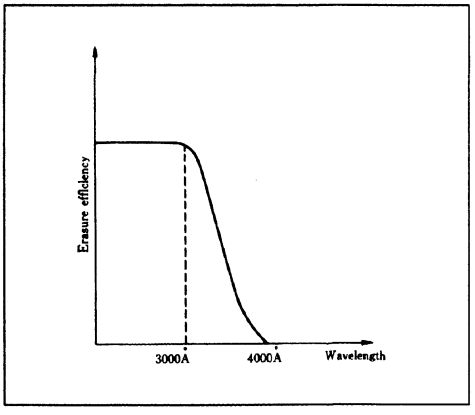


Figure 6-4 Erasure Efficiency of EPROM

6.3 EPROM Data Retention Characteristics

About 2 to 20 x 10^{-14} coulombs of electrons are accumulated in the floating gate when programmed. However, these electrons dissipate with time and the data may be inverted. The mechanism of electron dissipation is generally explained as follows.

Data Dissipation by Heat: The electrons at the floating gate are in a non-equilibrium state, so the dissipation of electrons by thermal energy is unavoidable. Therefore, the data retention time depends on temperature. Figure 6-6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

Data Dissipation by Ultraviolet Light: Ultraviolet light at a wavelength no greater than 3000 to 4000 Å is capable of releasing the electric charge at the floating gate of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet light, and so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Figure 6-7 shows the standard, data retention time under an ultraviolet eraser, sunlight and fluorescent lighting.

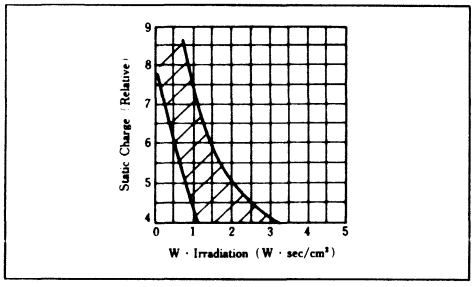


Figure 6-5 Standard Erasure Characteristics

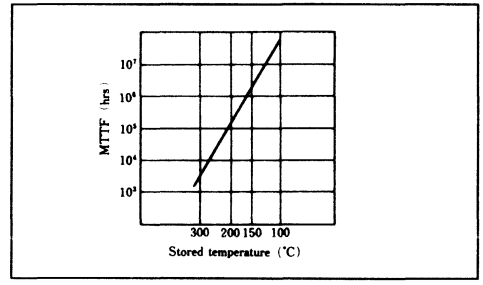


Figure 6-6 EPROM Data Retention Characteristic

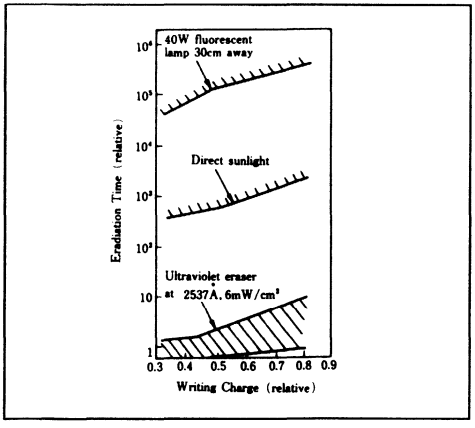


Figure 6-7 EPROM Data Retention Time

6.4 Optimized High Speed Programming

With the increase of EPROM density, the time for programming becomes more important. Methods for high speed programming have been developed and put into practical use for each EPROM generation.

These are the three methods for high speed programming.

1. First generation—Conventional programming
   This method is employed in 3 mm and 5 mm process products. Programming is performed with a uniform pulse of 50 ms per byte. Although it has the advantage of applying sufficient energy to all bits, it takes a significant amount of time to program high density devices.

2. Second generation—High performance programming
   This method is employed in 2 mm process products. High performance programming (Figure 6-8) is performed with a base pulse of 1 ms. It repeats programming and reading (verifying) until the data is properly recorded. There are two good points for this programming.
   First, the programming itself is performed at an optimum rate, depending on the capability of each memory cell.
   Second, after verification, the data is programmed using three times as long a pulse to assure high reliability data retention.

3. Third generation—Fast high-reliability programming
   This method is employed in 1.3 mm process products. Fast high-reliability programming (Figure 6-9) is performed with a base pulse of 0.2 ms. It also shortens the supplement pulse width to one-third of the high performance programming. As a result, this method uses less

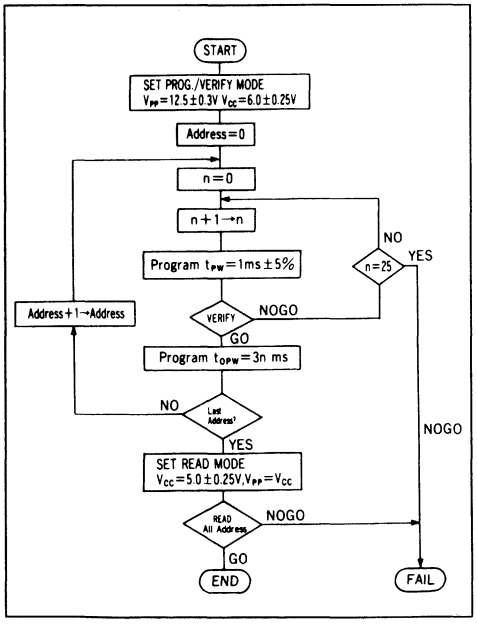


Figure 6-8 High Speed Programming (high performance programming)

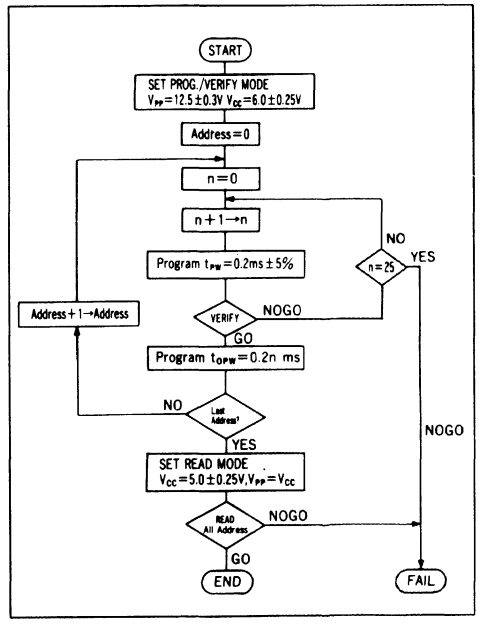


Figure 6-9 0.2 ms High Speed Programming (fast high-reliability programming)

programming time, reduced theoretically to one-tenth the time needed by the previous example. The 1-Mbit EPROM series employs page programming, which programs 32 bits at once (Figure 6-10), reducing programming time to a quarter of the time of fast high-reliability programming for 128 k × 8 organization, and to half for 64 k × 16 organization. Figure 6-11 shows the relative programming times of these methods.

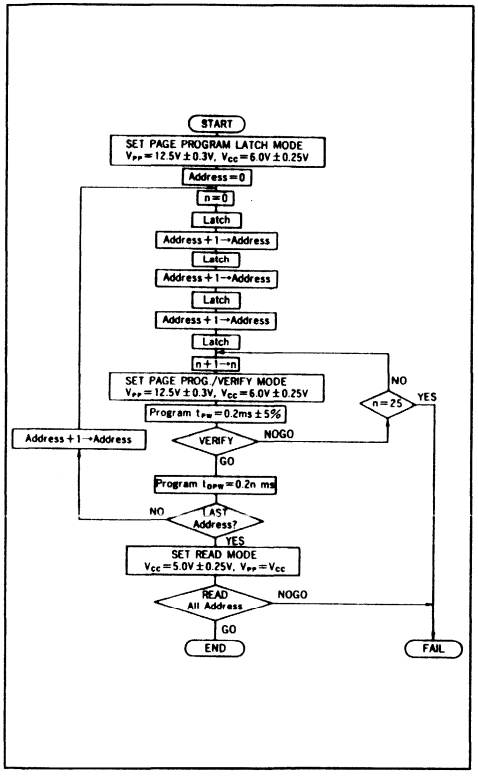


Figure 6-10 Page-Mode Programming (page programming)

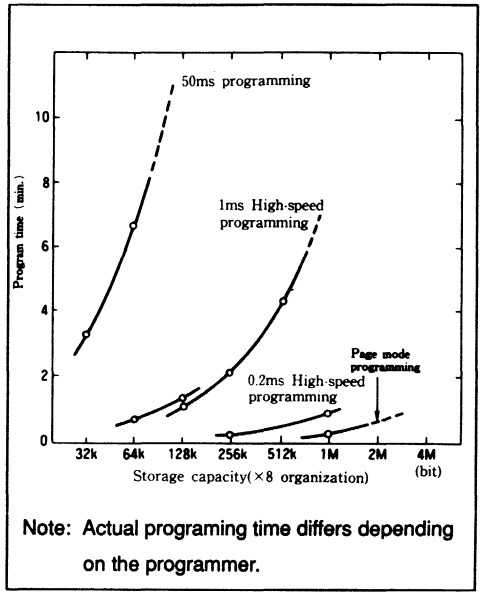


Figure 6-11 Comparison of Shortened Programming Time

6.5 Device Identifier Code

EPROM programming conditions depend on the EPROM manufacturers' standards and specific device types. Confusion on the proper use of varying methods required may cause poor or failing operation. As a countermeasure, some EPROMs provide embedded device identifier codes including such information as the manufacturer and device type. Some newly developed commercial EPROM programmers can set write conditions automatically by recognizing this code.

Different programming conditions are as follows.

1. Program voltage
2. Program timing
3. High performance programming algorithm
4. Pin configuration

The Hitachi EPROM has a device identifier code area adjacent to the memory access area as shown in Figure 6-12.

Table 6-1 describes how to use the device identifier code. Setting A9 at 12 V and A1–A8, A10–A13 at V_{IL}, access the device identifier code area and I/O0–I/O7, and output the programming condition code with V_{IL} or V_{IH} of A0.

Table 6-1 Hitachi EPROM Device Identifier Code

		A_0	I/O8–I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
Manufacturer code	Hitachi	V_{IL}	—	0	0	0	0	0	1	1	1	07
ROM code	HN27128A	V_{IH}	—	0	0	0	0	1	1	1	1	0D
	HN27256	V_{IH}	—	0	0	0	1	0	0	0	0	10
	HN27C256	V_{IH}	—	1	0	1	1	0	0	0	0	B0
	HN27C256H	V_{IH}	—	0	0	1	1	0	0	0	1	31
	HN27C256A	V_{IH}	—	0	0	1	1	0	0	0	1	31
	HN27512	V_{IH}	—	1	0	0	1	0	1	0	0	94
	HN27C1024H	V_{IH}	—	1	0	1	1	1	0	1	0	BA
	HN27C101A	V_{IH}	—	0	0	1	1	1	0	0	0	38
	HN27C301A	V_{IH}	—	1	0	1	1	1	0	0	1	B9

A9: 12 V

A1–A8, A10–A13: V_{IL}

A14, A15: Don't care

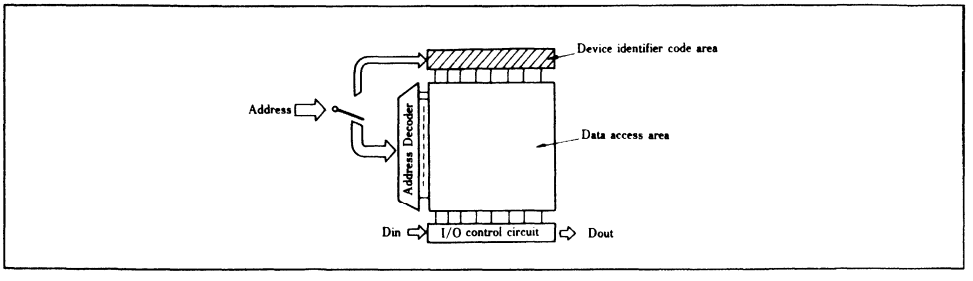


Figure 6-12 Device Identifier Code

6.6 Shielding Label

When using an EPROM in an environment where it can be exposed to ultraviolet light, Hitachi recommends placing a shielding label over the transparent lid to absorb the ultraviolet light. In choosing a shielding label, the following points should be carefully checked.

1. Adhesiveness (mechanical strength)
   Avoid repeated removal and reattachments, or exposure to dust that may reduce the adhesive strength. Ultraviolet erasure and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to place a new one over the old one since peeling may create a static charge.)

2. Allowable temperature range
   Use the shielding label in an environment where temperature is stable within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too tightly. When it hardens, the label may come off easily. When it sticks too tightly, the paste may remain on the window glass after the label has been removed.

3. Moisture resistance
   Use the shielding label in an environment where humidity is stable within the specified allowable humidity range.

6.7 EPROM Programmer

The EPROM programmer stores the user's program in its internal RAM and writes the program in the EPROM. For this programming, at least three functions are necessary: blank check function prior to programming, programming function, and the verify function after programming. Figure 6-13 shows the programming flowchart. Some programmers check for pin contact failure or reverse insertion before the blank check.

The outline of each check is as follows.

1. Pin contact check
   In the ROM pin and socket connection test, checking is normally performed by detecting forward current at each EPROM pin. Care is necessary as this forward biased resistance differs in products of each company.

2. Reverse insertion check
   This check detects the reverse insertion of the device, then places the equipment in reset mode and protects the device and equipment if the condition is found.

3. Blank check
   This check is performed before programming. It checks whether the device is an erased EPROM, or it prevents EPROM reprogramming. Since output data in the erased condition is high, the check is for whether the data in the EPROM are all 1s. It will fail even if one bit is 0. Normally, it is designed to provide a warning with a lamp or buzzer.

4. Programming
   The function of programming the data from the internal RAM of the programmer into the EPROM will fail when programming cannot be done. The normal flow is as shown in Figure 6-14. The EPROM data for a target location will be read out prior to programming and compared with the programming data intended for that location. If the data matches, programming will be skipped. If they differ, programming will be performed. Then, the data will be read back and compared with the original programming data, and if they match, the programmer will progress to the next address.

5. Verify
   This function checks after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer. It will fail when they do not match. Normally, when it fails, it lights the fail lamp and displays the address and data.

6. How to input a program
   Table 6-2 shows several metnods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are preferred options.

6.8 Handling EPROMs

Being touched with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give the false impression that information has been correctly written in. As already reported at international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges by irradiating the EPROM with ultraviolet rays for a short time. The EPROM should be reprogrammed after this irradiation since it also reduces the electric charges in the floating gates. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods, as in the prevention of common static breakdown of ICs.

1. Ground operators who handle the EPROM. Avoid using things such as gloves that may generate static electricity.
2. Avoid rubbing the glass window with plastic or other materials that may generate static electricity.
3. Avoid the use of coolant sprays which may contain some free ions.
4. Use shielding labels (especially those containing conductive substances) that can evenly distribute any established charge.

Table 6-2 EPROM Data Input

Method	Content
Copy input	Input by copying the master ROM
Manual input	Input by the keyswitches on the front panel. Used for correction or revision of programs
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction, and list preparation of the program can be made

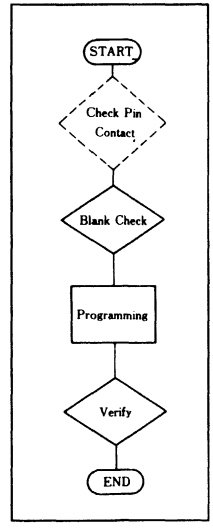


Figure 6-13 Programming Flowchart of EPROM Programmer (1)

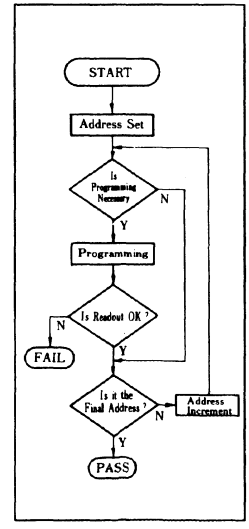


Figure 6-14 Programming Flowchart of EPROM Programmer (2)

6.9 Ensuring OTPROM Reliability

The one-time-programmable ROM (OTPROM) has two forms: standard dual in-line package (DIP) and small outline package (SOP). It is only one-time programmable because it has no window for ultraviolet light exposure; testing by programming; and erasure cannot be performed after it is assembled.

As a means of improving reliability, Hitachi performs screening tests for programming, access time, and data retention on OTPROM wafers during the manufacturing process.

However, rare defects may occur in the assembly process that cannot be completely removed in the final test screening which is only a reading test. Therefore, Hitachi recommends that users perform high temperature baking after programming these devices to ensure the highest reliability.

Detailed conditions and procedures for screening are shown in Figure 6-15. First, program and verify the devices. Then leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, check the readout function, and discard chips with data retention failures.

From the results of devices in which the recommended screening test is properly performed, we find the data retention characteristics of OTPROMs are generally equal to EPROMs.

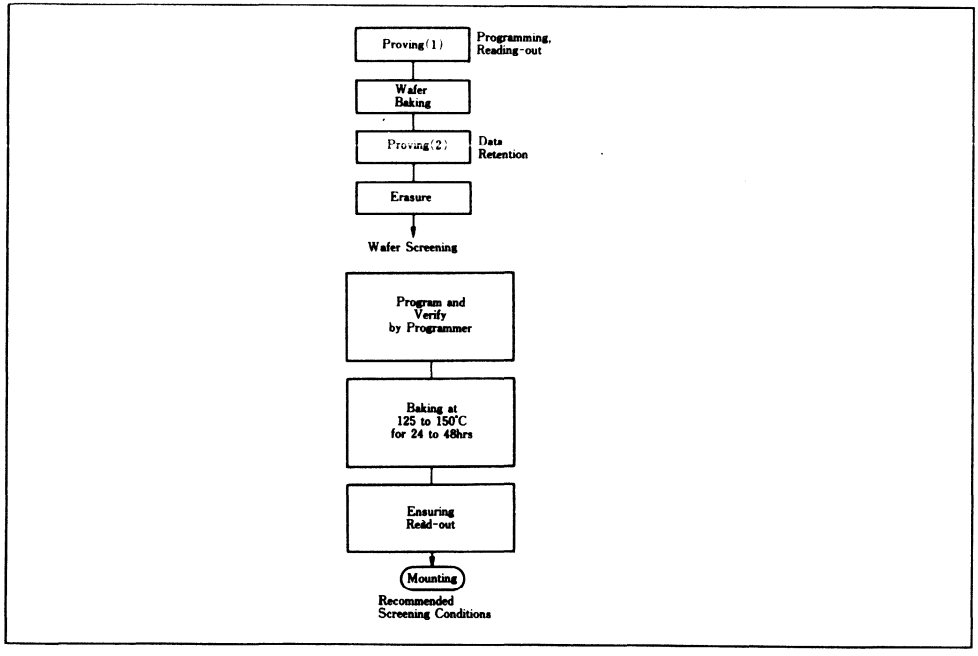


Figure 6-15 Screening Flowchart of OTPROM

7. Mask ROM Programming Instruction

The writing of custom program code into mask ROMs is performed by a CAD system on a large-scale computer. ROM code data should confirm to the specifications given below, using either paper tape, EPROM, or magnetic tape. Additional instructions, such as chip select or customer part numbers, should be noted on the "ROM Specification Identification Sheet."

7.1 Specification of EPROM

1. Submit the three sets of EPROM-stored data. Specify the address of the EPROM in the case of two or four EPROMs.

2. The ROM code data is input from the start address to the final address in the EPROM.

3. Type of EPROM.
   HN482764 (8 kwords × 8 bits, 2764 compatible)
   HN4827128 (16 kwords × 8 bits, 27128 compatible)
   HN27256 (32 kwords × 8 bits, 27256 compatible)
   HN27C256 (32 kwords × 8 bits, 27C256 compatible)

7.2 Specification of Magnetic Tape

1. Use the following magnetic tape format, which can be read by a device compatible with an IBM magnetic tape device.
   Length: 2400 feet, 1200 feet or 600 feet
   Width: 1/2 inch
   Channel: 9 channels
   Bit density: 800 BPI or 1600 BPI (Clearly state on the "ROM Specification Identification Sheet" which is used.)

2. Use EBCDIC code.

3. Use these format parameters for data recorded on magnetic tape:
   No leading tape mark
   No label
   Record size 80 bytes/record
   Block size 10 records/block
   The end of the file should be indicated by two successive tape marks (TM) (Figure 7-1).

4. The HMCS6800 load module data mode is the object mode output from the assembler HMCS6800.
   Divide the 8-bit code into the upper and lower 4-bit codes, and convert each into hexadecimal notation.
   Example: The code 1100 0110 is as follows under binary notation.

(Upper 4 bits)				(Lower 4 bits)				Bit weight
D7	D6	D5	D4	D3	D2	D1	D0	(ROM output
1	1	0	0	0	1	1	0	equivalence)

   The actual load module mode format detail is shown in Figure 7-2.

   S0 indicates the head of the file and S9 indicates the end of the file. The actual data starts following S1. This means that data starts from the address (hexadecimal) indicated in the address size section of the record. The address of the address size of the data recorder is compared with the next data recorder address by counting in increments of one byte of data and checking whether it is sequential or not. The printed example of the HMCS6800 load module mode is as shown in Figure 7-3.

   If an address is skipped in the original source code, enter the skipped address into the "ROM Specification Identification Sheet" and the data (00 or FF) that should be entered into the

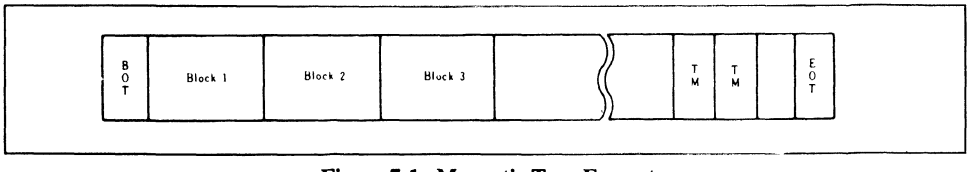


Figure 7-1 Magnetic Tape Format

5. BNPF mode. One word is symbolized by the word start mark B, the bit content represented by eight characters of P and N, and the BNPF slice composed of 10 successive characters of the word end mark F.
   The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.
   Example: The code of AA (hexadecimal) is symbolized as shown in Figure 7-4.

   It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of the "ROM Specification Identification Sheet" always becomes 0.
   B: Indicates the start of one word.
   N: Indicates one bit word.
   P: Indicates one bit of one data.
   F: Indicates the end of one word.

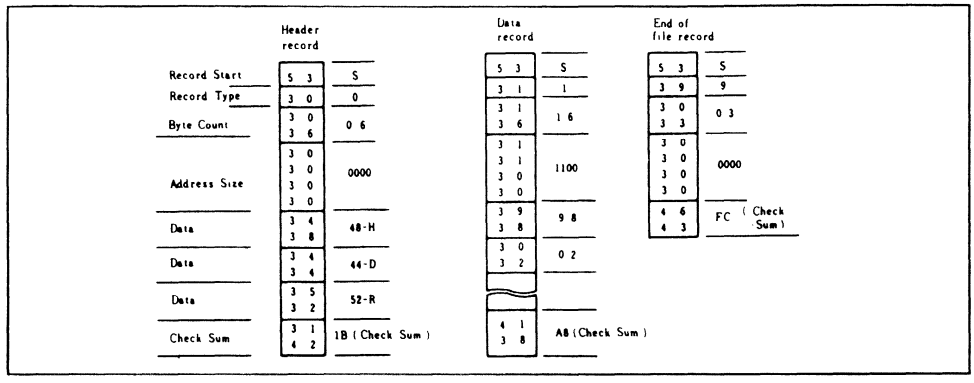


Figure 7-2 HMCS6800 Load Module Data Format

```
Header Record  →S00B000058204558414D504CB5

Data Record    →S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24

Data Record    →S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of
File Record    →S9030000FC
```

Figure 7-3 HMCS6800 Load Module Data Example

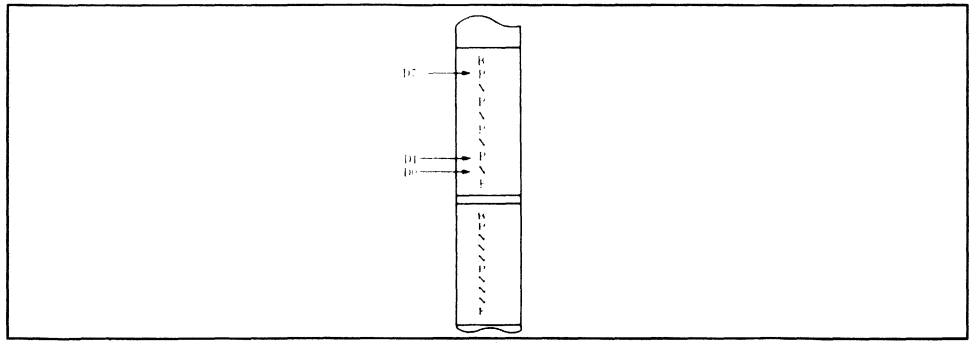


Figure 7-4 BNPF Mode Example

7.3 Floppy Disk Specification

1. Use the following type of floppy disk (Figure 7-5):
   Type: 8-inch single sided andsingle density
   Number of sectors: 26
   Number of tracks: 77

2. Use EBCDIC as the user code.

3. Format the floppy disk as described below. The composition is described in Table 7-1.
   Record size: 80 bytes/record

   Use the sectors as shown in Figure 7-6. Use one sector for one record, that is, the first of 128 bytes of the sector will contain data.

4. Data mode. See data mode for magnetic tape.

Table 7-1 Floppy Disk Composition

		Location	
No.	**Item**	**Track**	**Sector**
1	Standard volume label	00	07
2	Standard head label	00	08–26
3	Data area	01–73	01–26
4	Alternate tracks	75, 76	01–26
5	Spare track	00	01–06
		74	01–26

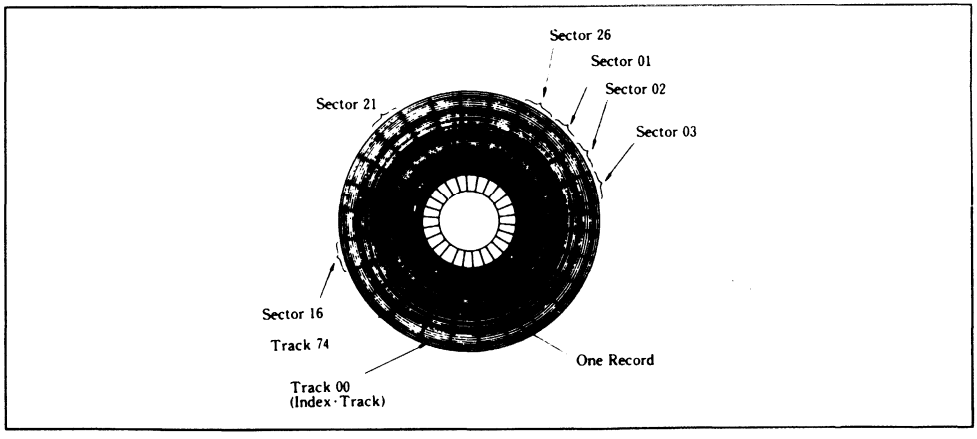


Figure 7-5 Floppy Disk Format

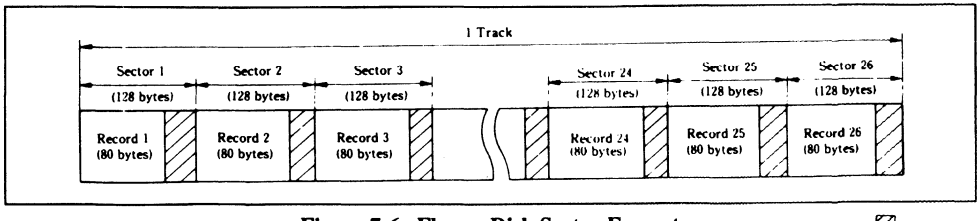


Figure 7-6 Floppy Disk Sector Format

: unused

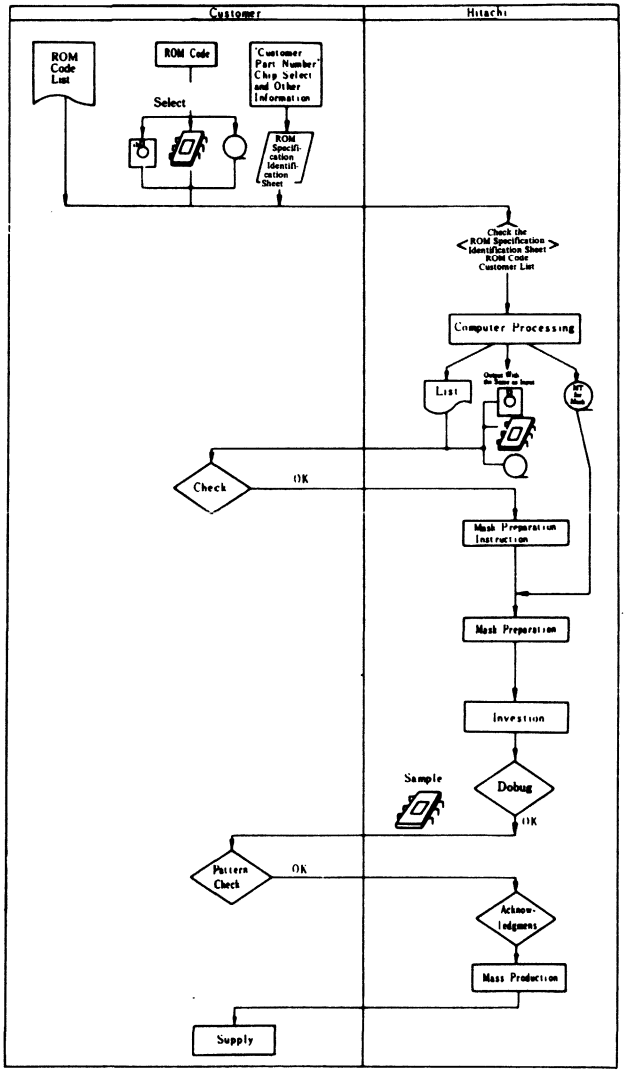


Figure 7-7 Mask ROM Development Flowchart

8. Instructions for Using Memory Devices

8.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled with these precautions:

1. In transporting and storing memory devices, place them in a conductive magazine or wrapper, or put all pins of each device into a conductive mat, so that they are kept at the same potential. Manufacturers should give sufficient consideration on proper packing when shipping their products.

2. When the devices are to be touched during mounting or inspection, the handler must be grounded. Do not forget to connect a resistor (1 MΩ approximately is desirable) in series to protect from electrical shock.

3. Keep the relative ambient humidity at about 50% during processing.

4. For working clothes, cotton is preferable to synthetic fabrics.

5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.

6. When transporting a board with memory devices mounted on it, enclose it with conductive materials.

7. Use conductive materials of high resistance (about 10^9 ohms) to protect the devices from electrostatic discharge. Otherwise, if accidentally put in contact with conductive materials such as a metal sheet, the devices may deteriorate or even breakdown, owing to the sudden release of charge stored on the surface.

8. Never set a system in which memory devices are used near anything that generates high voltage (e.g. a CRT anode electrode, etc.).

8.2 Using CMOS Memories

As shown in Figure 8-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 8-2 shows the relationship between the input voltage and current within the inverter. The top and bottom transistors turn on and create a current flow when the input voltage reaches an intermediate level. Therefore it is necessary to keep the input voltage below 0.2 V or above V_{CC} – 0.2 V in order to minimize power consumption. The data sheet specifies the standby current for two cases of input level (with minimum V_{IH} and maximum V_{IL}, and with 0.2 V or V_{CC} – 0.2 V), and the difference in values as being remarkably great. Some memory devices are designed to cut off such current flow in the standby mode by the control of input signals, but this depends on the specific device type. This should be confirmed in data sheets for each device type.

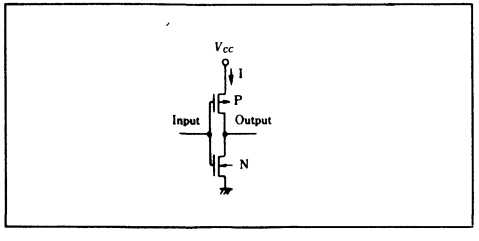


Figure 8-1 CMOS Inverter

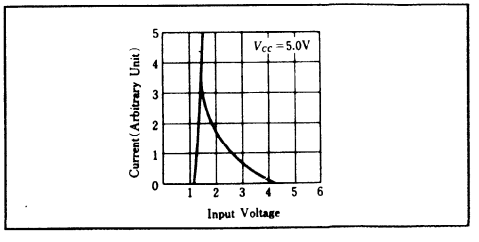


Figure 8-2 Relationship Between Input Voltage and Current in a CMOS Inverter

Another problem peculiar to CMOS devices is latch up. Figure 8-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in Figure 8-4. When positive dc current or pulse noise is applied (Figure 8-4a), T_{R3} is turned on owing to the bias voltage generated between the base and emitter. Also, trigger current flows to ground through R_P, the base resistance of T_{R2}. As a result, T_{R2} becomes conductive and the current flows from power supply (V_{CC}) through the base resistance of T_{R1} (R_N), which also puts T_{R1} into conduction. Then as the base of T_{R2} is rebiased by the collector current from T_{R1}, the closed loop consisting of T_{R1} and T_{R2} reacts. Thus, current flows constantly between the power supply (V_{CC}) and ground even without the trigger current caused by outside noise.

Latch up can also be caused by a negative pulse (Figure 8-4 b). Most semiconductor memory manufacturers are trying to improve latch up immunity in their products. Hitachi provides a broad enough guard band by applying a diffusion layer around the inputs and outputs, taking care not to connect the input to the p^+ diffusion layer. The input voltage for the 64-kbit static RAM HM62256, for example, is specified as follows:

V_{IH} max 6.0 V (not dependent on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
–0.5 V (dc level)

Thus almost no consideration for latch up is required in system designs using these devices.

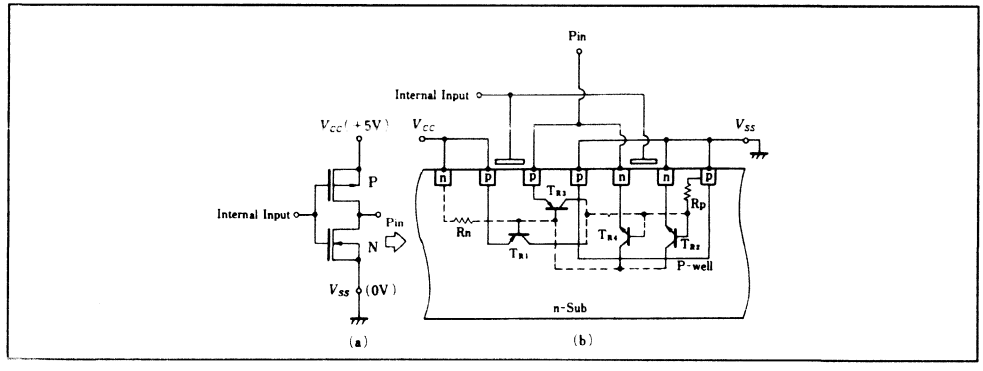


Figure 8-3 Cross Section Structure of CMOS Inverter

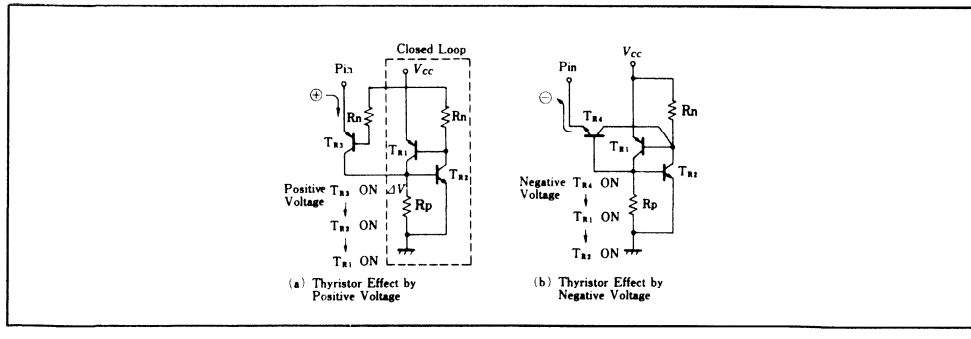


Figure 8-4 Equivalent Circuit of Parasitic Thyristor

8.3 Noise Prevention

Noise in semiconductor memories is roughly classified into input signal noise and power supply noise.

Input Signal Noise: Input signal noise is caused by overshoot and undershoot. If either of them exceeds the recommended dc operating conditions, normal operation is hindered, and voltage over absolute maximum rating will break the device. When operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohms into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because it is often caused by an unstable reference voltage (ground level).

Power Supply Noise: Power supply noise can be classed as low frequency and high frequency as shown in Figure 8-5. To assure a stable memory operation, combined low- and high-frequency noise should be held below 10 percent of the standard level of the peak-to-peak power supply voltage.

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during the transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, the voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1–0.01 μF should be inserted near the device. The following points must be considered in designing the layout of a board:

1. For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.

2. Bypass capacitors must be applied to the power supply pins of memory devices as near as possible, and inductance in the path from the V_{CC} pin to V_{SS} pin through the bypass capacitor must be kept as low as possible.

3. The line connected to the power supply on the board should be as wide as possible.

4. It is preferable for the power supply line to be at right angles to the devices selected at the same time, lest too much peak current should flow through one power supply line at a time.

8.4 Address Input Waveform of Hi-BiCMOS Memory

Data stored in memory might be destroyed in a case where the address input of a HM6716, HM6719, HM6787, HM6788, or HM6789 series device floats and sticks near threshold voltage (e.g. CPU sets the address bus to off state in Figure 8-7). Consequently, the following three methods are recommended to prevent malfunctions of a Hi-BiCMOS memory device.

A: Insert the latch as shown in Figure 8-7 to keep the address input from floating.
B: Set $\overline{CS}$ high while the address input floats.
C: Insert a pull-up resistor (R) to hold the time constant of the rising edge waveform on the address input pin ($t_r = R \times C$) below 150 ns.

Stable operation can be assured if you have already adopted the above three methods (A, B, C). Should you have any further problems please contact one of our sales offices.

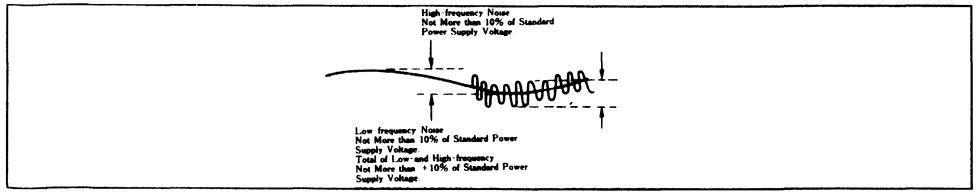


Figure 8-5 Power Supply Noise

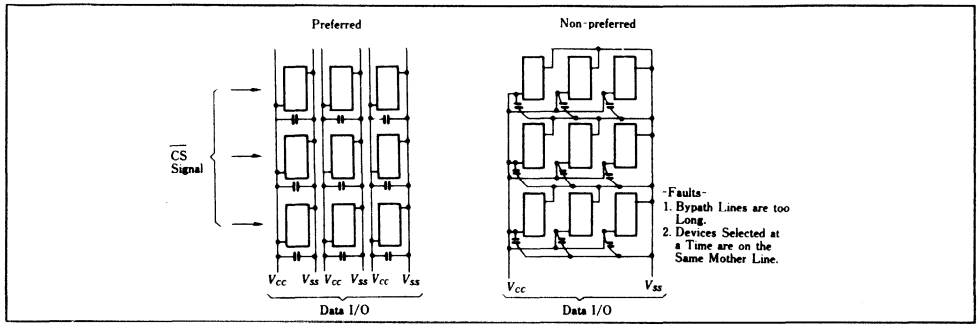


Figure 8-6 Examples of a Power Supply Board Pattern

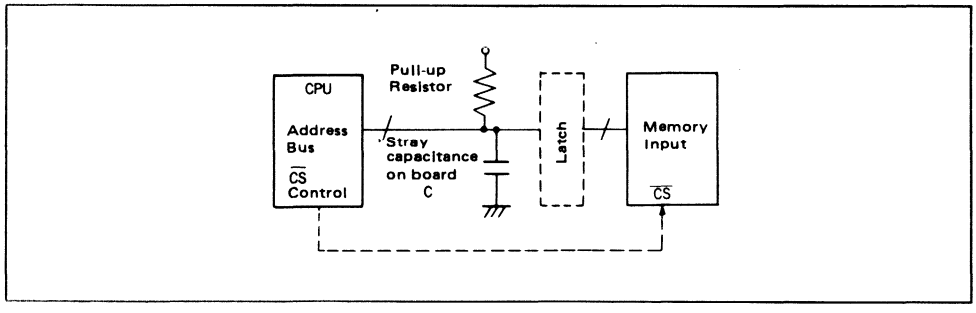


Figure 8-7

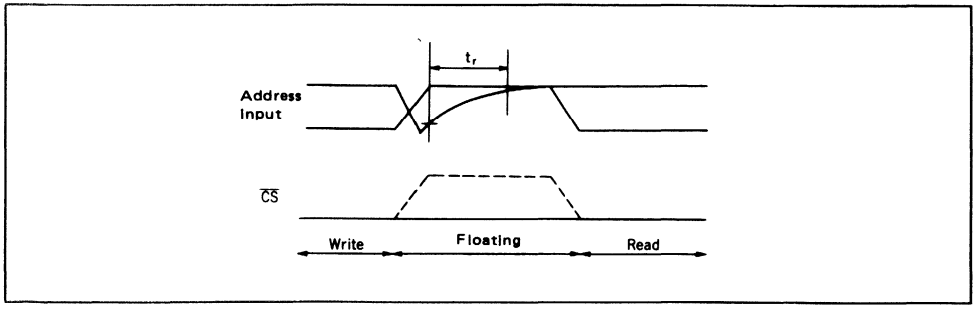


Figure 8-8

DATA SHEETS

MOS
STATIC
RAM

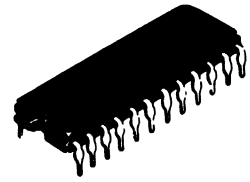
HM6116 Series —— Maintenance Only

2048-word x 8-bit High Speed CMOS Static RAM

■FEATURES

- Single 5V Supply
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.)
    10μW (typ.) (L-version)
  - Operation: 200mW (typ.)
    175mW (typ.) (L-version)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116P Series



(DP-24)

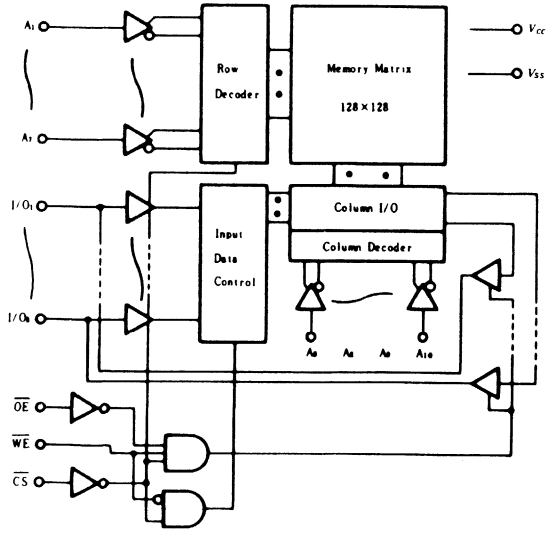
HM6116FP Series

(FP-24D)

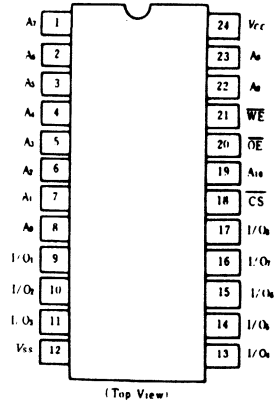
■ORDERING INFORMATION

Type No.	Access Time	Package
HM6116P-2 HM6116P-3 HM6116P-4	120ns 150ns 200ns	600mil 24pin Plastic DIP
HM6116LP-2 HM6116LP-3 HM6116LP-4	120 ns 150 ns 200 ns	
HM6116FP-2 HM6116FP-3 HM6114FP-4	120 ns 150 ns 200 ns	24pin Plastic SOP
HM6116LFP-2 HM6116LFP-3 HM6116LFP-4	120 ns 150 ns 200 ns	

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



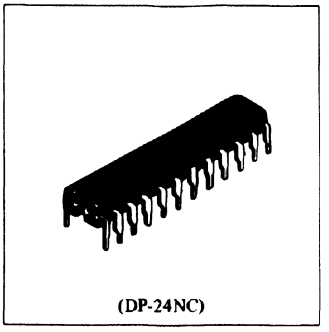
(Top View)

Note) This device is not available for new application.

HM6716, HM6719 Series

2048-word x 8-bit High Speed Hi-BiCMOS Static RAM
2048-word x 9-bit High Speed Hi-BiCMOS Static RAM

- **Features**
- Fast Access Time: 25/30ns (max)
- Low Power Dissipation (DC): 280mW (typ.)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

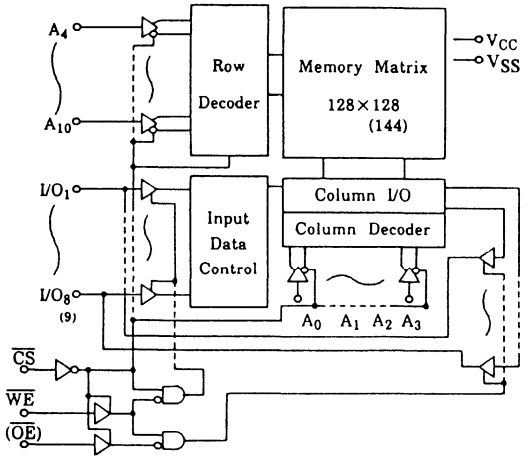


(DP-24NC)

■ Ordering Information

Type No.	Access Time	Package
HM6716P-25	25ns	300 mil 24 Pin Plastic DIP
HM6716P-30	30ns	
HM6719P-25	25ns	
HM6719P-30	30ns	

■ Block Diagram

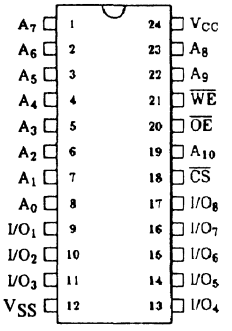


■ Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range (with bias)	T_{stg} (bias)	−10 to +85	°C

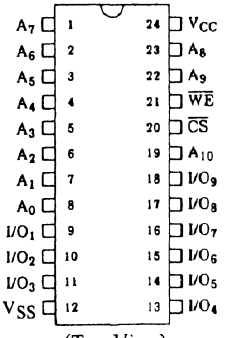
■ Pin Arrangement

● **HM6716**



(Top View)

● **HM6719**



(Top View)

■ Truth Table

● HM6716

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–

● HM6719

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (2) (3)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

■ Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}*)	−3.0	–	0.8	V

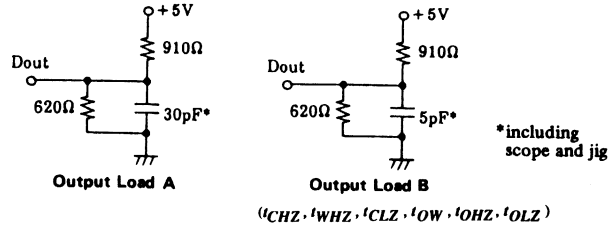
*) Pulse Width: 20ns, DC: −0.5V

■ DC and Operating Characteristics (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}= V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	–	120	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$=0mA	–	–	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	–	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC}−0.2V	–	–	10	mA
Output Low Voltage	V_{OL}	I_{OL}=4mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1mA	2.4	–	–	V

■ AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input and Output reference levels: 1.5V
Input rise and fall time: 4ns
Output Load: See Figure



(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW}, t_{OHZ}, t_{OLZ})

■ **Capacitance** (T_a = 25°C, f = 1.0 MHz)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	–	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ **AC Characteristics** (V_{CC} 5V ± 10%, T_a = 0 to +70°C, unless otherwise noted.)

● **Read Cycle**

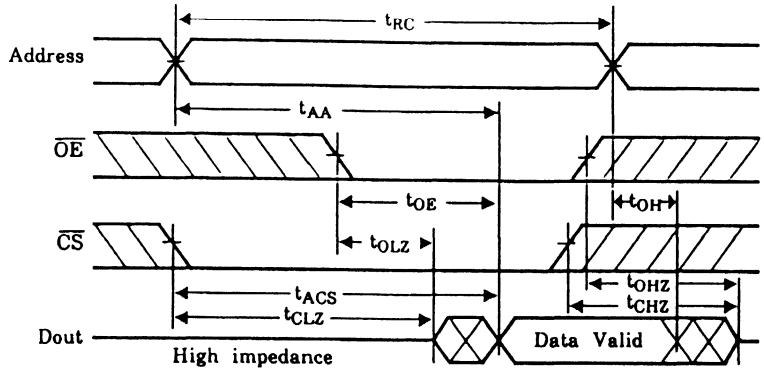
Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	–
Address Access Time	t_{AA}	–	25	–	30	ns	–
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	–
Chip Selection to Output in Low Z	t_{CLZ}	0	–	0	–	ns	*2
Output Enable to Output Valid	t_{OE}	0	20	0	20	ns	*1
Output Enable to Output in Low Z	t_{OLZ}	0	–	0	–	ns	*1, *2
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns	*2
Chip Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	*3

● **Write Cycle**

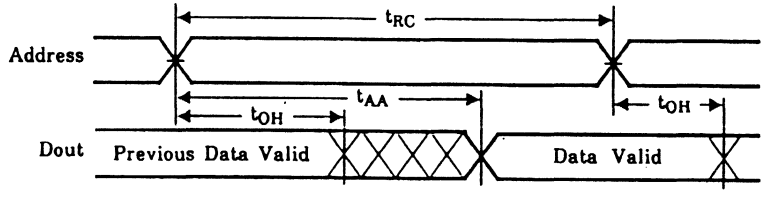
Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	25	–	30	–	ns	–
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	–
Write Pulse Width	t_{WP}	20	–	25	–	ns	–
Write Recovery Time	t_{WR}	0	–	0	–	ns	–
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Write to Output in High Z	t_{WHZ}	0	10	0	12	ns	*2
Data Valid to End of Write	t_{DW}	15	–	15	–	ns	–
Data Hold Time	t_{DH}	5	–	5	–	ns	–
Output Active from End of Write	t_{OW}	0	–	0	–	ns	*2

Notes) *1. These parameters are for HM6716.
*2. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
*3. Please contact your nearest Hitachi's Sale Dept. regarding specification.

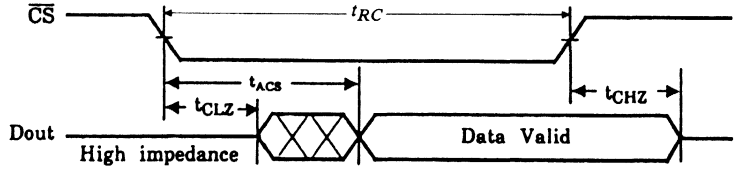
- Timing Waveforms
- Read Cycle (1)*1



- Read Cycle (2)*1,*2,*4

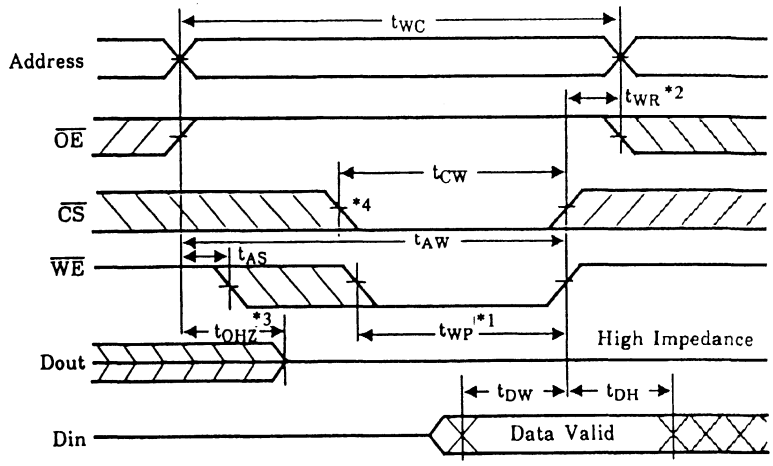


- Read Cycle (3)*1,*3,*4

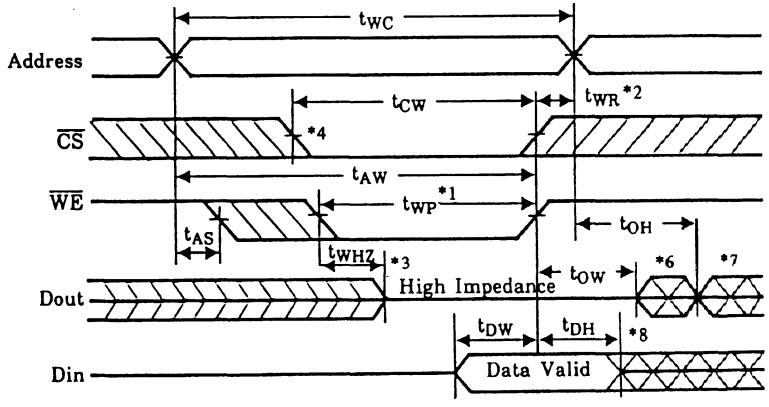


Notes) *1. $\overline{WE}$ is High for Read Cycle.
*2. Device is continuously selected, $\overline{CS}=V_{IL}$.
*3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
*4. $\overline{OE}=V_{IL}$.

- **Write Cycle (1)**



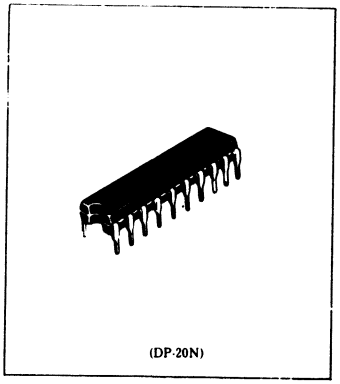
- **Write Cycle (2)** *5



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL}).
*6. Dout is the same phase of write data of this write cycle.
*7. Dout is the read data of next address.
*8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6268 Series

4096-word x 4-bit High Speed CMOS Static RAM



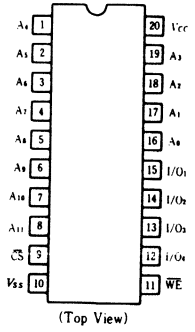
■FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35/45ns (max.)
- Low Power Standby: 100μW typ, 5μW typ (L-version)
  Active: 250mW typ.
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

■ORDERING INFORMATION

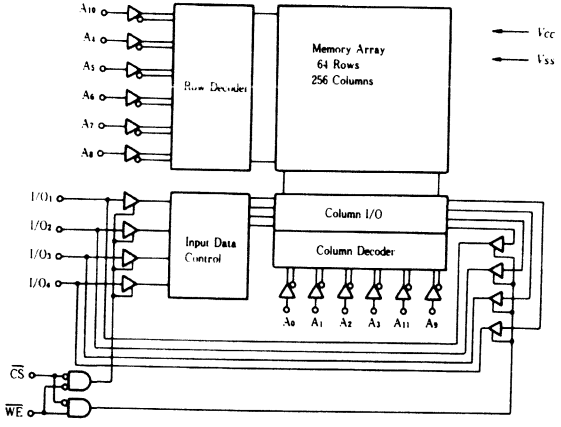
Type No.	Access Time	Package
HM6268P-25 HM6268P-35 HM6268P-45	25ns 35ns 45ns	300mil 20pin Plastic DIP
HM6268LP-25 HM6268LP-35 HM6268LP-45	25ns 35ns 45ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width≦10ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	-
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED OPERATING CONDITIONS (Ta = 0 to +70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	-	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	-	0.8	V

Note) *1. −3.0V for pulse width≦10ns.

■DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70℃)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	-	-	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	-	-	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, min. cycle	-	50*3	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	-	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ ≧ V_{CC} − 0.2V,	-	0.02	2.0	mA
		0V ≦ V_{IN} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{IN}	-	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4	-	-	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. 40mA typ. for 45ns version.

■CAPACITANCE (Ta = 25°C, f = 1.0MHz)

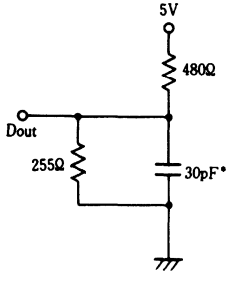
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	-	9	pF

Note: This parameter is sampled and not 100% tested.

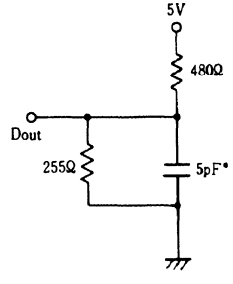
■AC CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 to +70℃, unless otherwise noted.)

- **AC Test Conditions**
  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



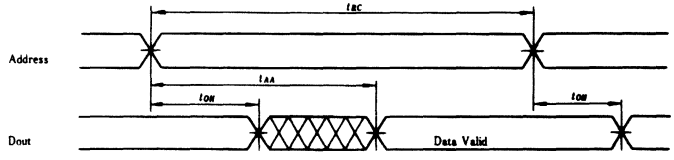
*Including scope and jig.

● READ CYCLE

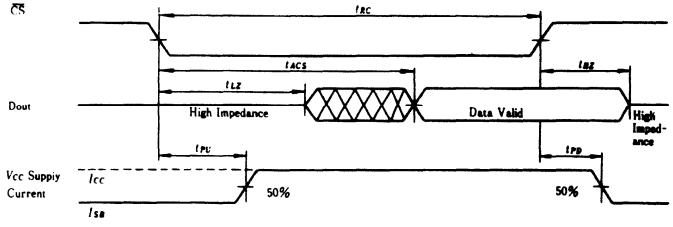
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*1	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	25	—	30	ns

Note) * 1. Transition is measured ± 200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1(1),(2)



● Timing Waveform of Read Cycle No. 2(1),(3)



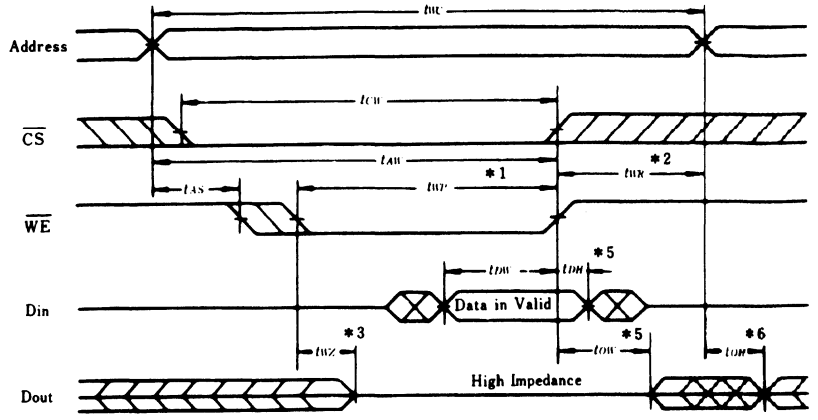
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

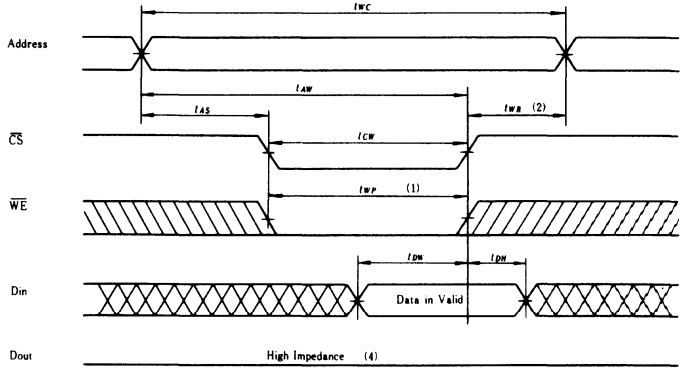
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	35	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}*1	0	8	0	10	0	15	ns
Output Active from End of Write	t_{OW}*1	0	—	0	—	0	—	ns

Note) * 1. Transition is measured ± 200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

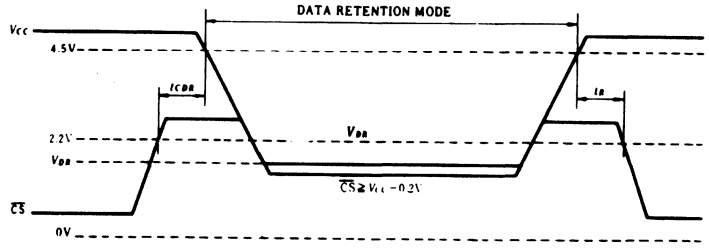
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leq Ta \leq 70°C$)

This characteristics guaranteed only for L-version.

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{in} \geq V_{CC} - 0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

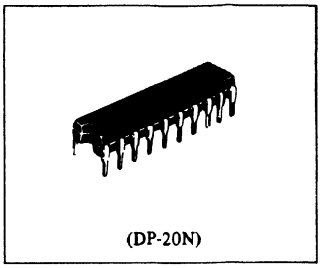
Notes) *1. t_{RC} = Read Cycle Time.
*2. $V_{CC} = 3.0V$
*3. $V_{CC} = 2.0V$

●LOW V_{CC} DATA RETENTION WAVEFORM



HM6267 Series

16384-word x 1-bit High Speed CMOS Static RAM



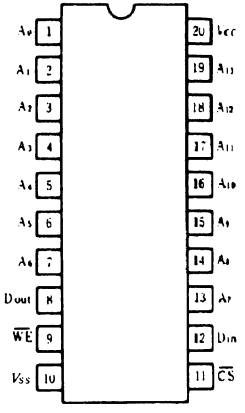
■ FEATURES

- High Speed: Fast Access Time 35/45/55ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.)/5μW (typ.) (L-version),
  Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

■ ORDERING INFORMATION

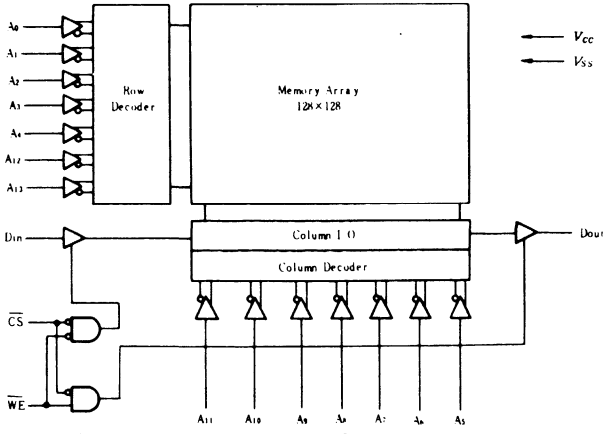
Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plactic DIP
HM6267P-45	45ns	
HM6267P-55	55ns	
HM6267LP-35	35ns	
HM6267LP-45	45ns	
HM6267LP-55	55ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*1	V_T	-0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

Notes) *1. With respect ot V_{SS}.
*2. -3.5V for pulse width ≦ 20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.5*1	–	0.8	V

Note) *1. -3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6267-35			HM6267-45/55			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT}=0mA, min. cycle	–	40	100	–	40	80	mA
Stand by Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, min cycle	–	10	20	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} - 0.2V, 0V ≦ V_{IN} ≦ 0.2V or V_{CC} - 0.2V ≦ V_{IN}	–	0.02	2	–	0.02	2	mA
			–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = -4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limts are at V_{CC} = 5V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	—	7	pF	V_{OUT}=0V

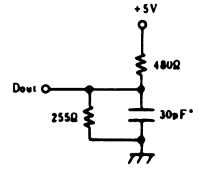
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

● AC TEST CONDITIONS

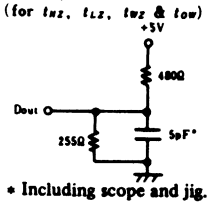
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

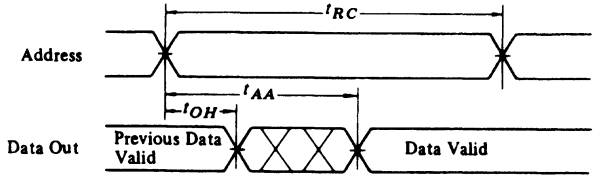


* Including scope and jig.

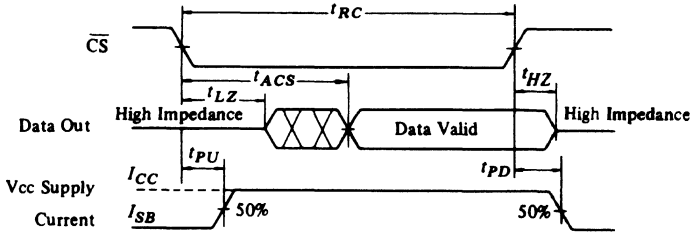
• Read Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	-	45	–	55	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	-	55	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2,3,7
Chip Deselectio to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2,3,7
Chip Selectio to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	–	30	ns	

• TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



• TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

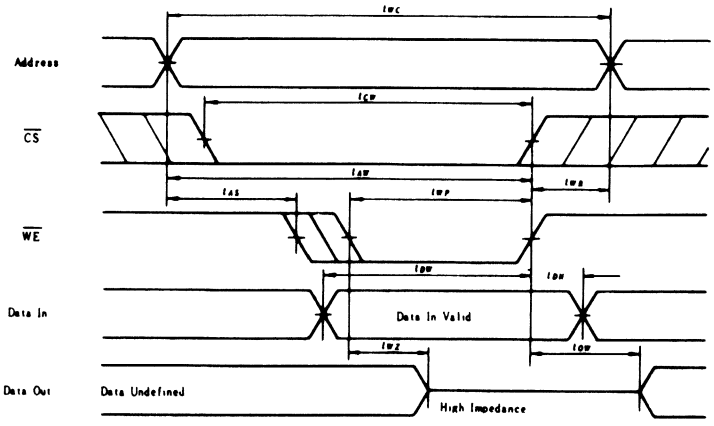


Notes) 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

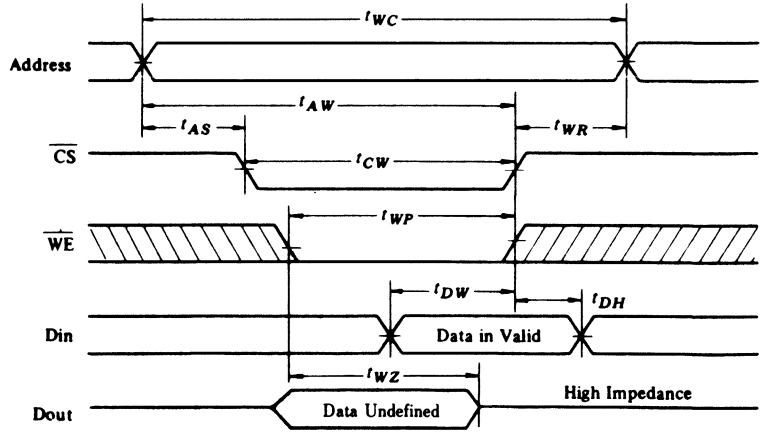
• Write Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	55	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	25	ns	3,4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3,4

● **TIMING WAVEFORM OF WRITE CYCLE NO. 1** ($\overline{WE}$ Controlled)



● **TIMING WAVEFORM OF WRITE CYCLE NO. 2** ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

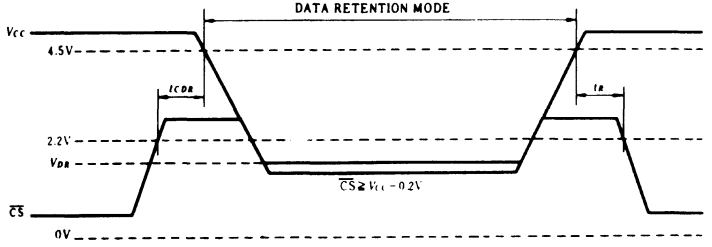
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leq Ta \leq 70°C$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{in} \geq V_{CC} - 0.2V$ or $0V \leq V_{in} \leq 0.2V$	—	—	30*2 20*3	μA
Chip Deselect to Data Retention Time	t_{CDR}	see retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. V_{CC} = 3.0V
*3. V_{CC} = 2.0V

●LOW V_{CC} DATA RETENTION WAVEFORM



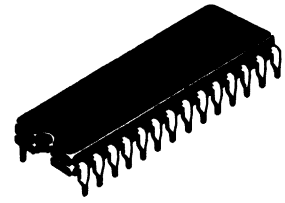
HM6264A Series

8192-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

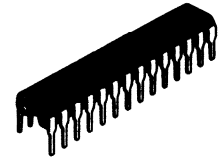
- Low Power Standby — Standby: 0.1mW (typ.) 10μW (typ.) L-/LL-version
- Low Power Operation — Operating: 15mW/MHz (typ.)
- Fast access Time — 100ns/120ns/150ns (max.)
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- . Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/LL-version)

HA6264AP Series



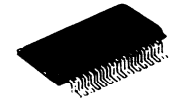
(DP-28)

HM6264ASP Series



(DP-28N)

HM6264AFP Series



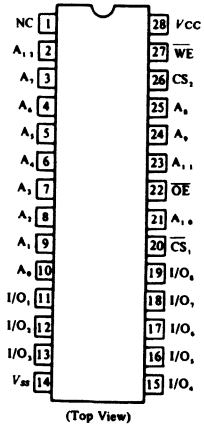
(FP-28D/DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6264AP-10	100ns	600 mil 28 pin Plastic DIP
HM6264AP-12	120ns	
HM6264AP-15	150ns	
HM6264ALP-10	100ns	
HM6264ALP-12	120ns	
HM6264ALP-15	150ns	
HM6264ALP-10L	100ns	
HM6264ALP-12L	120ns	
HM6264ALP-15L	150ns	
HM6264ASP-10	100ns	300 mil 28 pin Plastic DIP
HM6264ASP-12	120ns	
HM6264ASP-15	150ns	
HM6264ALSP-10	100ns	
HM6264ALSP-12	120ns	
HM6264ALSP-15	150ns	
HM6264ALSP-10L	100ns	
HM6264ALSP-12L	120ns	
HM6264ALSP-15L	150ns	
HM6264AFP-10	100ns	28 pin Plastic SOP (Note)
HM6264AFP-12	120ns	
HM6264AFP-15	150ns	
HM6264ALFP-10	100ns	
HM6264ALFP-12	120ns	
HM6264ALFP-15	150ns	
HM6264ALFP-10L	100ns	
HM6264ALFP-12L	120ns	
HM6264ALFP-15L	150ns	

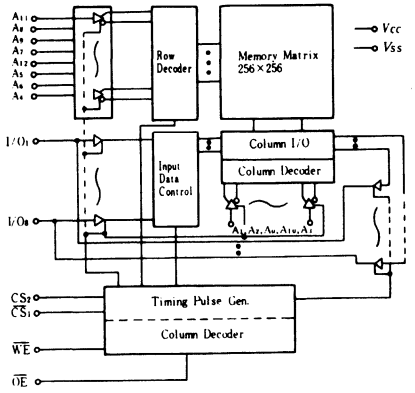
Note) T is added to the end of the type no. for a SOP of 3.00 mm (max.) thickness.

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage*1	V_T	−0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

Notes) *1. With respect to V_{SS}.
*2. −3.0V for pulse width ≦ 50ns

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB},I_{SB1}	
X	X	L	X		High Z	I_{SB},I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read Cycle
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2		6.0	V
	V_{IL}	−0.3*1		0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{in}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, $I_{I/O}$=0mA	–	7	15	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1}=V_{IL}$, CS2=V_{IH} $I_{I/O}$=0mA	–	30	45*5	mA
				30	55*6	
	I_{CC2}	Cycle time = 1μs, duty = 100%, $I_{I/O}$ = 0mA, $\overline{CS1} \leqq 0.2V$, CS2 $\geqq V_{CC}-0.2V$ $V_{IH} \geqq V_{CC}-0.2V$, $V_{IL} \leqq 0.2V$	–	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}	–	1	3	mA
	I_{SB1}*2	$\overline{CS1} \geqq V_{CC}-0.2V$, CS2$\geqq V_{CC}-0.2V$ or 0V $\leqq$ OS2 $\leqq$ 0.2V, 0V $\leqq V_{in}$	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. V_{IL} min=–0.3V
*3. This characteristics is guaranteed only for L-version.
*4. This characteristics is guaranteed only for LL-version.
*5. For 120ns/150ns version.
*6. For 100ns version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

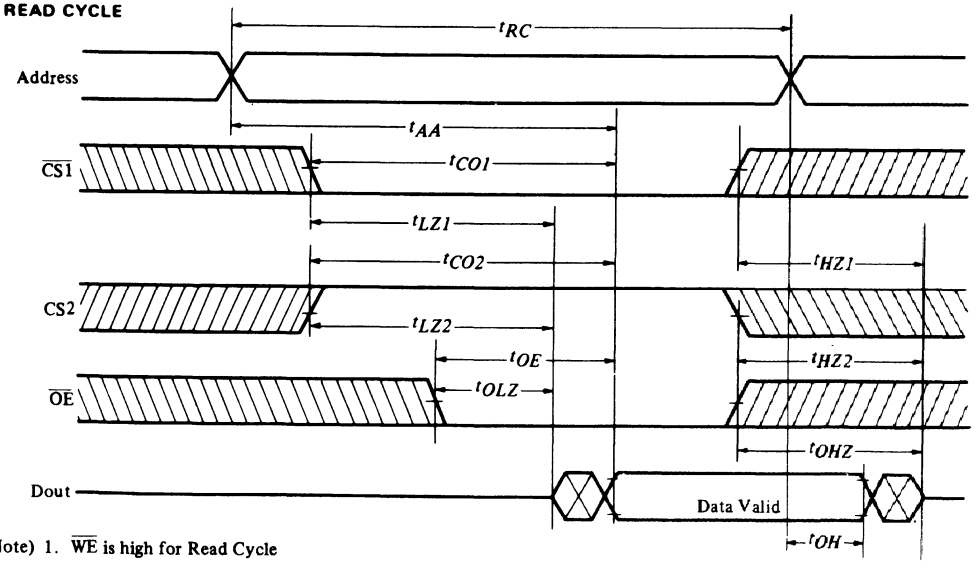
Input Pulse Levels: 0.8V/2.4V
Input Rise and Fall Time: 10ns
Input Timing Reference Level: 1.5V
Output Timing Reference Level: 0.8V/2.0V
Output Timing Reference Level: HM6264A-10 1.5V
HM6264A-12/15 0.8V/2.0V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

• **READ CYCLE**

Item		Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	10	–	ns

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from d device to device.

• **READ CYCLE**

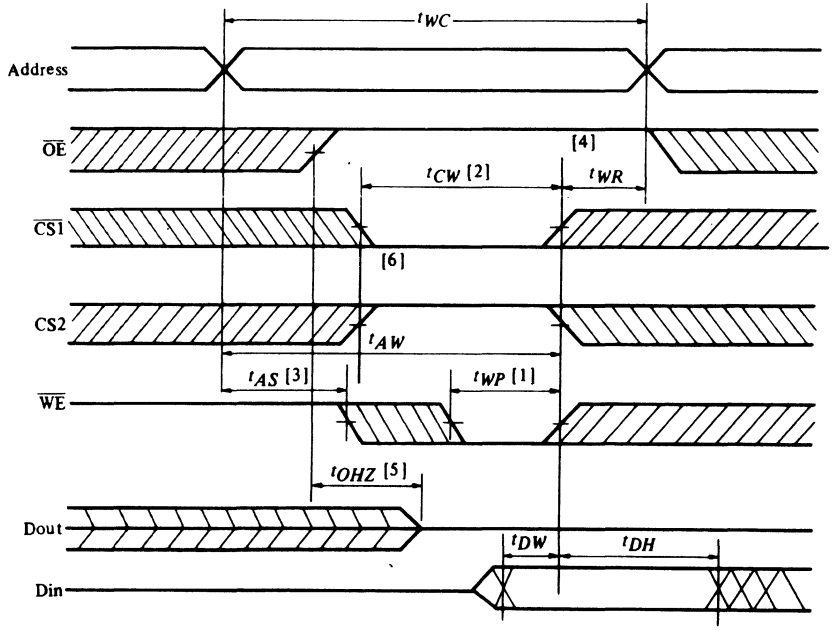


Note) 1. $\overline{WE}$ is high for Read Cycle

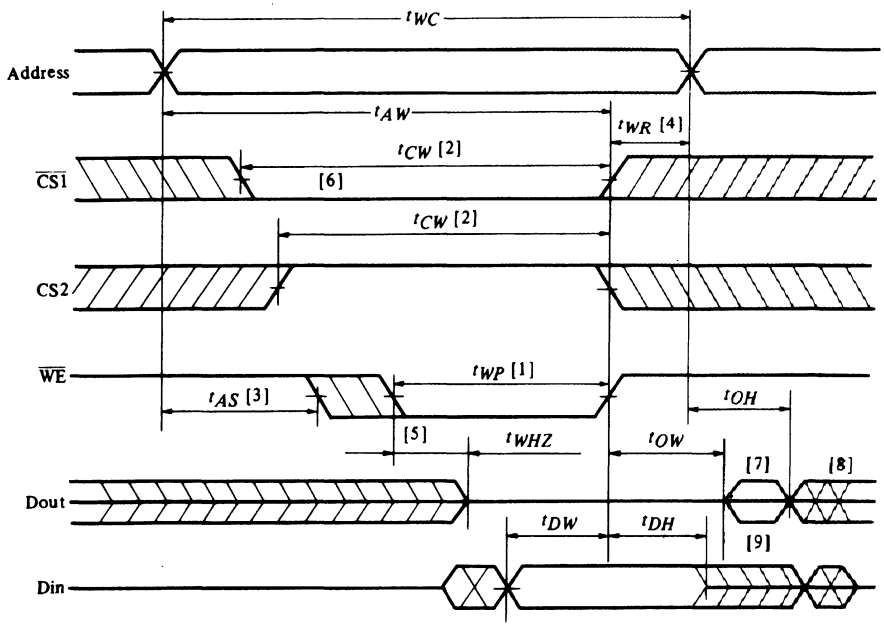
• **WRITE CYCLE**

Item	Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	80	–	85	–	100	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width	t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Enable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

• **WRITE CYCLE (1) ($\overline{OE}$ clock)**



• WRITE CYCLE (2) (OE Low Fix)



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

3) t_{AS} is measured from the address valid to the beginning of write.

4) t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

7) Dout is the same phase of the latest written data in this write cycle.

8) Dout is the read data of next address.

9) If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

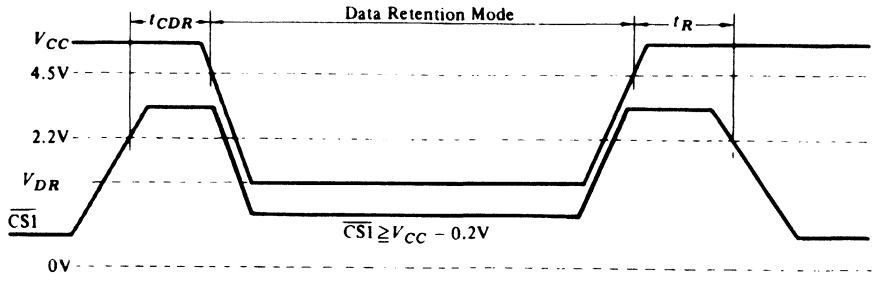
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L/LL-version.

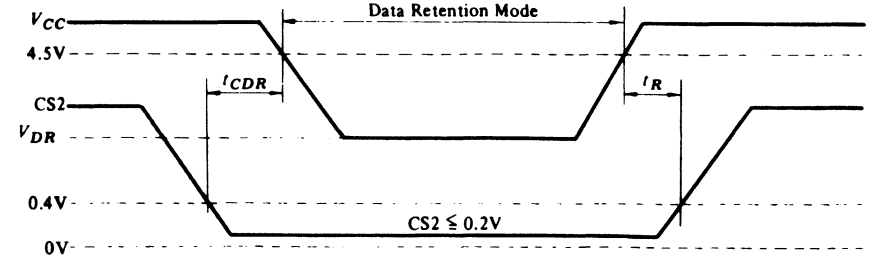
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$	2.0	–	–	V
Data RetentionCurrent	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $0V \leq CS2 \leq 0.2V, 0V \leq V_{in}$	–	1*1	50*1	μA
			–	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*3	–	–	ns

Notes) *1. V_{IL} min = −0.3V, 20μA max at T_a=0 to 40°C, This characteristics is guaranteed only for L-version.
*2. V_{IL} min = −0.3V, 10μA max at T_a = 0 to 40°C, This characteristics is guarnteed only for LL-version.
*3. t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)



Note) In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM6288 Series

16384-word×4-bit High Speed CMOS Static RAM

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6288, packaged in a 300 mil plastic DIP and SOJ, is available for high density mounting. Low power version retains the data with battery back up.

■FEATURES

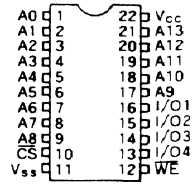
- Single 5V Supply and High Density Plastic Package.
- High Speed: Fast Access Time 25/35/45 ns (max.)
- Low Power dissipation
  - Active mode 300mW (typ.)
  - Standby mode 100μW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6288P-25 HM6288P-35	25ns 35ns	300 mil 22-pin Plastic DIP (DP-22NB)
HM6288LP-25 HM6288LP-35	25ns 35ns	
HM6288JP-25 HM6288JP-35	25ns 35ns	300 mil 24-pin SOJ (CP-24D)
HM6288LJP-25 HM6288LJP-35	25ns 35ns	

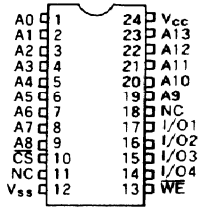
■PIN ARRANGEMENT

- HM6288P Series



(Top View)

- HM6288JP Series

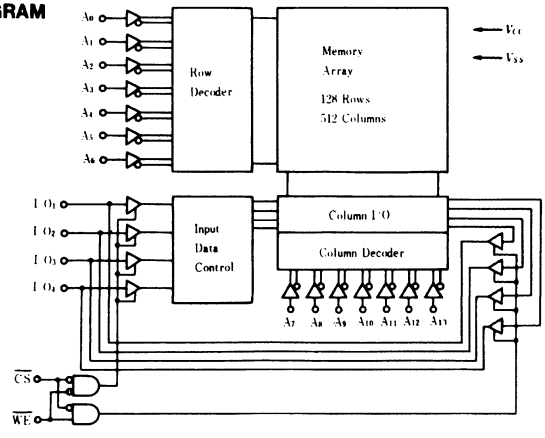


(Top View)

■Pin Description

Pin Name	Function
A0 - A13	Address
I/O1–I/O4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5^{*1} to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note: *1. V_T min. = −2.0V for pulse width ≦ 10ns

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High Z	- -
L	H	Read	I_{CC}	Dout	Read'Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5^{*1}	–	0.8	V

Note: *1. V_{IL} min. = −2.0V for pulse width ≦ 10ns

■DC AND OPERATING CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC}=MAX. V_{IN}=V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, min. cycle	–	60	120	mA
Standby V_{CC} Current	I_{SB}	$\overline{CS}$=V_{IH}, min. cycle	–	15	30	mA
Standby V_{CC} Current 1	I_{SB1}*2	$\overline{CS}$ ≧ V_{CC}−0.2V	–	0.02	2.0	mA
	I_{SB1}*3	0V ≦ V_{IN} ≦ 0.2V or V_{CC}−0.2V ≦ V_{IN}	–	0.02	0.1	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−4.0mA	2.4	–	–	V

Notes: *1. Typical limits are at V_{CC}=5.0V, Ta=+25°C and specified loading.
*2. P version
*3. LP version

■CAPACITANCE (Ta=25°C, f=1.0MHz)

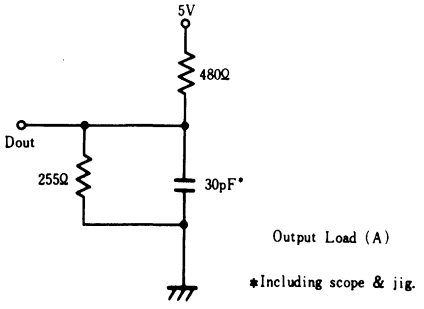
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note: This parameter is sampled and not 100% tested

■AC CHARACTERISTICS

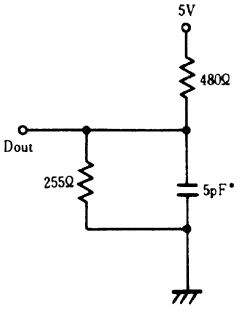
- AC Test Conditions

Input pulse levels: 0V to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure



Output Load (A)

*Including scope & jig.



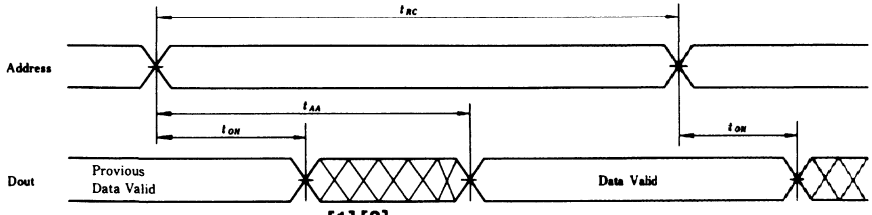
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

■ READ CYCLE

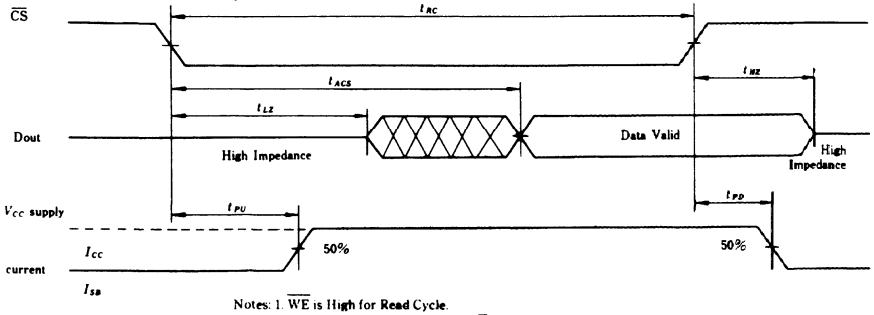
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	ns
Address Access Time	t_{AA}	–	25	–	35	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	ns
Output Hold from Address Change	t_{OH}	3	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Seselection to Power Down Time	t_{PD}	–	25	–	30	ns

* Transition is measured ±200mV from steady state voltage with Load(B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No.1 [1] [2]



● Timing Waveform of Read Cycle No.2 [1] [3]



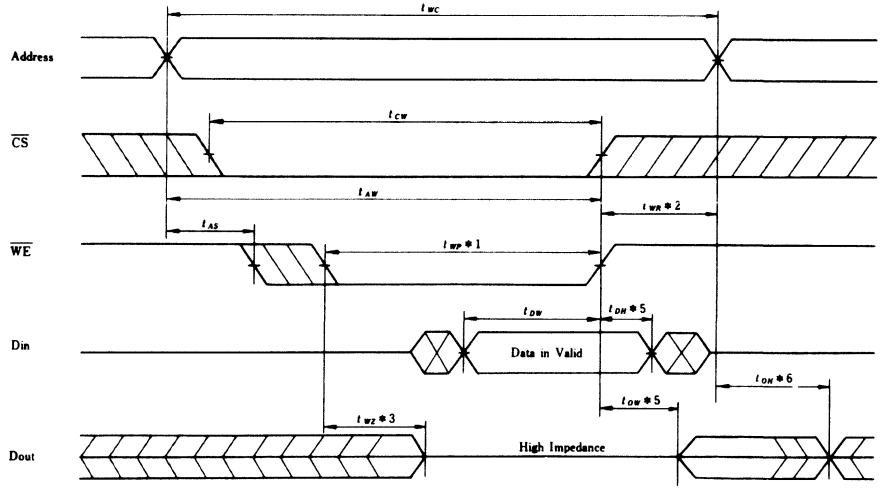
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

■ WRITE CYCLE

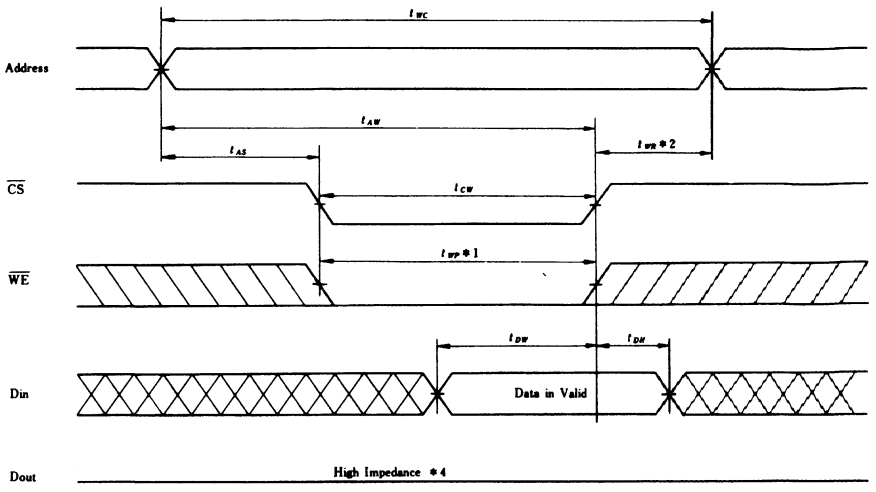
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Date Valid to End of Write	t_{DW}	12	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WZ}*	0	8	0	10	ns
Output Active from End of Write	t_{OW}*	5	–	5	–	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 ($\overline{WE}$ Controlled)



● Timing Waveform of Write Cycle No.2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

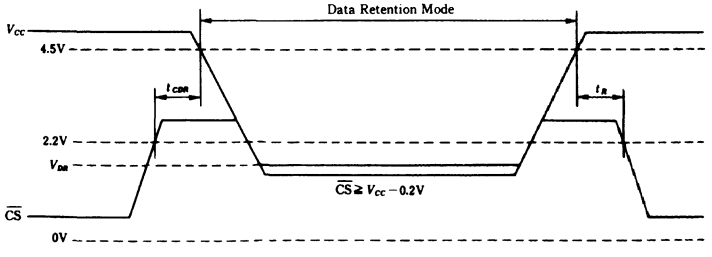
● Low *Vcc* Data Retention Characteristics ($Ta = 0$ to $+70°C$)

(This Characteristics is guaranteed only for L-version.)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$
Data retention current	I_{CCDR}	–	–	50[2] 35[3]	μA	$V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[1]	–	–	ns	

NOTE : 1. t_{RC} = Read cycle time
2. $V_{CC} = 3.0V$
3. $V_{CC} = 2.0V$

Low *Vcc* Data Retention Waveform



HM6289 Series

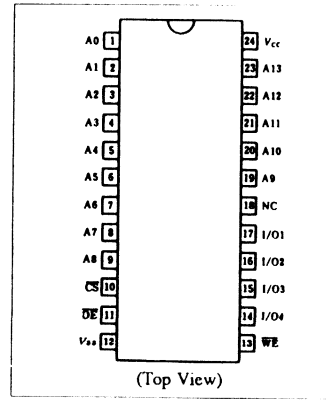
16384-Word × 4-Bit High Speed CMOS Static RAM (with $\overline{OE}$)

The Hitachi HM6289 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. Low power version retains the data with battery back up.

Pin Arrangement



(Top View)

Features

- High speed
  - Access time:
    - t_{AA}: 25/35 ns (max)
    - t_{OE}: 12/15 ns (max)
- High density 24-pin SOJ package
- Low power
  - Active mode: 300 mW (typ)
  - Standby mode: 100 µW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

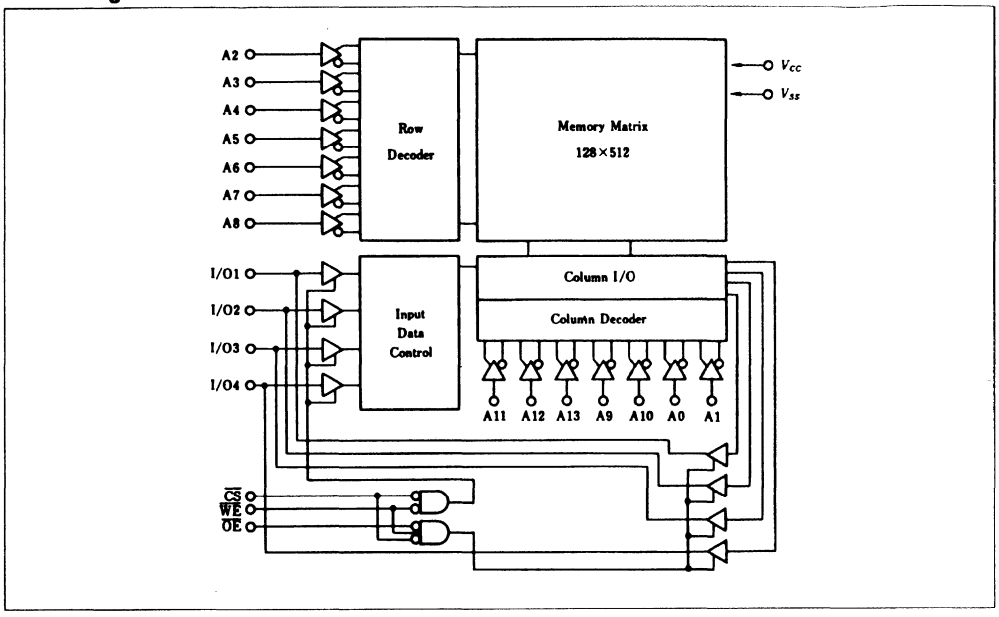
Ordering Information

Type No.	Access Time	Package
HM6289JP-25	25 ns	300-mil
HM6289JP-35	35 ns	24-pin
HM6289LJP-25	25 ns	SOJ
HM6289LJP-35	35 ns	(CP-24D)

Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O pin	Ref. Cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	Icc	Dout	Read cycle (1)–(3)
L	H	L	Write	Icc	Din	Write cycle (1)–(2)
L	L	L	Write	Icc	Din	Write cycle (3)–(6)

Note: ×; H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{in}	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +85	°C

Note: *1. Vin min = −2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = 0V to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0 V to Vcc
Operating Vcc current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. cycle
Standby Vcc current (1)	I_{SB1}*2	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V
	I_{SB1}*3	—	0.02	0.1	mA	0V ≤ Vin ≤ 0.2 V or Vcc – 0.2 V ≤ Vin
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. P-version
*3. LP-version

Capacitance (Ta = 25°C, f = 1MHz)

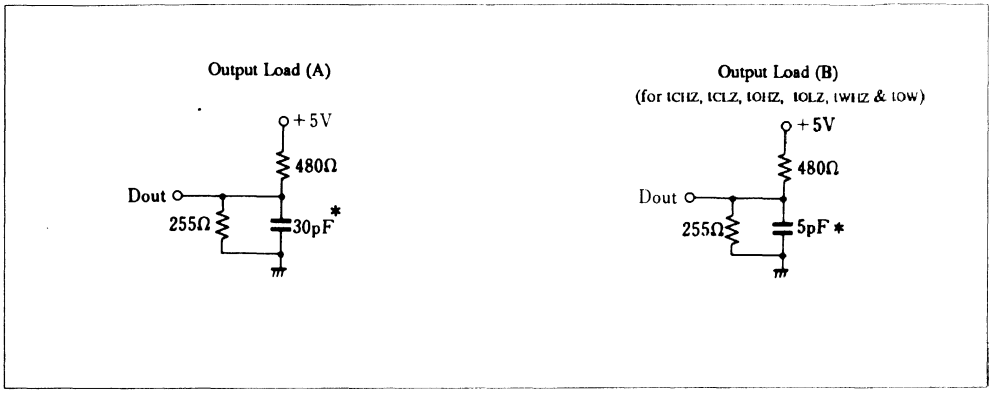
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	V I/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures



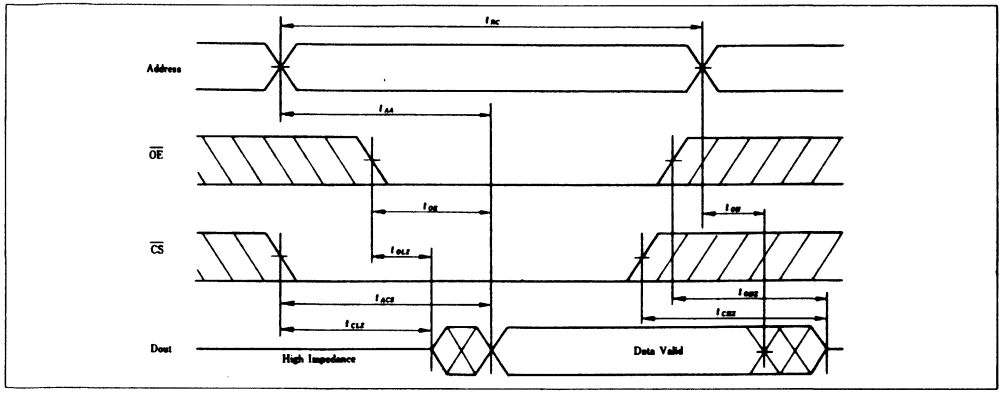
Note: * Including scope & jig.

Read Cycle

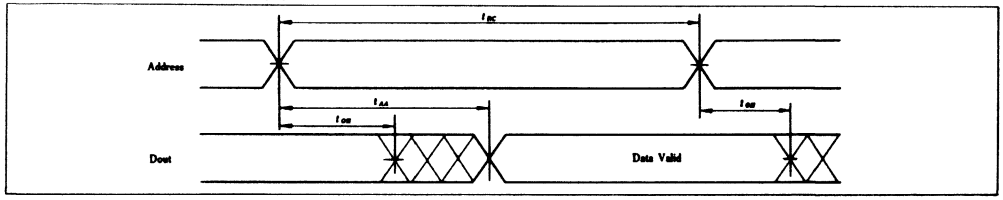
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	12	0	20	ns
Chis disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Note: *1. Output transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

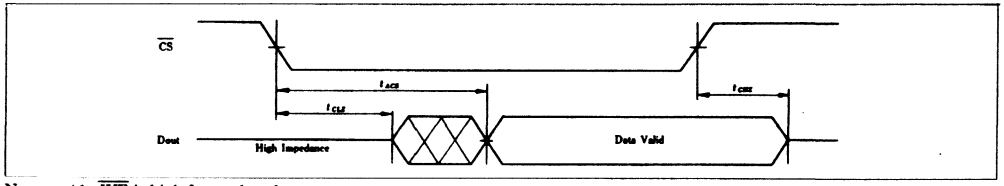
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1,*2,*4



Read Timing Waveform (3) *1,*3,*4



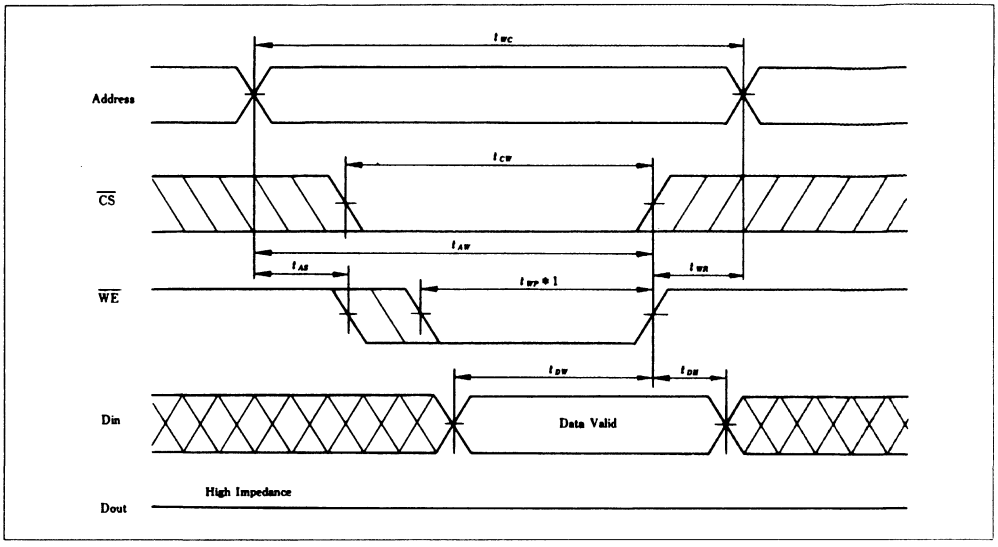
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

Write Cycle

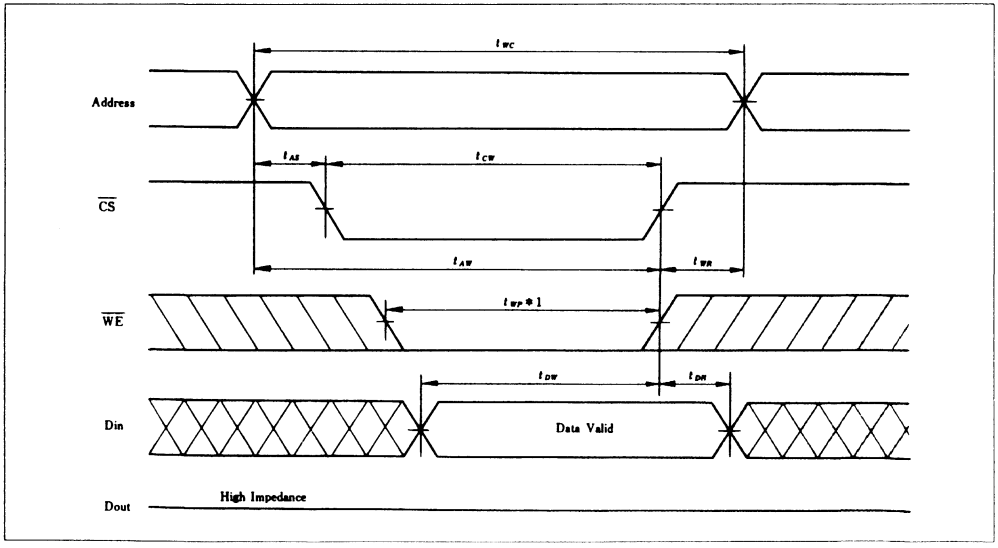
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	10	0	10	ns
Write to output in high-Z*1	t_{WHZ}	0	8	0	10	ns
Data to write time overlap	t_{DW}	12	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write*1	t_{OW}	5	—	5	—	ns

Note: *1. Output transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

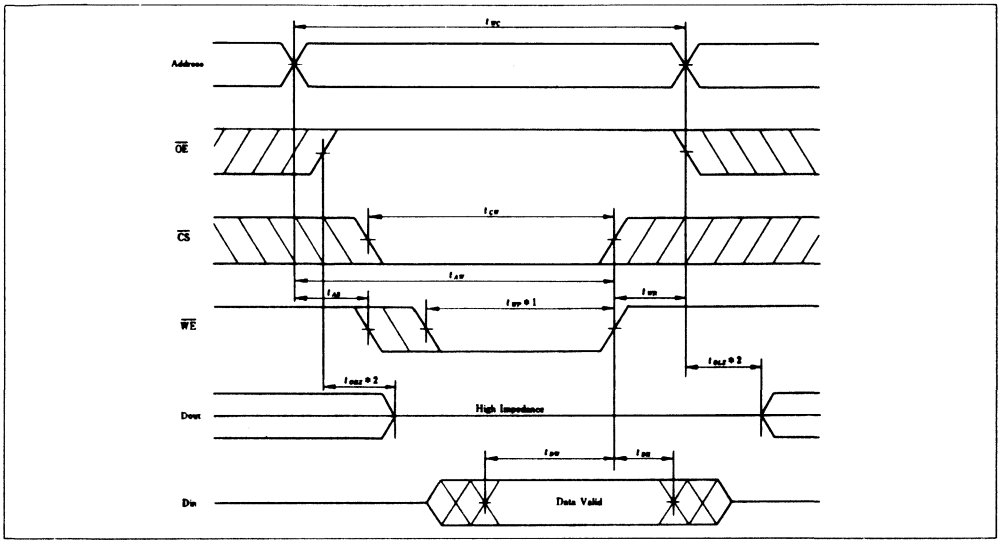
Write Timing Waveform (1) ($\overline{OE}$ = High, $\overline{WE}$ = Controlled)



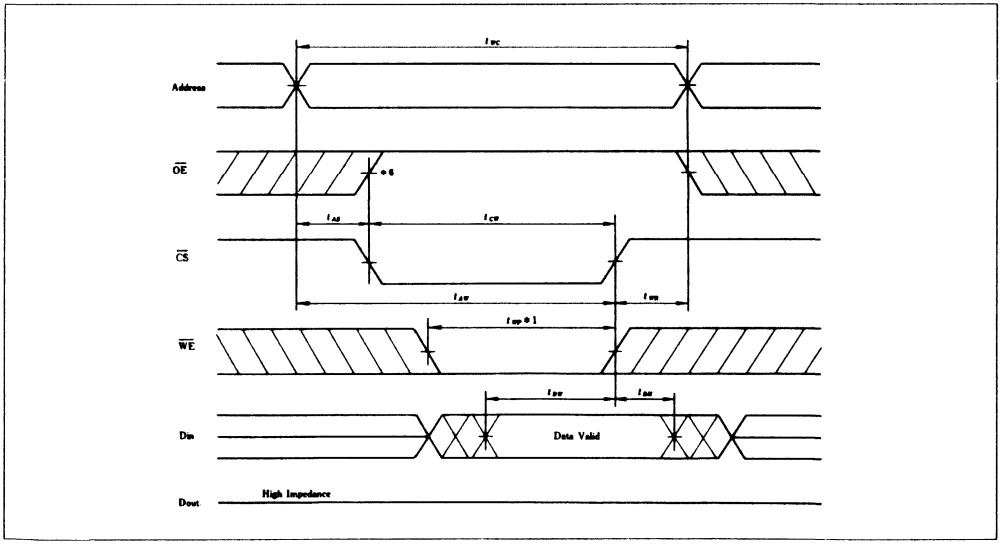
Write Timing Waveform (2) ($\overline{OE}$ = High, $\overline{CS}$ = Controlled)



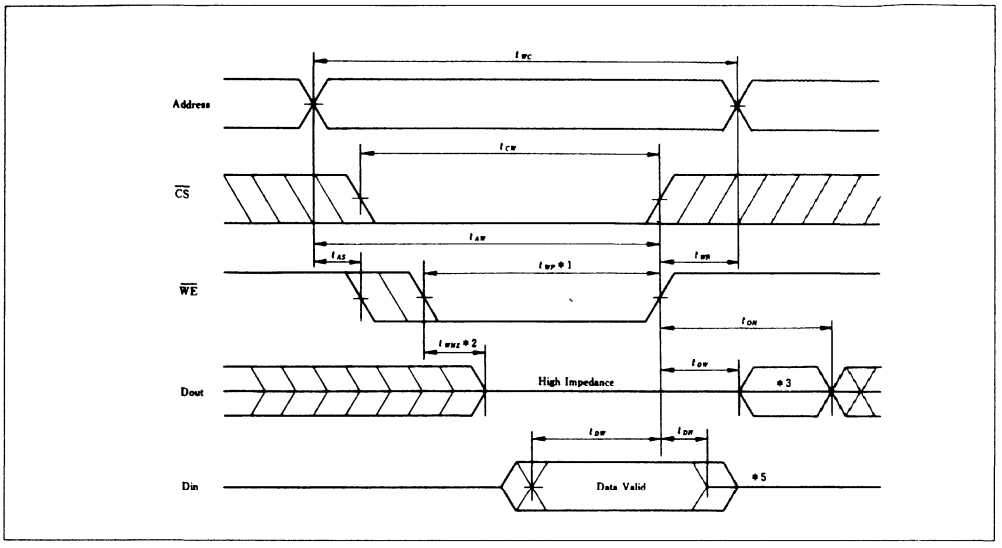
Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ = Controlled)



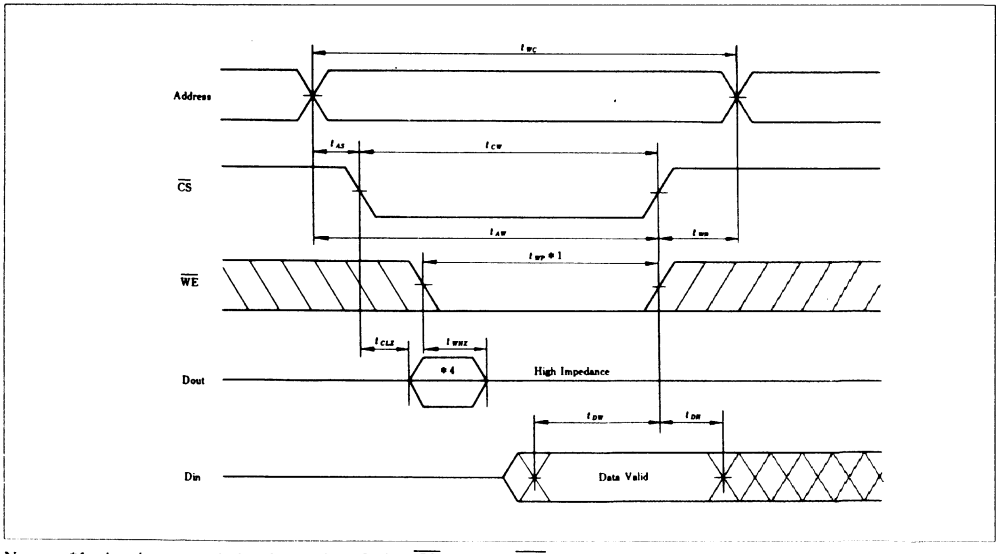
Write Timing Waveform (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ = Controlled)



Write Timing Waveform (5) ($\overline{OE}$ = Low, $\overline{WE}$ = Controlled)



Write Timing Waveform (6) ($\overline{OE}$ = Low, $\overline{CS}$ = Controlled)



Notes:
- *1 A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (tWP)
- *2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
- *3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- *4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
- *5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tOW. Then the data input signals of opposite phase to the outputs must not be applied to them.
- *6. Dout is the same phase of write data of this write cycle, if tWR is long enough.
- *7. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

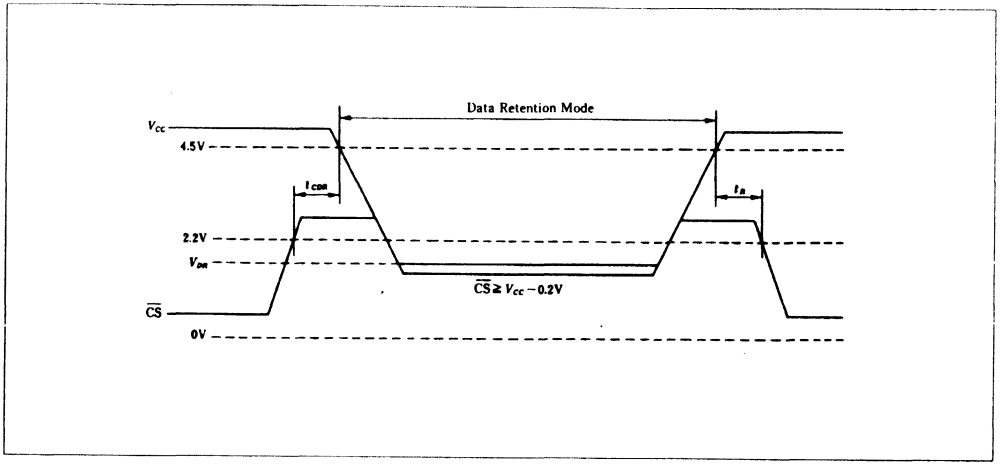
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V,
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Note: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

Low Vcc Data Retention Waveform

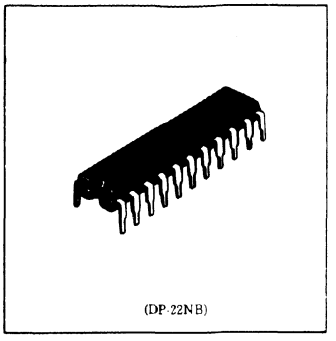


HM6788 Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

■FEATURES

- Super Fast Access Time : 25/30ns (max.)
- Low power Operation
  Operating: 230mW (typ), Standby: 10mW (typ)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe required
- Fully TTL compatible Input and Output

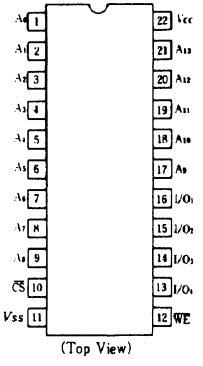


(DP-22NB)

■ORDERING INFORMATION

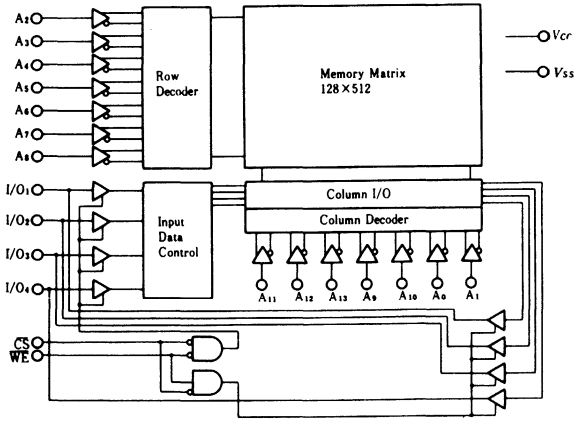
Type No.	Access Time	Package
HM6788P-25	25ns	300 mil 22 pin Plastic DIP
HM6788P-30	30ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2)

×: H or L

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 20ns pulse width.

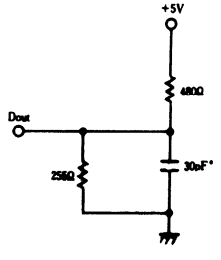
■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	80	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}=0mA$	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–		30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.5	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

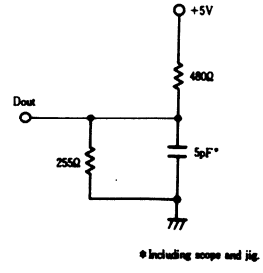
■AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

Input pulse levels: V_{SS} to 3.0V
Input rise and fall time: 4ns
Input and Output reference levels: 1.5V
Output Load: See Figure



Output Load A



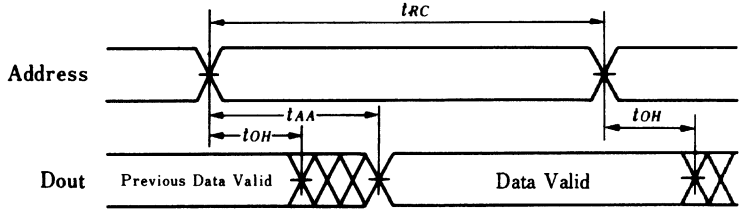
Output Load B
(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW})

● READ CYCLE

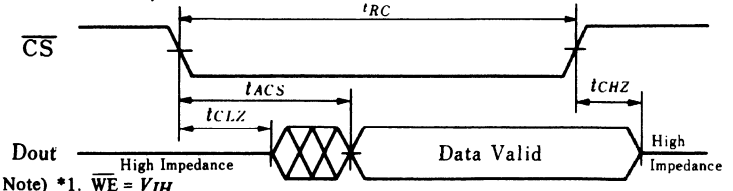
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Address Access Time	t_{AA}	—	25	—	30	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	ns
Chip Selection to Output in Low Z	t_{CLZ} *2	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ} *2	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time*1	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time*1	t_{PD}	—	20	—	30	ns
Input Voltage Rise/Fall Time*3	t_r	—	150	—	150	ns

Notes) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV form steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*3. Please contact your nearest Hitachi's Sale Dept. regarding specification.

● Timing waveform of Read Cycle No. 1 *1,*2



● Timing waveform of Read Cycle No. 2*1,*3



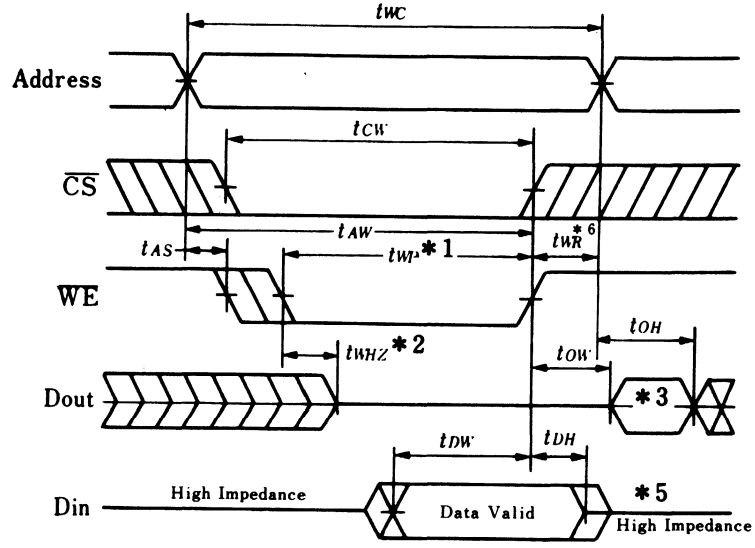
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

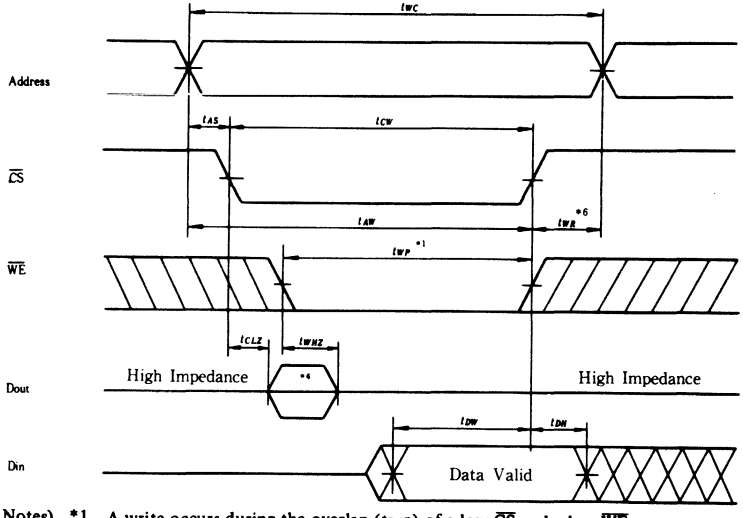
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	20	—	25	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	20	—	25	—	ns
Write Pulse Width	t_{WP}	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High Z	t_{WHZ} *1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	—	15	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Output Active from End of Write	t_{OW} *1	0	—	0	—	ns

*1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Dout is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
*6. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	8.0	V_{OUT}=0V

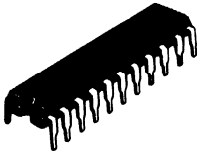
Note) This parameter is sampled and not 100% tested.

HM6788H Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 15/20ns (max.)
- Low power Operation
  Operating: 280mW (typ)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe required
- Fully TTL compatible Input and Output

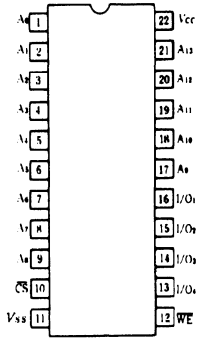


(DP-22NB)

Ordering Information

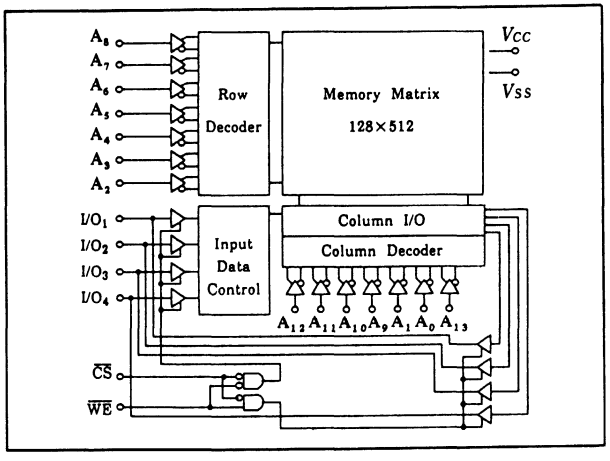
Type No.	Access Time	Package
HM6788HP-15	15ns	300 mil 22 pin Plastic DIP
HM6788HP-20	20ns	

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1), (2)

×: H or L

Recommended DC Operating Conditions ($0°C \leq Ta \leq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 10ns pulse width.

DC and Operating Characteristics ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	10	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}=0mA$	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	–	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

AC Characteristics (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

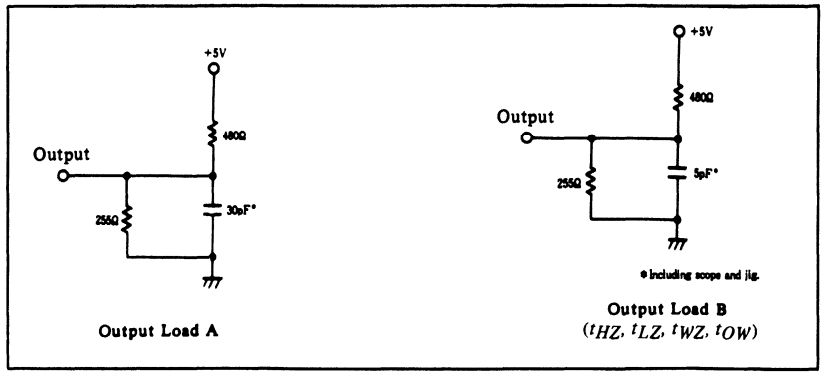
- **AC Test Conditions**

  Input pulse levels: V_{SS} to 3.0V

  Input rise and fall time: 4ns

  Input and Output reference levels: 1.5V

  Output Load: See Figure



Output Load A

Output Load B

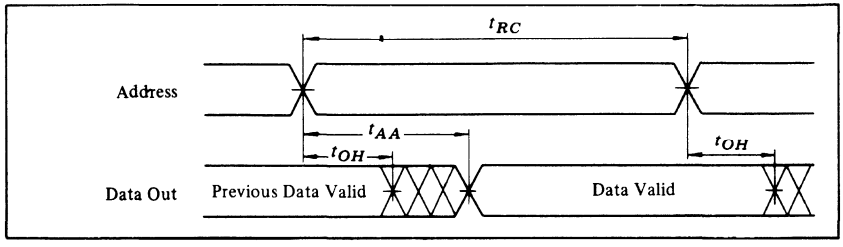
(t_{HZ}, t_{LZ}, t_{WZ}, t_{OW})

Read Cycle

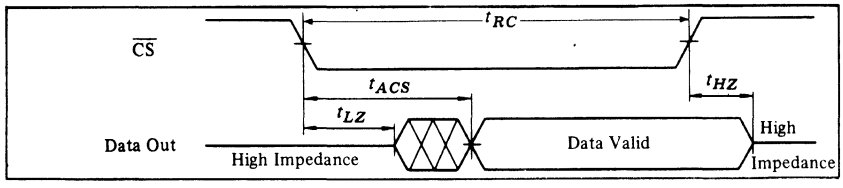
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	

Note) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

- **Timing waveform of Read Cycle No. 1*1,*2**



- **Timing waveform of Read Cycle No. 2*1,*3**



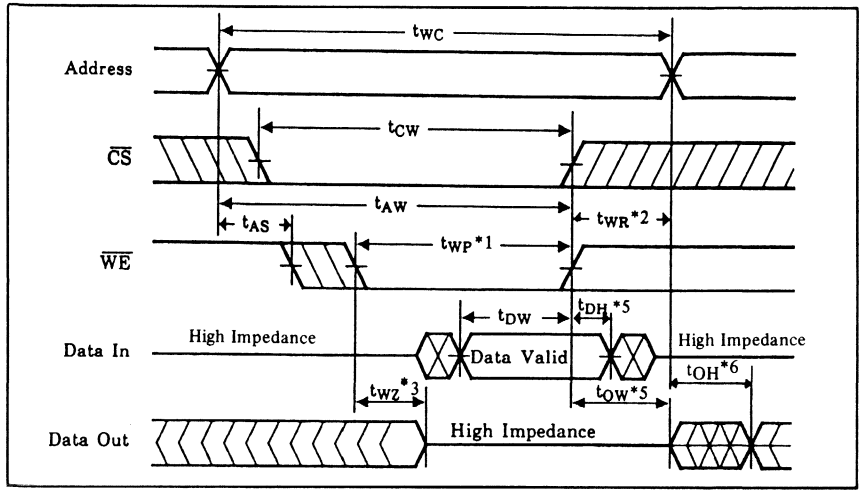
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

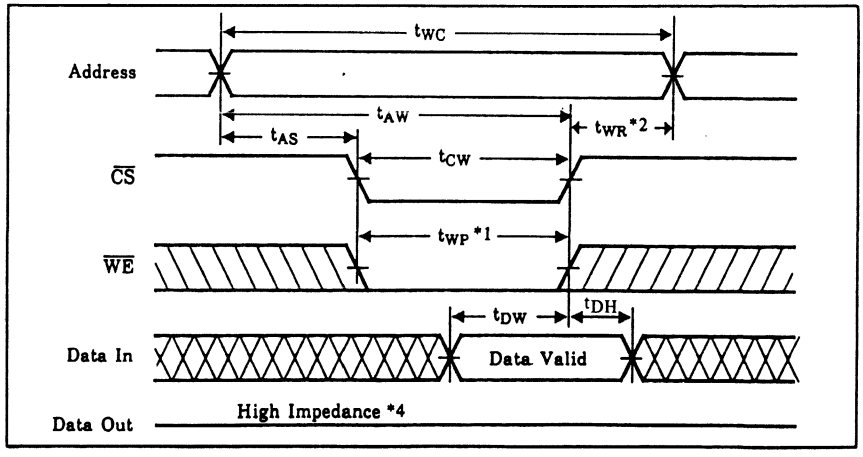
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	1	–	1	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Data Valid to End of Write	t_{DW}	9	–	10	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).
4. This parameter is sampled and not 100% tested.

- **Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)**



- **Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)**



Note)*1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

*6. Data Out is the same phase of write data of this write cycle.

Capacitance (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	$V_{I/O}$=0V

Note) This parameter is sampled and not 100% tested.

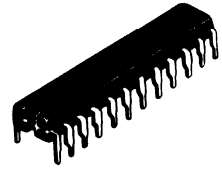
HM6789 Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

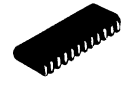
- Super Fast Access Time:. . . . . 25/30 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 230 mW (typ.)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe required
- Fully TTL Compatible Input and Output

HM6789P Series



(DP-24NC)

HM6789JP Series

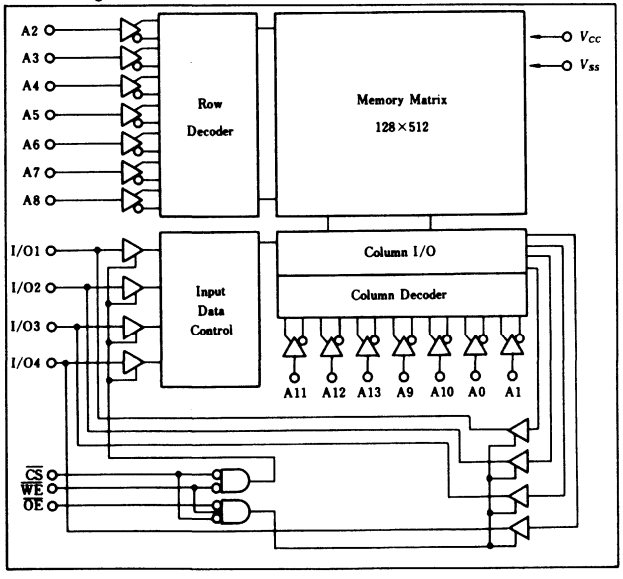


(CP-24D)

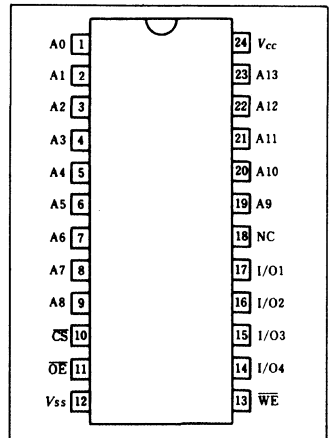
Ordering Information

Type No.	Access Time	Package
HM6789P-25	25ns	300 mil 24 pin
HM6789P-30	30ns	Plastic DIP
HM6789JP-25	25ns	300 mil 24 pin
HM6789JP-30	30ns	Plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 20ns.

Function Table

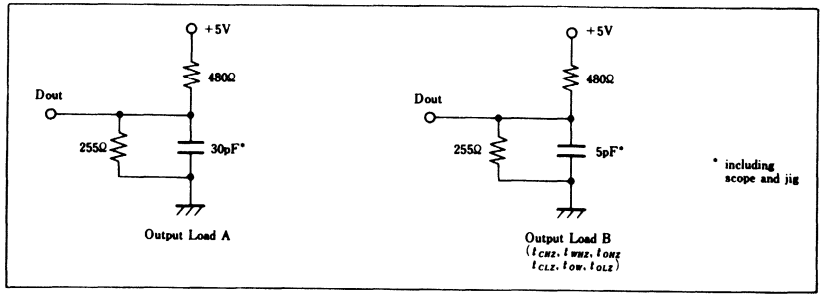
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Din	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} – 0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} – 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	8	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

- Read Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	0	–	0	–	ns
Output Enable to Output Valid	t_{OE}	0	15	0	15	ns
Output Enable to Output in Low Z	t_{OLZ}*1	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Input Voltage Rise/Fall Time	t_T*2	–	150	–	150	ns

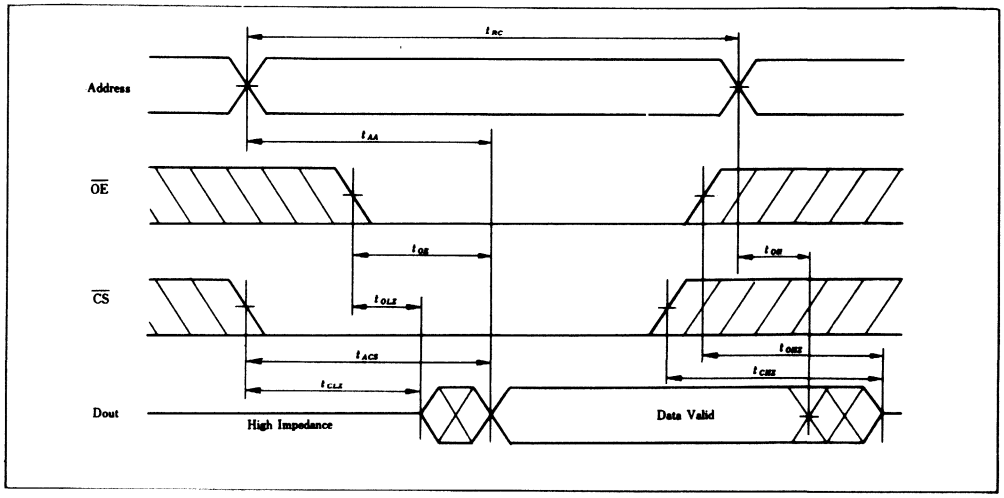
- Write Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	30	–	ns
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	20	–	25	–	ns
Write Pulse Width	t_{WP}	20	–	25	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}*1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	–	20	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Output Disable to Output in Hihg Z	t_{OHZ}*1	0	10	0	10	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

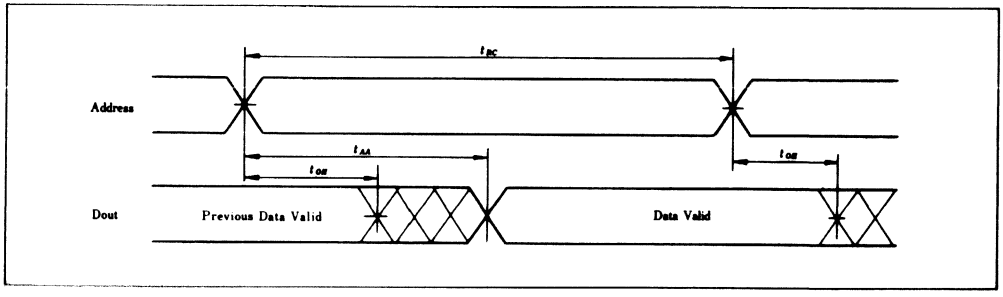
Notes) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.
*2. Please contact your nearest Hitach's Sale Dept. regarding specification.

- Timing Waveform

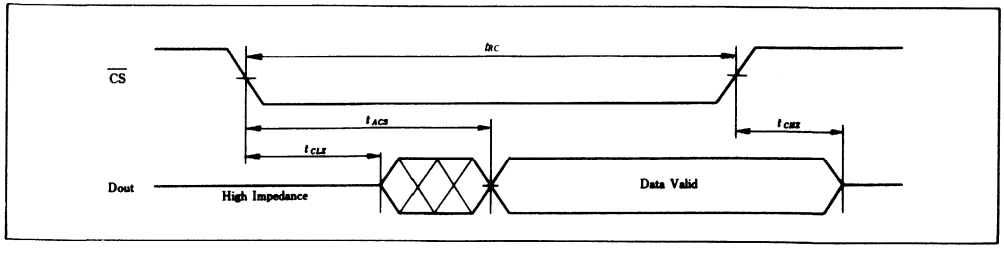
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

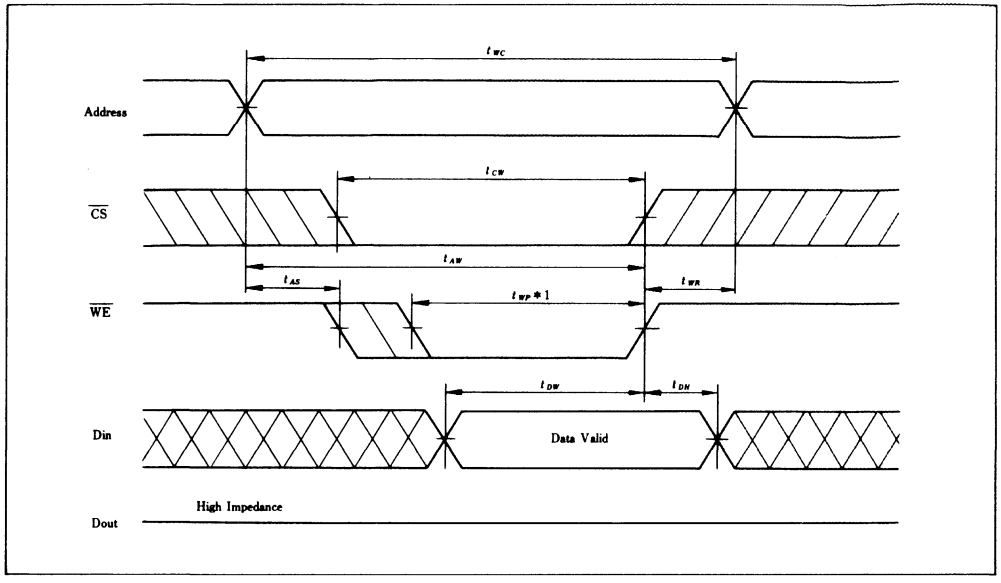


Read Cycle (3) *1, *3, *4

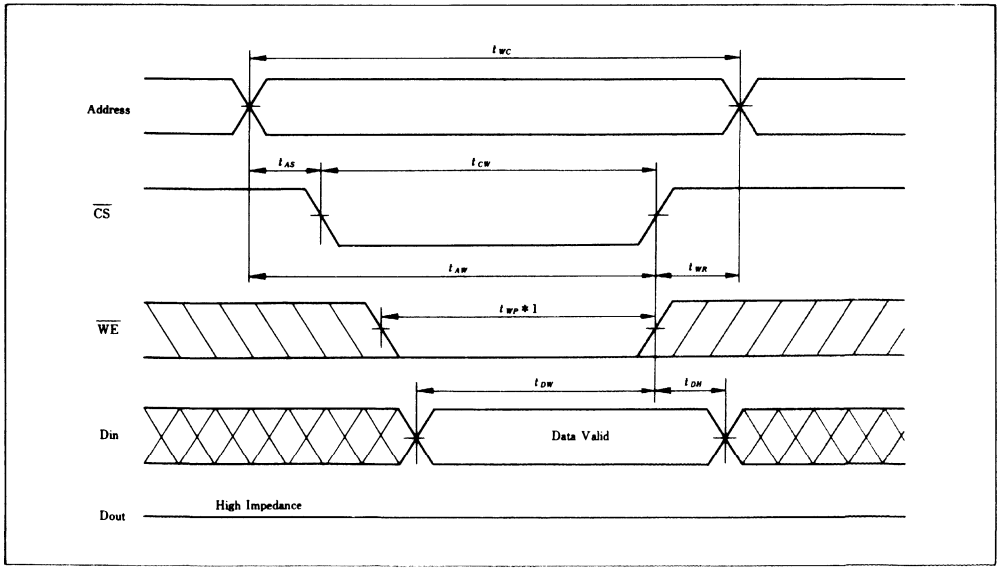


Notes) *1. $\overline{WE}$ = V_{IH}
*2. $\overline{CS}$ = V_{IL}
*3. $\overline{OE}$ = V_{IL}
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

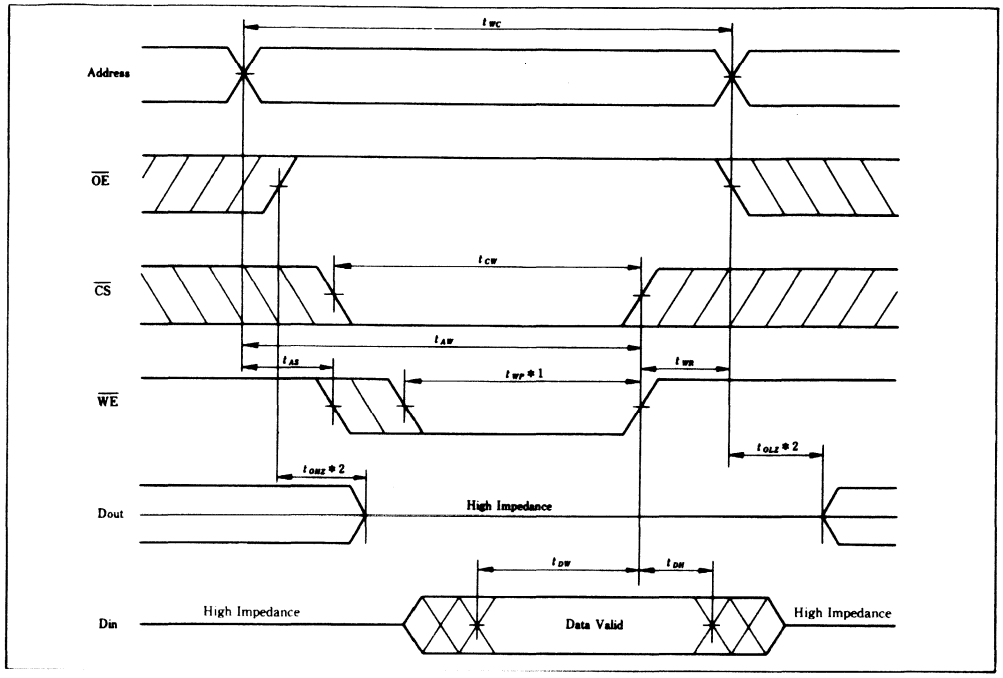
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



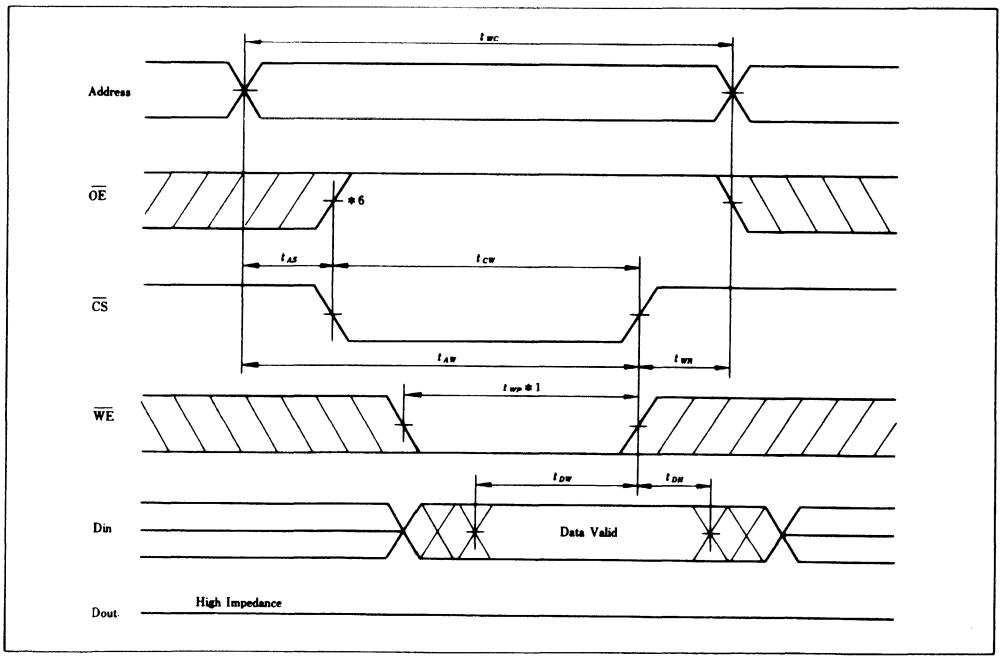
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



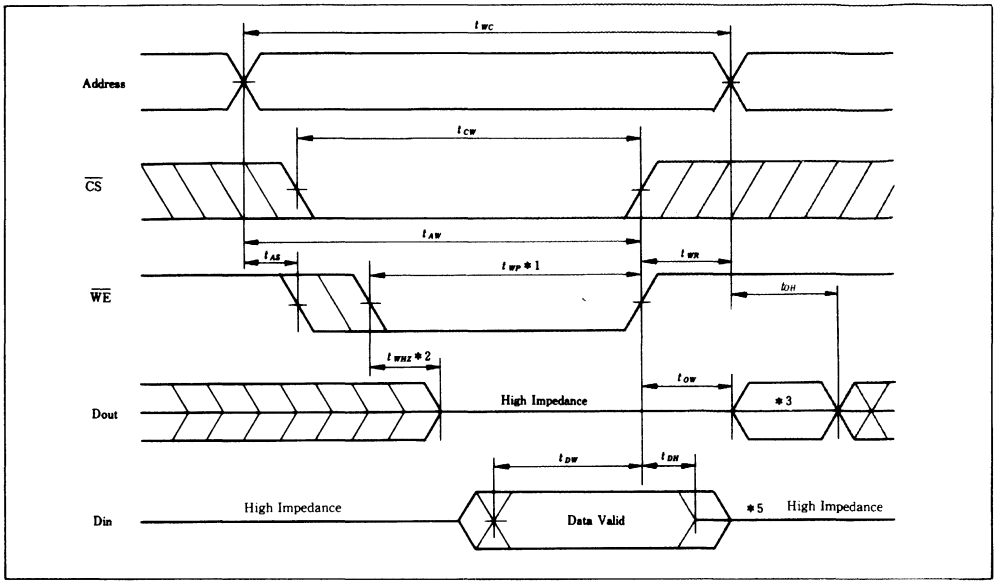
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



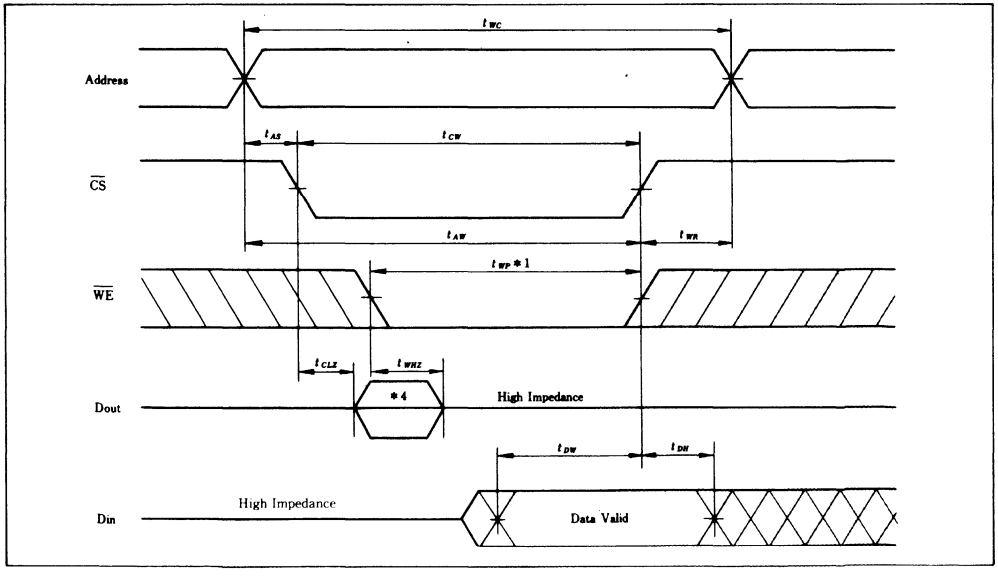
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3. Dout is the same phase of write data of this write cycle.

*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

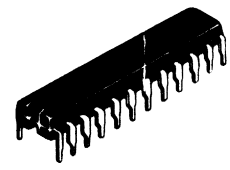
HM6789H Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

- Super Fast Access Time: . . . . . 15/20 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 280 mW (typ.)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe required
- Fully TTL Compatible Input and Output

HM6789HP Series



(DP-24NC)

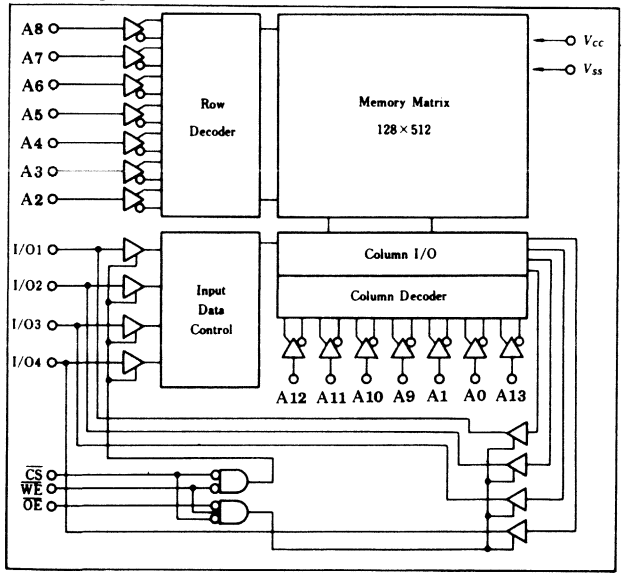
HM6789HJP Series

(CP-24D)

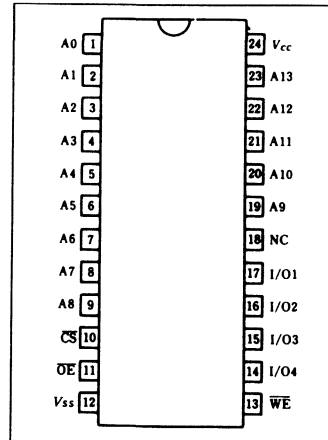
Ordering Information

Type No.	Access Time	Package
HM6789HP-15	15ns	300 mil 24 pin
HM6789HP-20	20ns	plastic DIP
HM6789HJP-15	15ns	300 mil 24 pin
HM6789HJP-20	20ns	plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 10ns.

Function Table

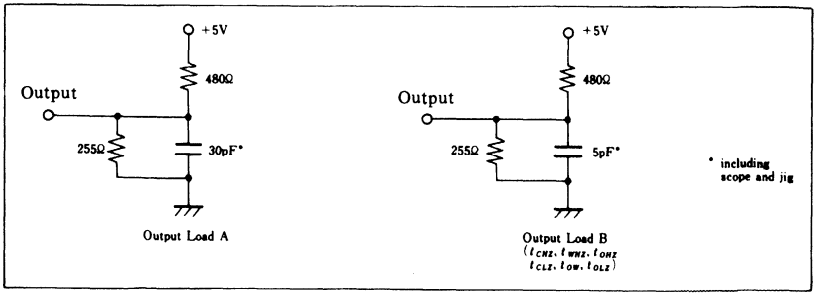
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data Out	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} − 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	15	–	20	–	ns
Address Access Time	t_{AA}	–	15	–	20	ns
Chip Select Access Time	t_{ACS}	–	15	–	20	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	3	–	3	–	ns
Output Enable to Output Valid	t_{OE}	0	12	0	12	ns
Output Enable to Output in Low Z	t_{OLZ}*1	3	–	3	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	6	0	8	ns
Output Hold from Address Change	t_{OH}	3	–	3	–	ns

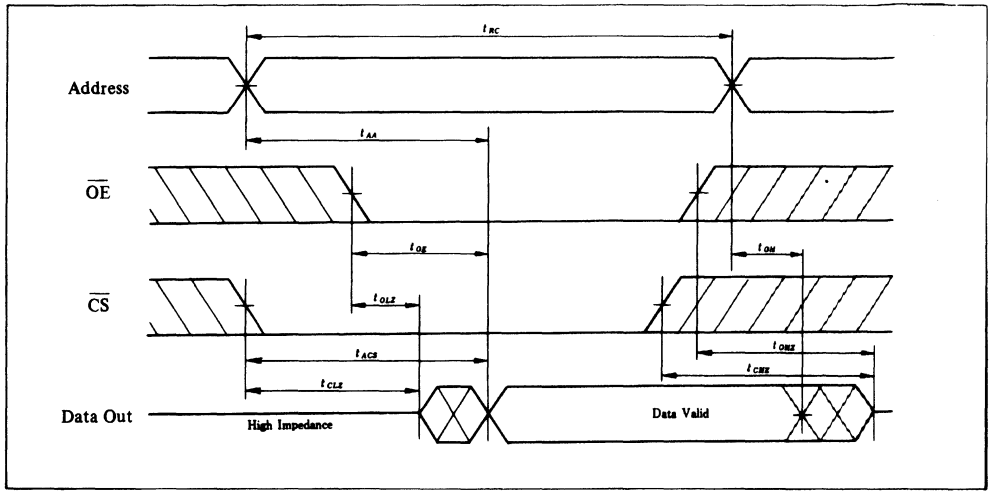
Write Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	15	–	20	–	ns
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	10	–	15	–	ns
Write Pulse Width	t_{WP}	10	–	15	–	ns
Write Recovery Time	t_{WR}	1	–	1	–	ns
Write to Output in High Z	t_{WHZ}*1	0	6	0	8	ns
Data Valid to End of Write	t_{DW}	9	–	10	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}*1	0	6	0	8	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

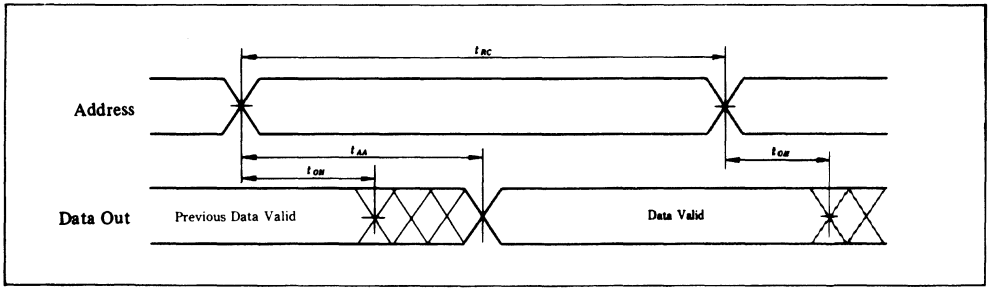
Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Timing Waveform

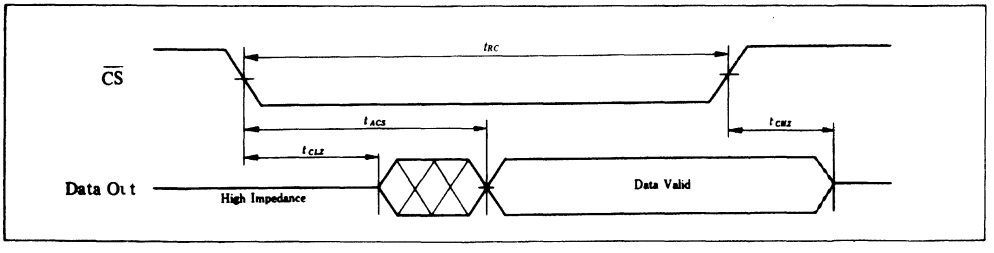
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

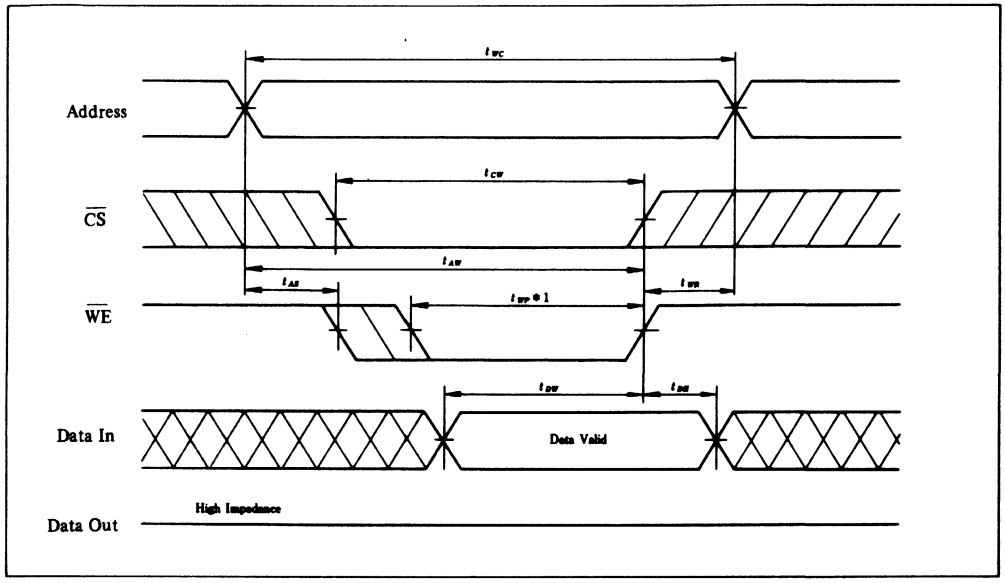


Read Cycle (3) *1, *3, *4

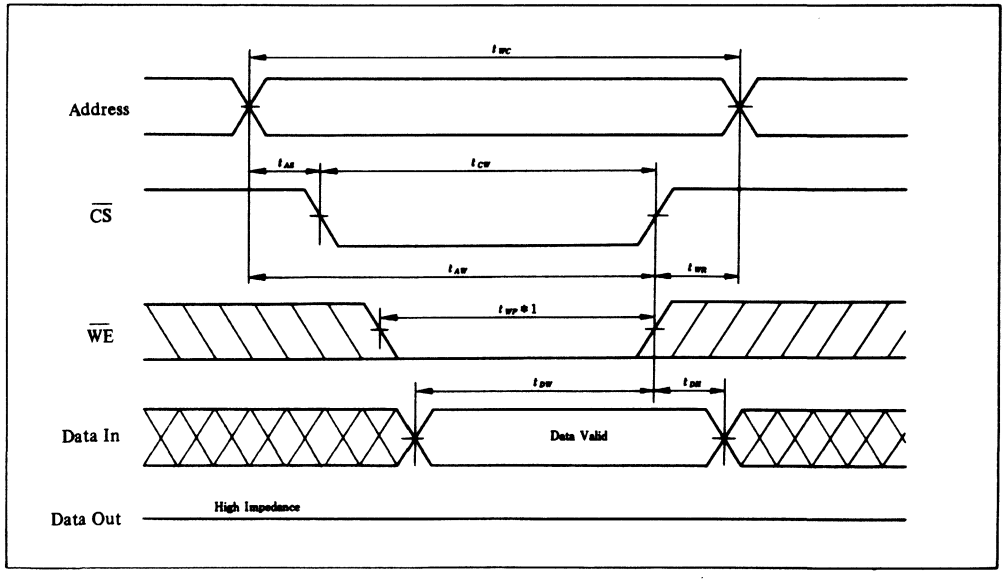


Notes) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. $\overline{OE} = V_{IL}$
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

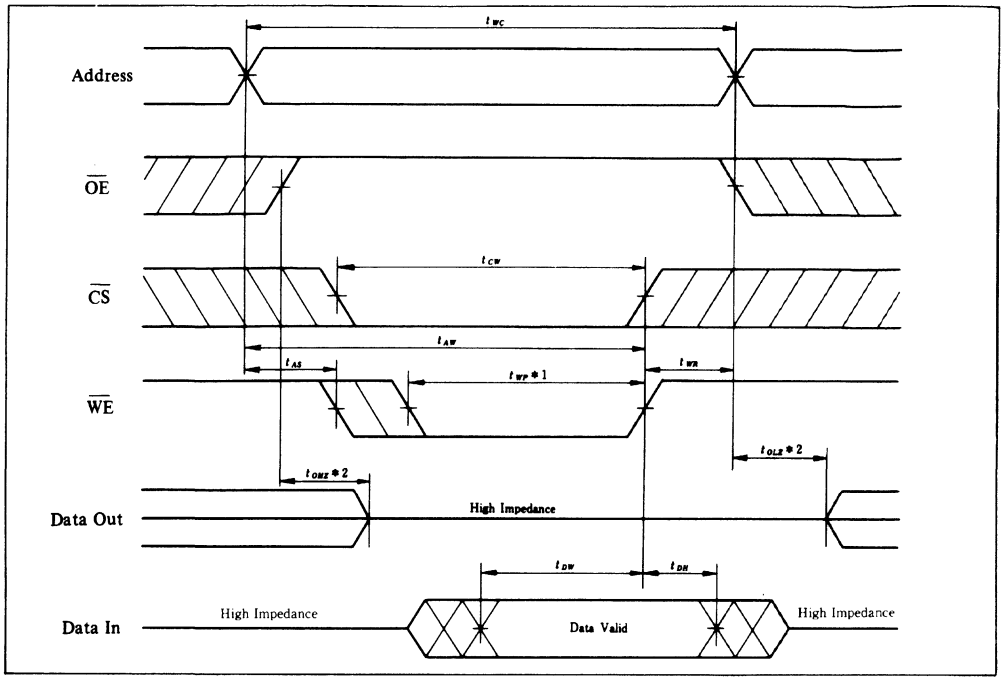
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



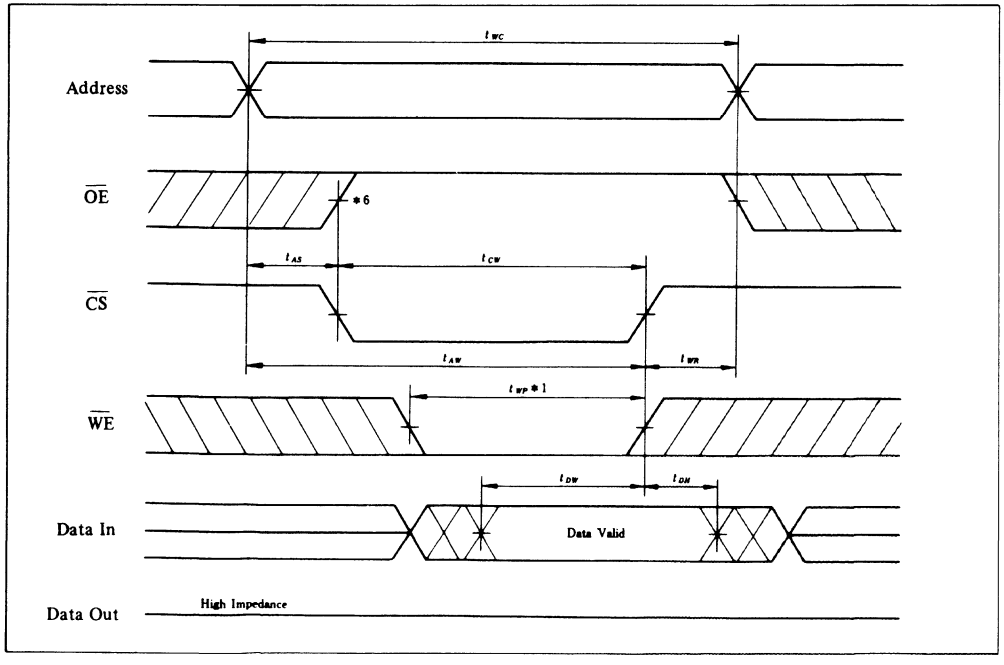
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



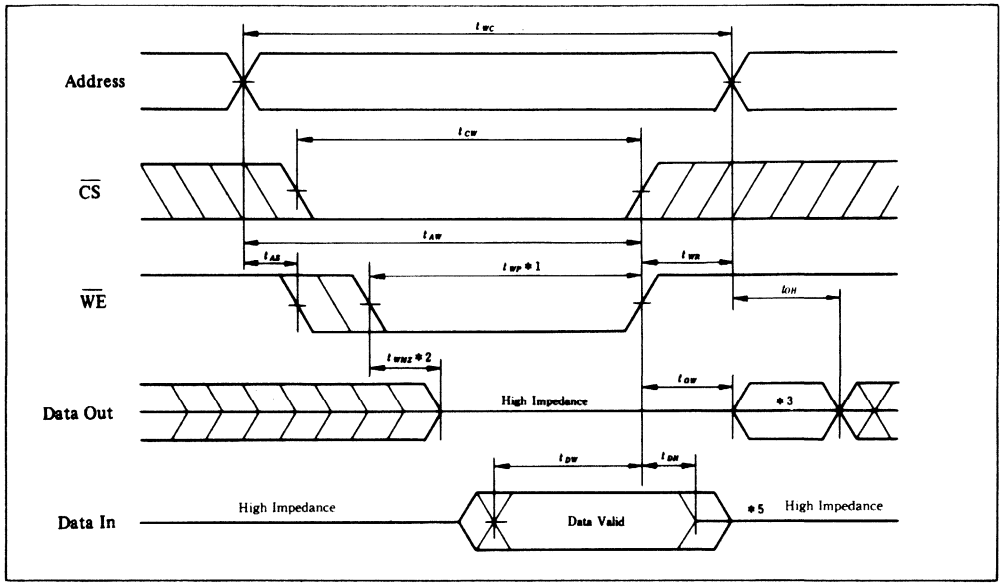
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



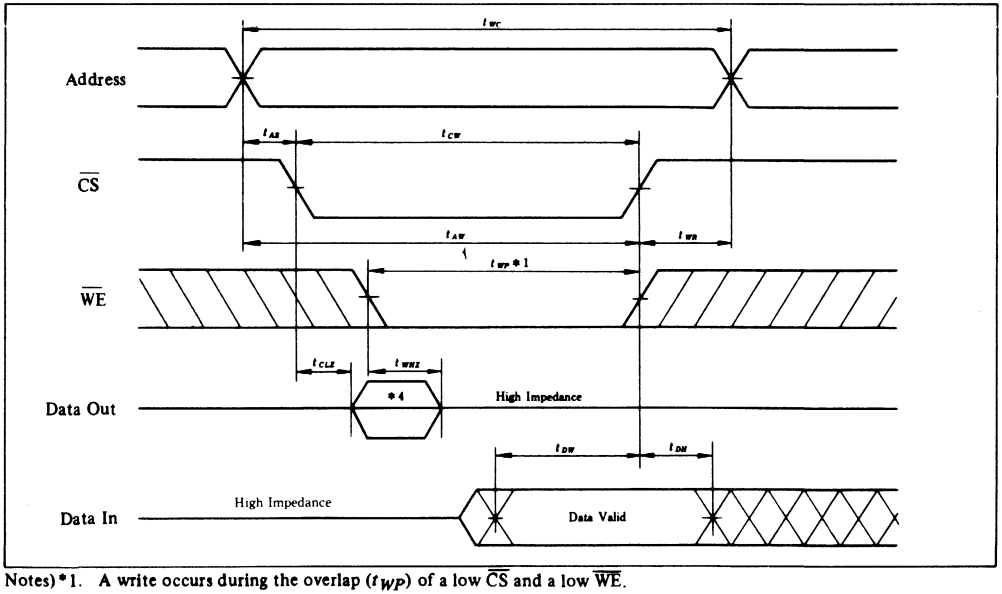
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3. Data Out is the same phase of write data of this write cycle.

*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

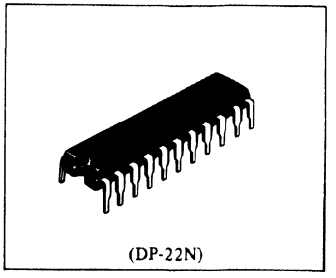
*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6287 Series

65536-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
  Standby: 100μW (typ.)/10μW (typ.) (L-version)
  Operation: 300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output
- Capability of Battery Back Up Operation (L-version)

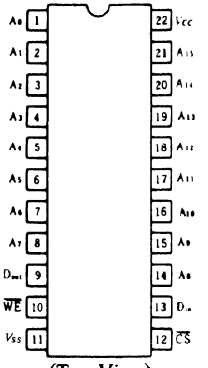


(DP-22N)

■ ORDERING INFORMATION

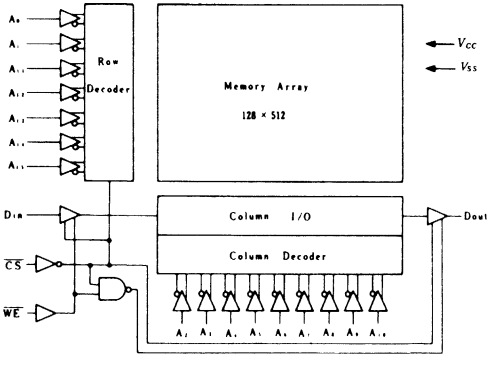
Type No.	Access Time	Package
HM6287P-45	45ns	300 mil 22 pin Plastic DIP
HM6287P-55	55ns	
HM6287P-70	70ns	
HM6287LP-45	45ns	
HM6287LP-55	55ns	
HM6287LP-70	70ns	

■ PIN ARRANGEMENT



(Top View)

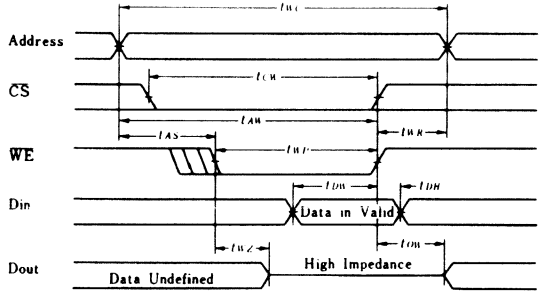
■ BLOCK DIAGRAM



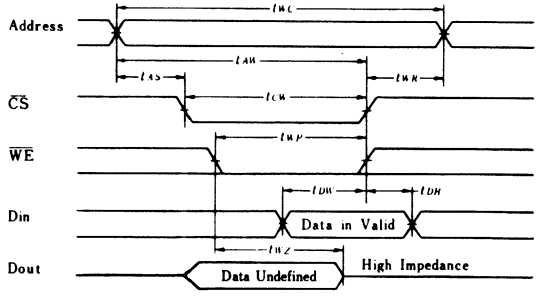
• WRITE CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns	2
Chip Selection to End of Write	t_{CW}	40	–	50	–	55	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	55	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	40	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	30	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3, 4

• Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



• Timing Waveform of Write Cycle No. 1 ($\overline{CS}$ Controlled)



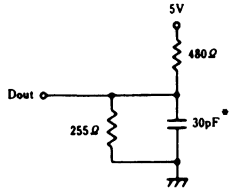
Notes) 1. If $\overline{CS}$ goes high Simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

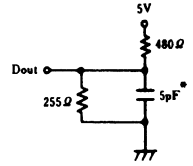
Input Pulse Levels: V_{SS} to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

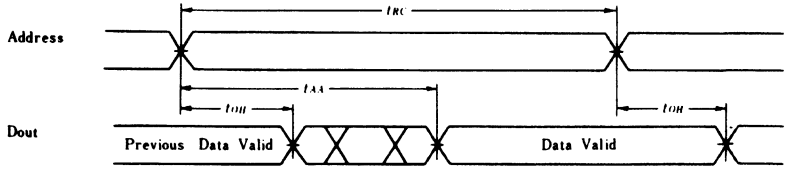


*Including scope & jig capacitance

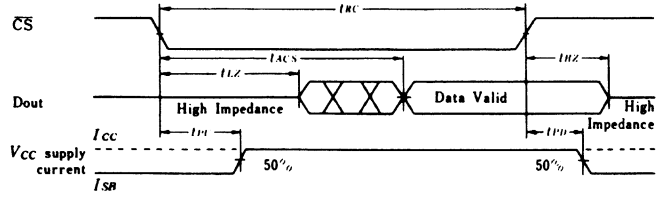
• READ CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns	1
Address Access Time	t_{AA}	–	45	–	55	–	70	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	7
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	–	40	ns	7

• Timing Waveform of Read Cycle No. 1 (4)(5)



• Timing Waveform of Read Cycle No. 2 (4)(6)



Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, while $\overline{CS} = V_{IL}$.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width ≦ 20ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{out} = 0mA, min. cycle	–	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	10	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V,	–	0.02	2.0	mA
		0V ≦ V_{in} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{in}	–	2*2	100*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = −4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	5	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	7.5	pF

Note) This parameter is sampled and not 100% tested.

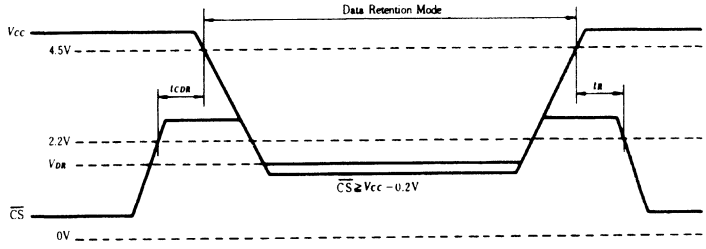
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$, $Vin \geqq V_{CC}-0.2V$ or $0V \leqq Vin \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}		–	1	50*2	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

Note) *1. t_{RC} = Read Cycle Time
*2. V_{CC} = 3.0V

● LOW V_{CC} DATA RETENTION WAVEFORM



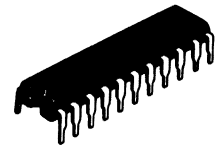
HM6287H Series

65536-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6287H is a high speed 64K static RAM organized as 64-kword × 1-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6287H packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting.

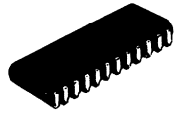
Low power version retains the data with battery back up.

HM6287HP Series



(DP-22NB)

HM6287HJP Series



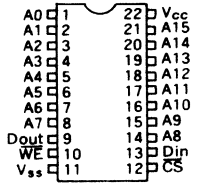
(CP-24D)

Features

- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 μW (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

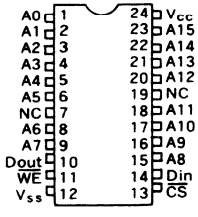
Pin Arrangement

HM6287HP Series



(Top View)

HM6287HJP Series



(Top View)

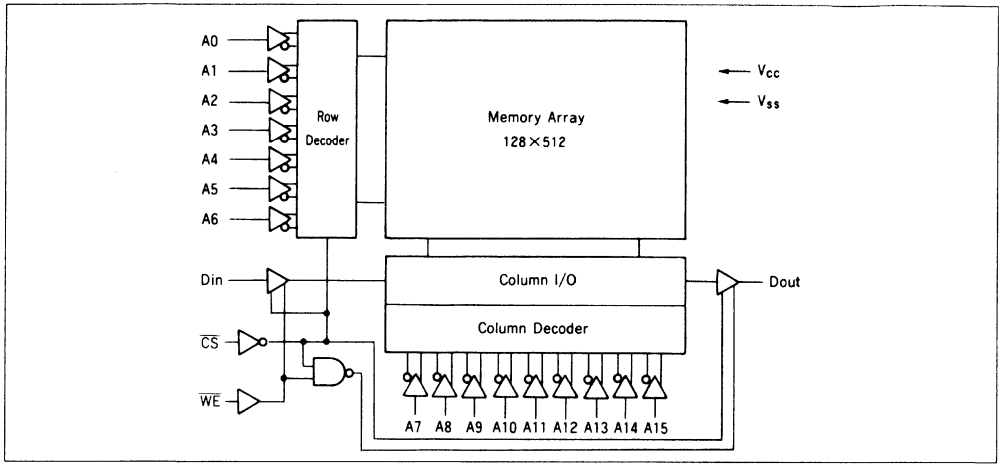
Pin Description

Pin Name	Function
A0 – A15	Address
Din	Input
Dout	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM6287HP-25	25 ns	300-mil 22-pin plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

Block diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read cycle 1, 2
L	L	Write	I_{CC}	High-Z	Write cycle 1, 2

Note: ×: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: *1. V_T min = −2.0 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: *1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = Vss to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = Vss to V_{CC}
Operating V_{CC} current	I_{CC}	—	60	120	mA	$\overline{CS}$ = V_{IL} Iout = 0 mA, min cycle
Standby V_{CC} current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby V_{CC} current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ Vin ≤ 0.2V or V_{CC} – 0.2 V ≤ Vin
		—	0.02*2	0.1*2	mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at V_{CC} = 5.0 V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	8	pF	Vout = 0 V

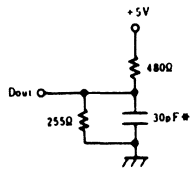
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

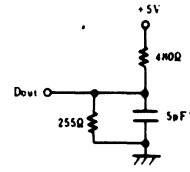
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B) (for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

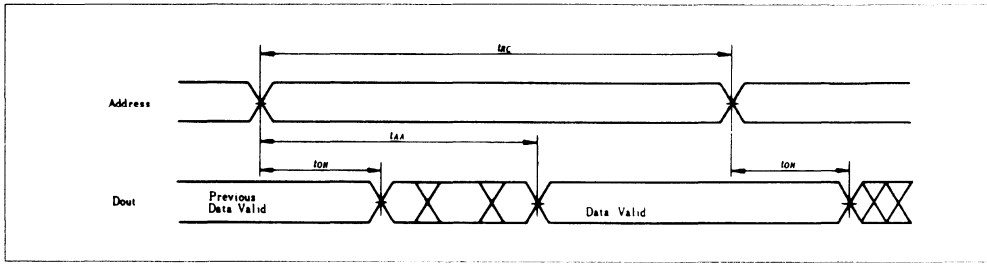


Note: Including scope & jig

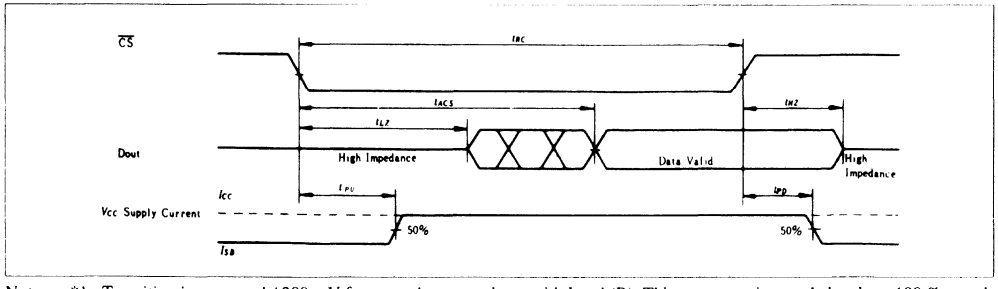
Read Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	12	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Read Timing Waveform (1) *2, *3, *5



Read Timing Waveform (2) *2, *4

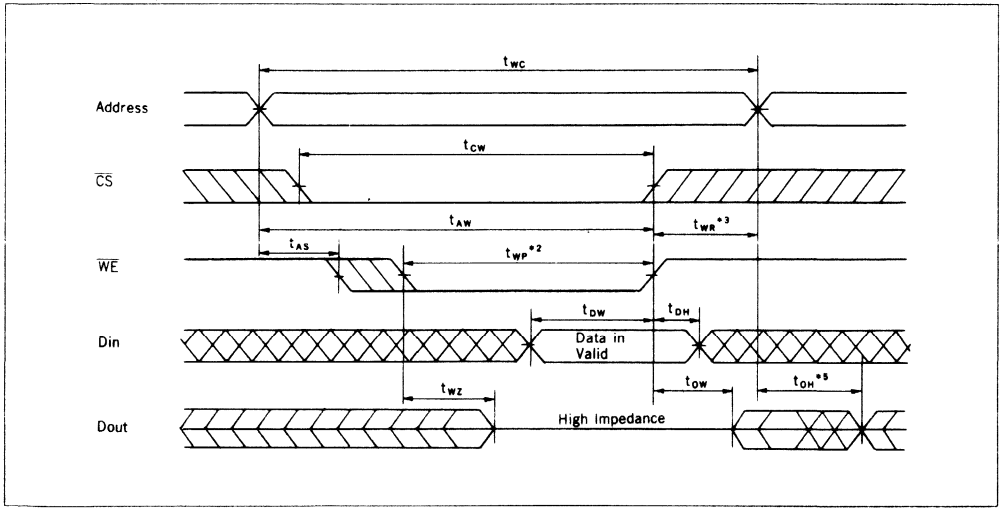


Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100 % tested.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. All read cycle timing are referenced from last valid address to the first transitioning address.

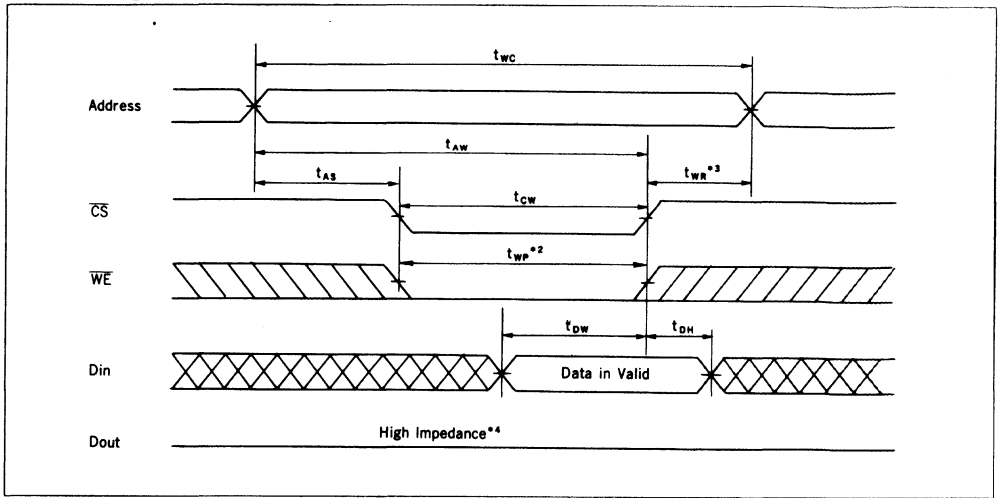
Write Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}*1	0	8	0	10	ns
Output active from end of write	t_{OW}*1	5	—	5	—	ns

Write Timing Waveform (1) (WE controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

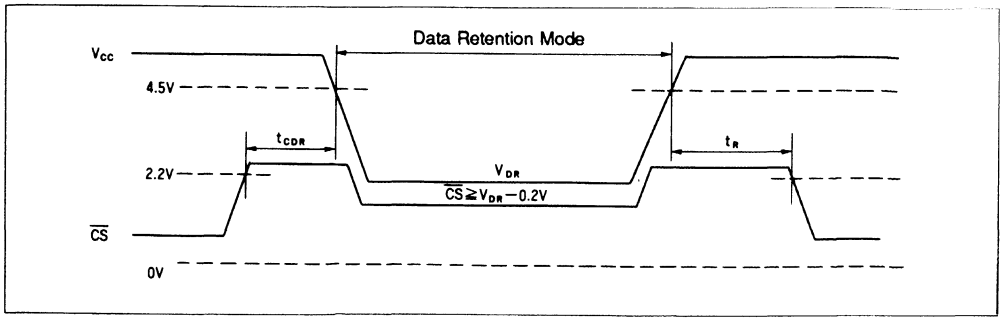
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

(This specification is guaranteed only for L-version.)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Notes: *1. t_{RC} = Read cycle time
*2. V_{CC} = 3.0 V
*3. V_{CC} = 2.0 V

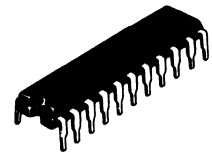
Low Vcc Data Retention Timing Waveform



HM6787 Series

65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

HM6787P Series



(DP-22NB)

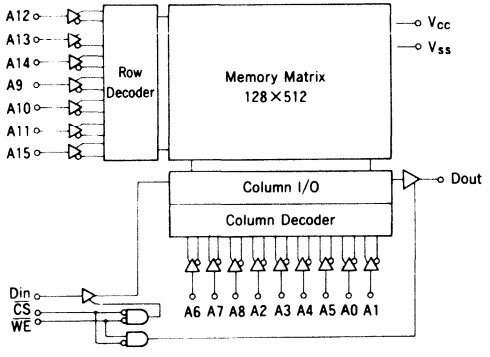
■ FEATURES

- Super Fast Access Time: 25ns/30ns (max.)
- Low Power Dissipation (DC):
  Operating 180mW (typ)
- High Driving Capability: I_{OL} 16mA
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output
- Skinny 22-pin Plastic Dip (300 mil)

■ ORDERING INFORMATION

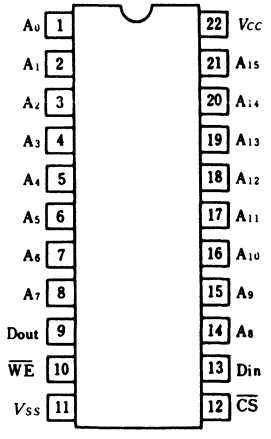
Type No.	Access Time	Package
HM6787P-25	25ns	300 mil 22 pin
HM6787P-30	30ns	Plastic DIP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

● HM6787P Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range (with bias)	T_{stg}(bias)	-10 to +85	°C

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}	Dout
L	L	Write	I_{CC}	High Z

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

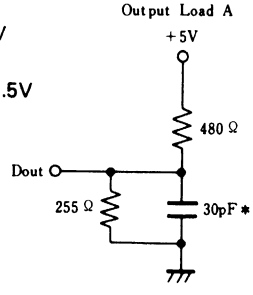
Note) *1. –3.0V for pulse width ≦ 20ns.

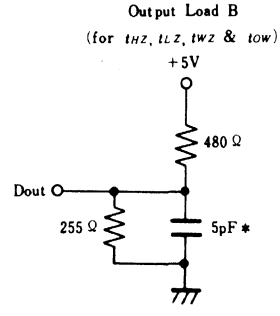
■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to +70°C)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT}=0mA	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	–	40	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$	–	–	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 16mA	–	–	0.5	V
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4	–	–	V

■ AC TEST CONDITIONS

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure





* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	7.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

• READ CYCLE

Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	
Address Access Time	t_{AA}	–	25	–	30	ns	
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	2
Chip Deselection to Power Down Time	t_{PD}	–	25	–	30	ns	2
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	3

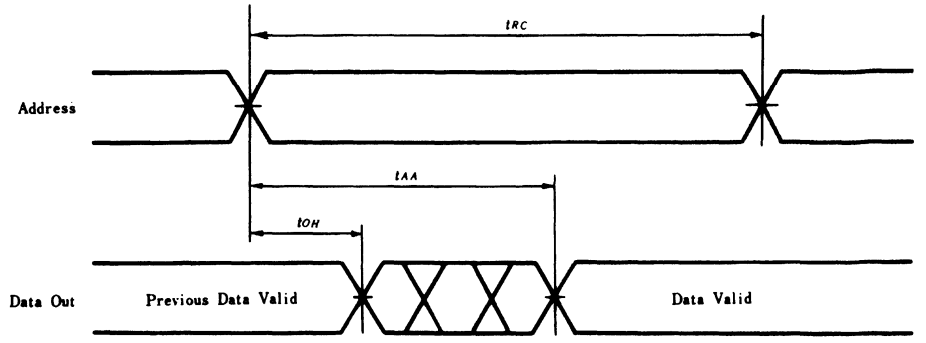
Notes) 1. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).
2. This parameter is sampled and not 100% tested.
3. Please contact your nearest Hitachi's Sale Dept. regarding specification.

• WRITE CYCLE

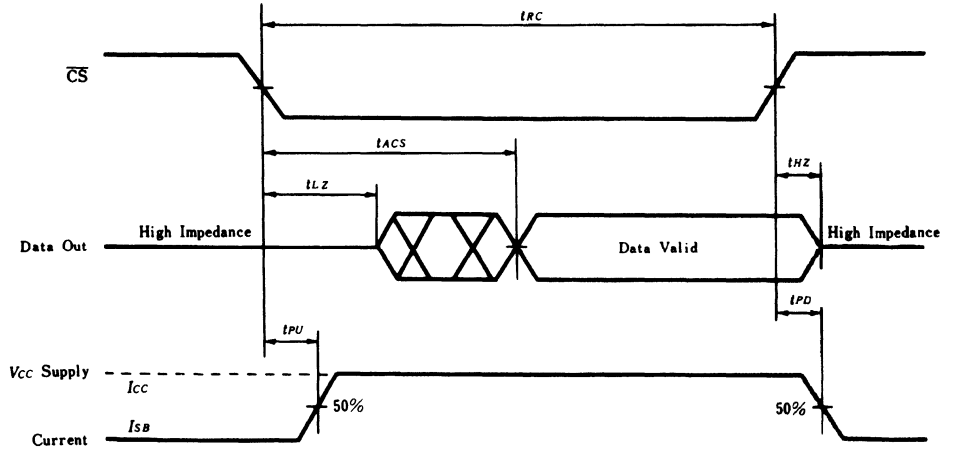
Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	25	–	30	–	ns	2
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	5	–	5	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).
4. This parameter is sampled and not 100% tested.

- **TIMING WAVEFORM OF READ CYCLE NO. 1[1), 2)]**

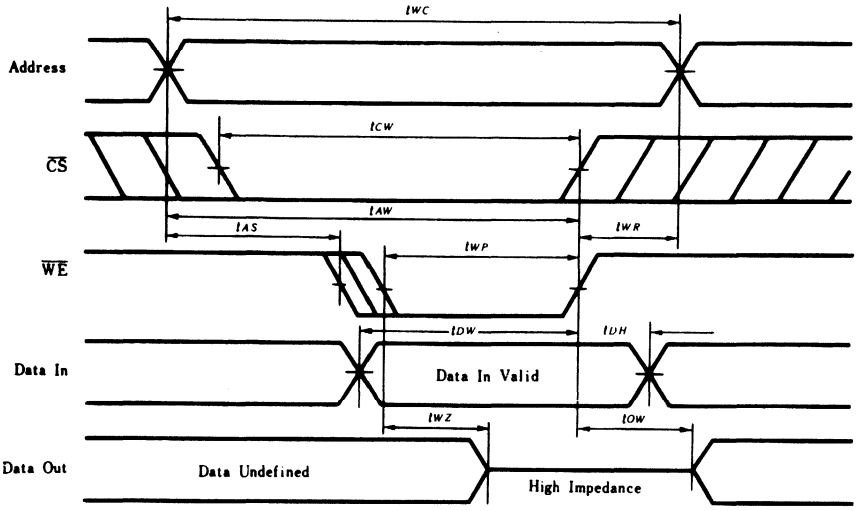


- **TIMING WAVEFORM OF READ CYCLE NO. 2[1), 3)]**



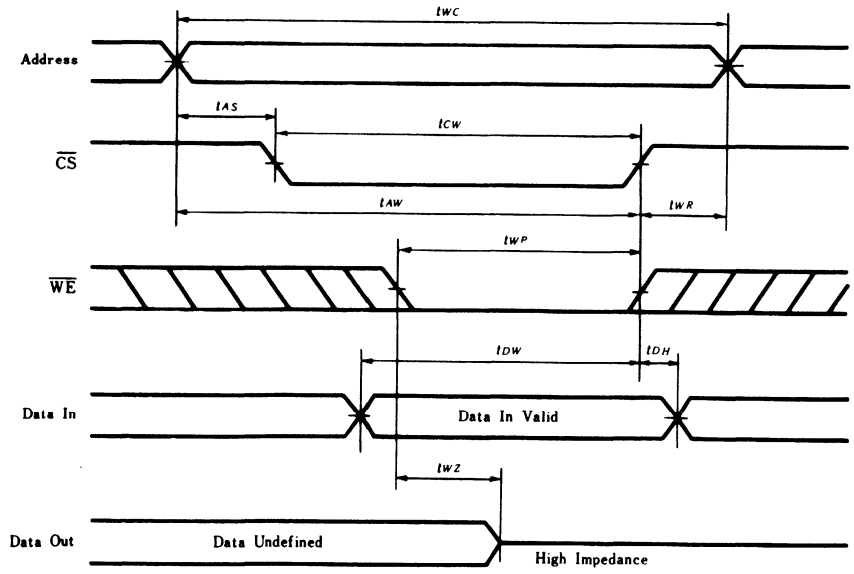
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

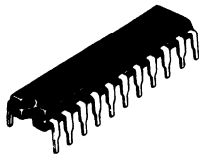
HM6787H Series

65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time: 15ns/20ns (max.)
- Low Power Dissipation (DC):
  Operating 210mW (typ)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

HM6787HP Series



(DP-22NB)

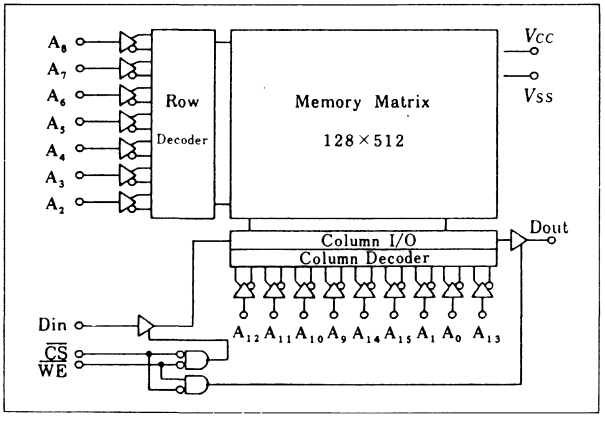
HM6787HJP Series

(CP-24D)

Ordering Information

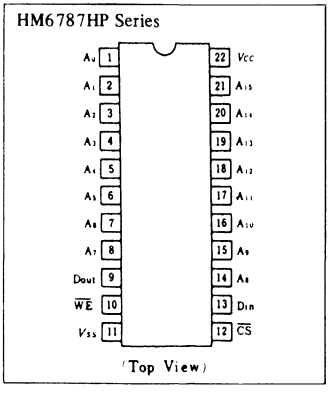
Type No.	Access Time	Package
HM6787HP-15	15ns	300 mil 22 pin
HM6787HP-20	20ns	Plastic DIP
HM6787HJP-15	15ns	300 mil 24 pin
HM6787HJP-20	20ns	Plastic SOJ

Block Diagram



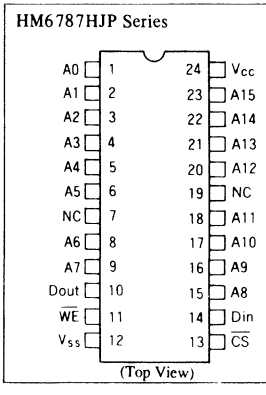
Pin Arrangement

HM6787HP Series



(Top View)

HM6787HJP Series



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range (with bias)	T (bias)	-10 to +85	°C

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Dout
L	L	Write	I_{CC}, I_{CC1}	High Z

Recommended DC Operating Conditions ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	-0.5*1	–	0.8	V

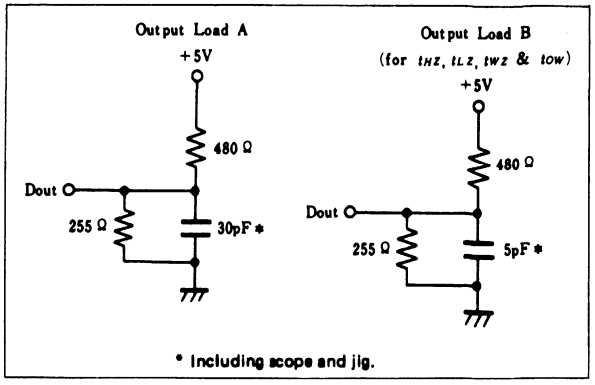
Note) *1. -3.0V for pulse width ≦ 10ns.

DC and Operating Characteristics ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $+70°C$)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS} = V_{IH}$, $V_{OUT} = V_{SS}$ to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS} = V_{IL}$, I_{OUT}=0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100%, I_{OUT} = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS} = V_{IH}$
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4mA

AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2

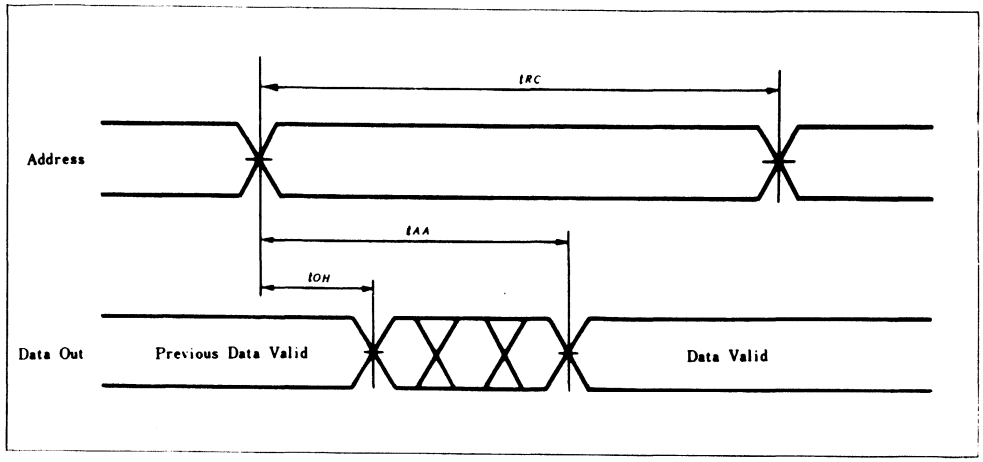
Note: 1. This parameter is sampled and 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

Write Cycle

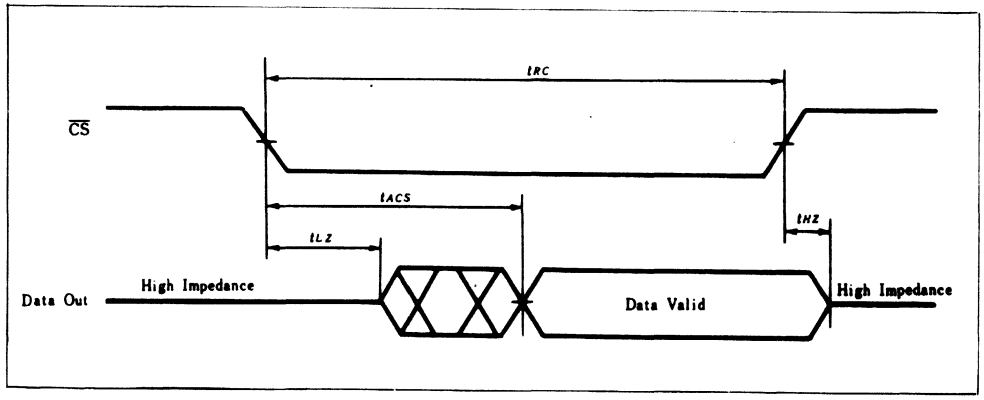
Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	3	–	3	–	ns	
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).
4. This parameter is sampled and not 100% tested.

Timing Waveform of Read Cycle No. 1[1), 2)]

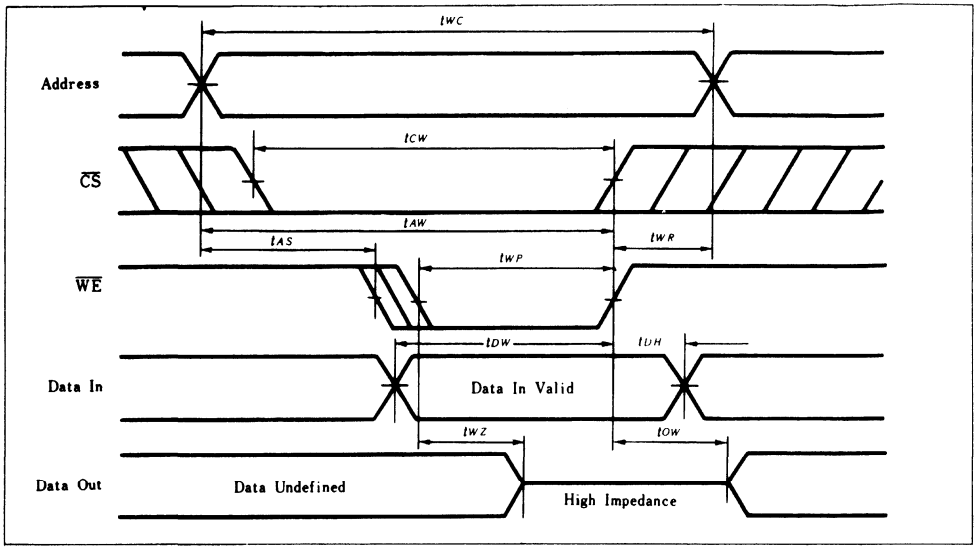


Timing Waveform of Read Cycle No. 2[1), 3)]



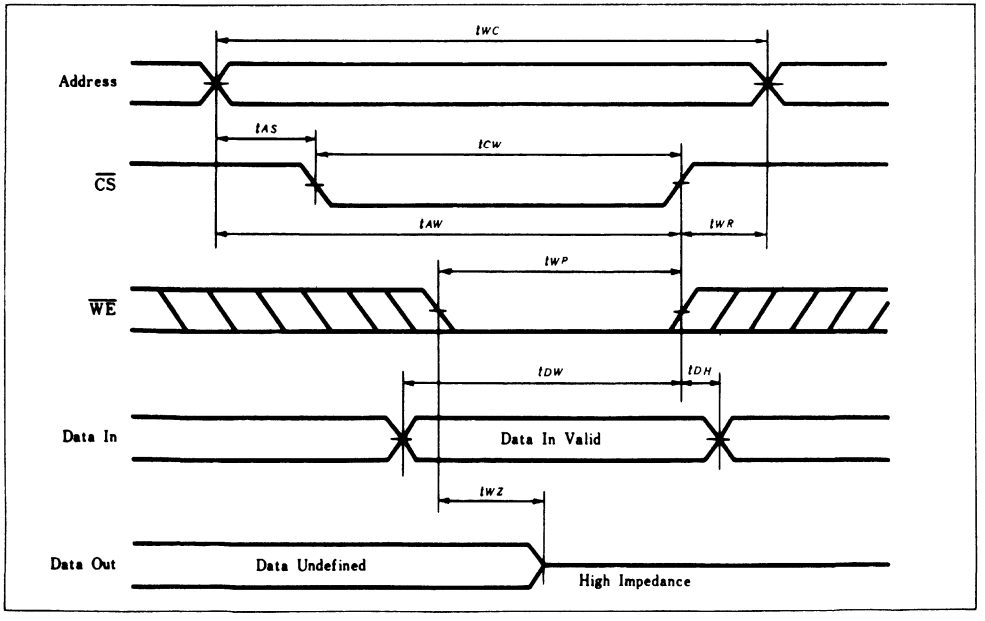
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load (B).

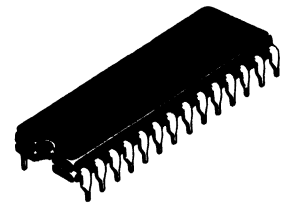
HM62256 Series

32768-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

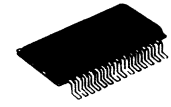
- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 200μW (typ)/10μW (typ) (L-/L-SL version),
  Operation: 40mW (typ.) (f = 1MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/L-SL version)

HM62256P Series



(DP-28)

HM62256FP Series

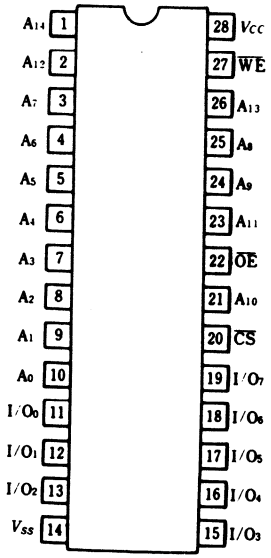


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62256P-8	85ns	600 mil 28 pin Plastic DIP
HM62256P-10	100ns	
HM62256P-12	120ns	
HM62256P-15	150ns	
HM62256LP-8	85ns	
HM62256LP-10	100ns	
HM62256LP-12	120ns	
HM62256LP-15	150ns	
HM62256LP-10SL	100ns	
HM62256LP-12SL	120ns	
HM62256LP-15SL	150ns	
HM62256FP-8T	85ns	28 pin Plastic SOP
HM62256FP-10T	100ns	
HM62256FP-12T	120ns	
HM62256FP-15T	150ns	
HM62256LFP-8T	85ns	
HM62256LFP-10T	100ns	
HM62256LFP-12T	120ns	
HM62256LFP-15T	150ns	
HM62256LFP-10SLT	100ns	
HM62256LFP-12SLT	120ns	
HM62256LFP-15SLT	150ns	

■ PIN ARRANGEMENT



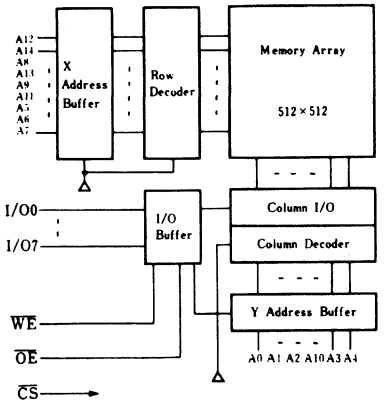
(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.0V for pulse width ≦ 50ns

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item		Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current		$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current		$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	8	15	mA
Average Operating Power Supply Current	HM62256-8	I_{CC1}	Min. Cycle, duty=100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	50	70	mA
	HM62256-10			–	40	70	
	HM62256-12			–	35	70	
	HM62256-15			–	33	70	
		I_{CC2}	$\overline{CS}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0V, $I_{I/O}$ = 0mA, f = 1MHZ	–	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS}$ = V_{IH}	–	0.5	3	mA
		I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V, 0V ≦ V_{IN}	–	0.04	2	mA
				–	2*2	100*2	μA
				–	2*3	50*3	
Output Voltage		V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
		V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V

Notes) *1. Typical values are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

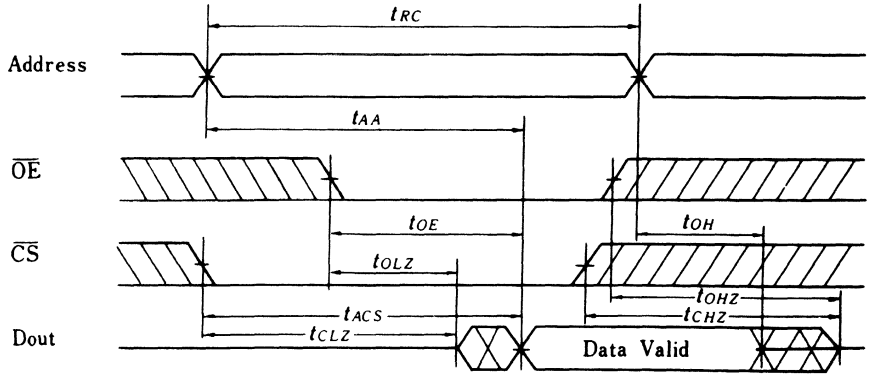
■ AC CHARACTERISTICS (V_{CC}=5V± 10%, T_a=0 to +70°C unless otherwise noted)

- **AC Test Conditions**
  - ○ Input pulse levels: 0.8V to 2.4V
  - ○ Input rise and fall times: 5ns
  - ○ Input and Output timing reference levels: 1.5V
  - ○ Output load: 1TTL Gate and C_L (100pF) (Including scope and jig)

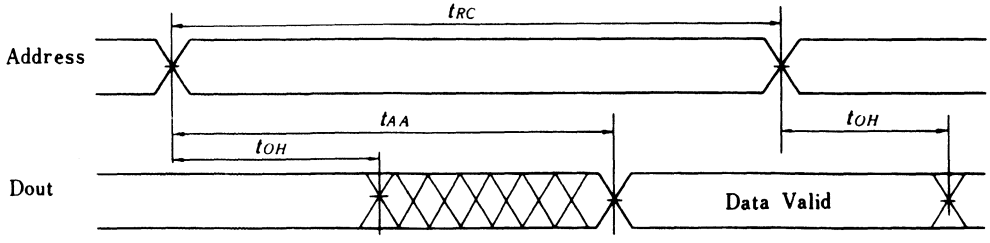
- **Read Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	–	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	85	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	45	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

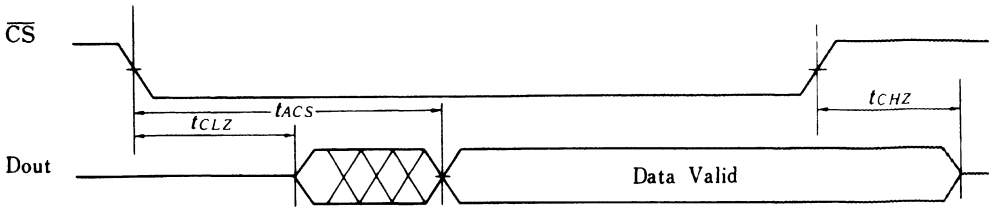
- **Timing Waveform of Read Cycle No. 1[1]**



- **Timing Waveform of Read Cycle No. 2[1][2][4]**



- **Timing Waveform of Read Cycle No. 3[1][3][4]**

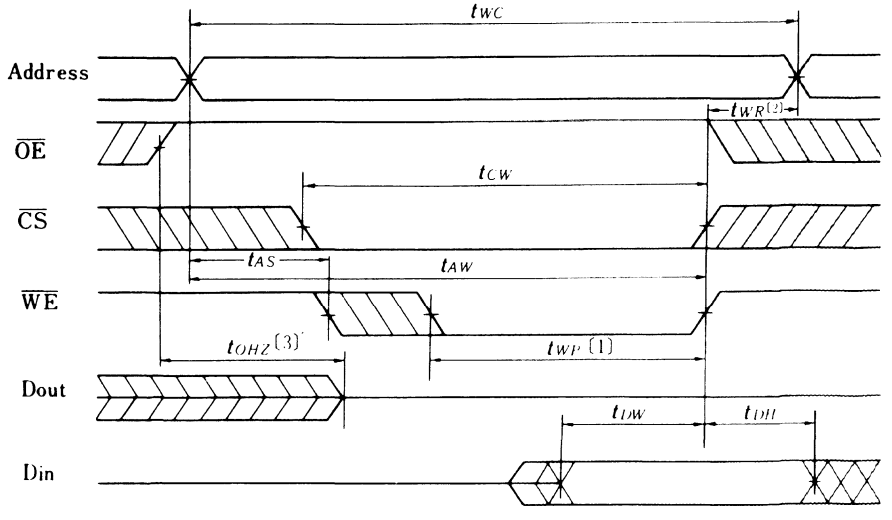


Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

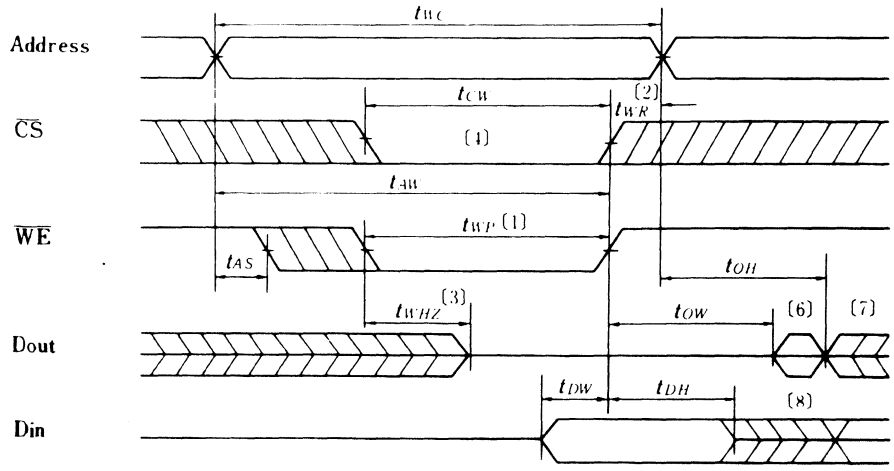
- **Write Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	–	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	75	–	80	–	85	–	100	–	ns
Address Valid to End of Write	t_{AW}	75	–	80	–	85	–	100	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	60	–	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns

- **Timing Waveform of Write Cycle No. 1 ($\overline{OE}$ Clock)**



- **Timing Waveform of Write Cycle No. 2[5] ($\overline{OE}$ Low Fixed)**



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

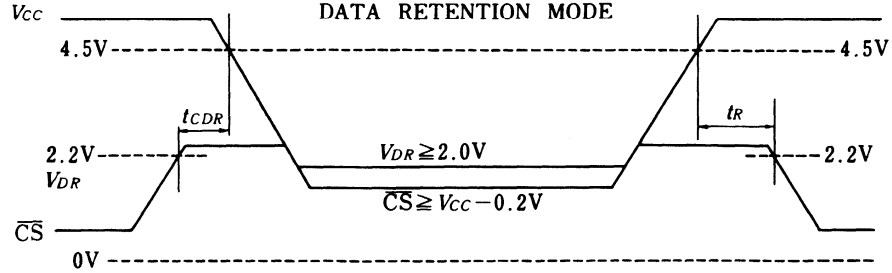
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

(This characteristics is guaranteed only for L-and L-SL version)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Date Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geq 2.8V$ $0V \leq V_{in}$	–	–	50*2	µA
			–	–	10*3	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

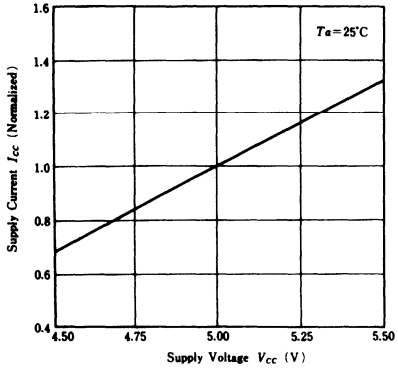
Note) *1. t_{RC} = Read Cycle Time
*2. This characteristic is guaranteed only for L-version, 20µA max. at T_a = 0 to 40°C.
*3. This characteristic is guaranteed only for L-SL version, 3µA max. at T_a = 0 to 40°C.

- **Low V_{CC} Data Retention Waveform**

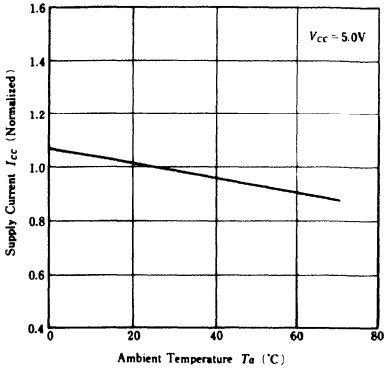


Note) In Data Retention Mode, $\overline{CS}$ controls the Address, $\overline{WE}$, $\overline{OE}$, and Din Buffers. *Vin* for these inputs can be in high impedance state in data retention mode.

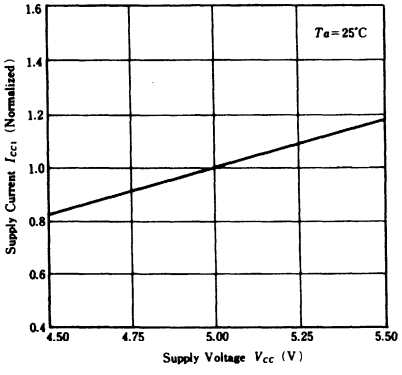
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1)



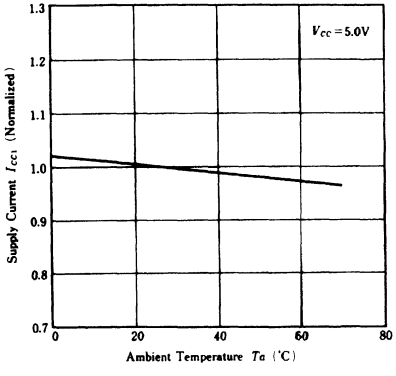
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (1)



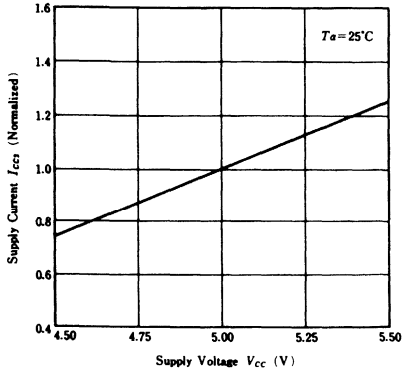
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2)



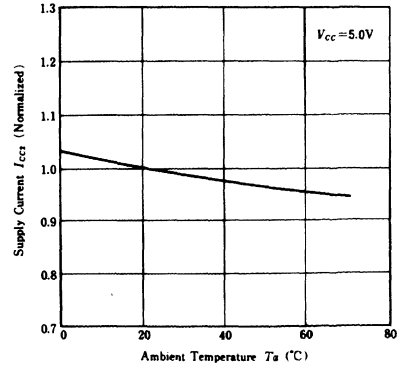
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (2)



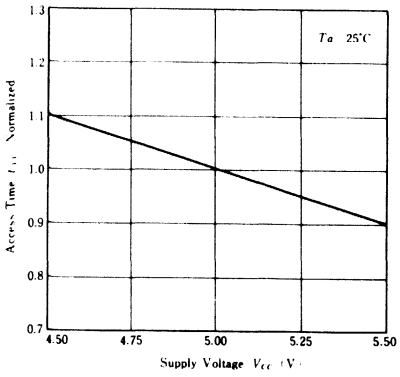
SUPPLY CURRENT vs. SUPPLY VOLTAGE (3)



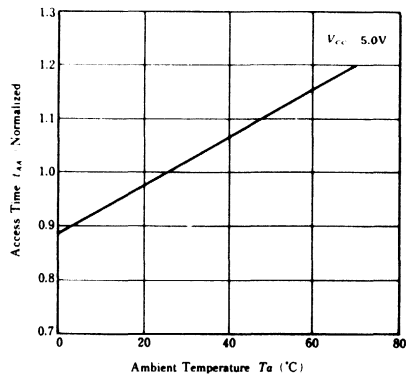
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (3)



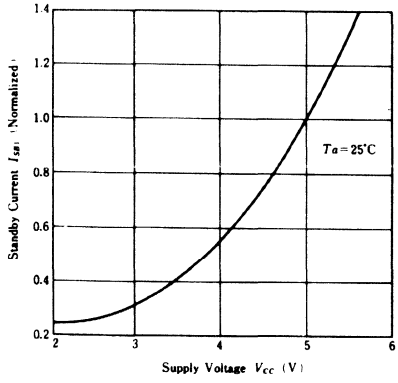
ACCESS TIME vs. SUPPLY VOLTAGE



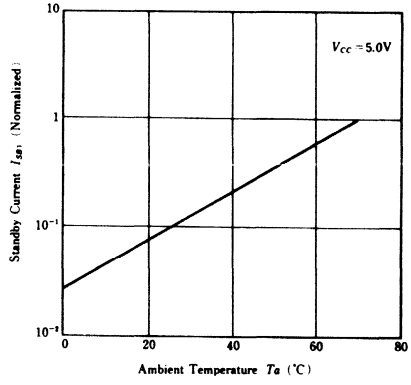
ACCESS TIME vs. AMBIENT TEMPERATURE



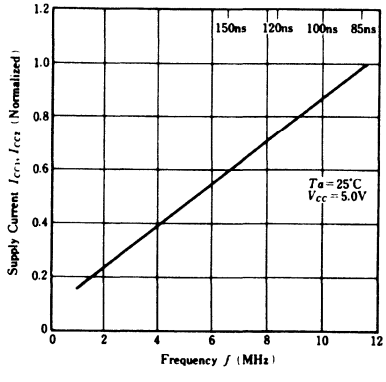
STANDBY CURRENT vs. SUPPLY VOLTAGE



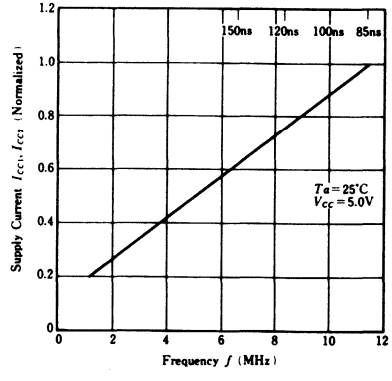
STANDBY CURRENT vs. AMBIENT TEMPERATURE



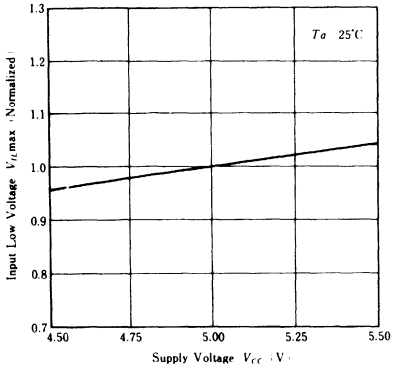
SUPPLY CURRENT vs. FREQUENCY (READ)



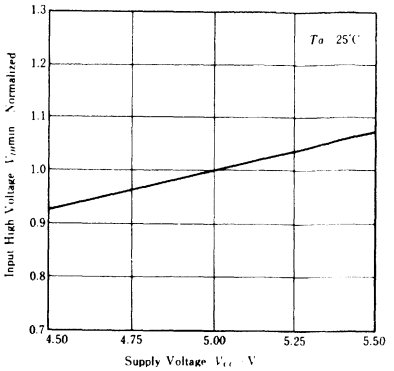
SUPPLY CURRENT vs. FREQUENCY (WRITE)



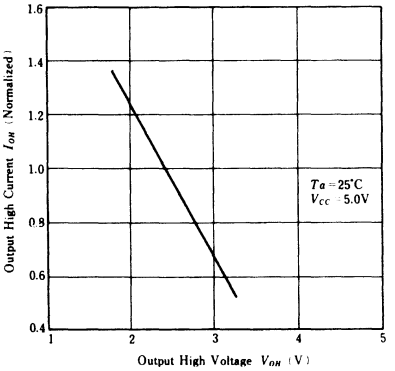
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



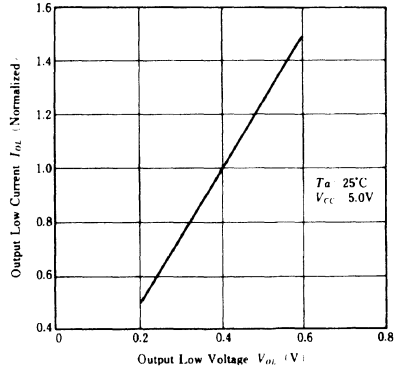
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



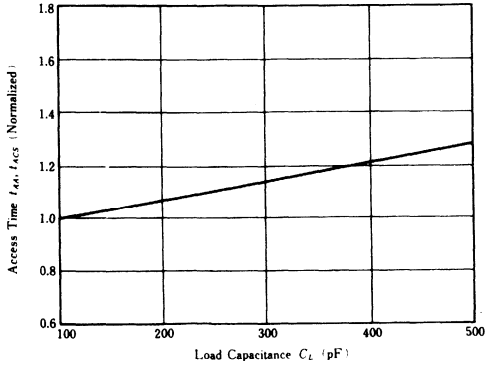
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME vs. LOAD CAPACITANCE



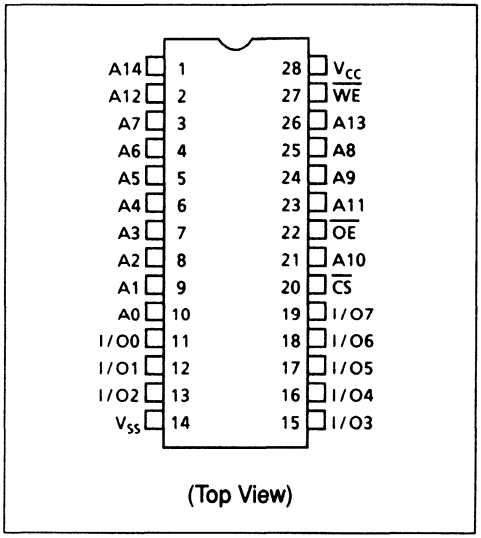
HM62832 Series

32768-Word × 8-Bit High Speed CMOS Static RAM

Features

- High speed: Fast access time 35/45 ns (max)
- Low power
  Standby: 10 µW (typ) (L-version)
  Operation: 300 mW (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output – Three state output
- Directly TTL compatible – All inputs and outputs

Pin Arrangement



(Top View)

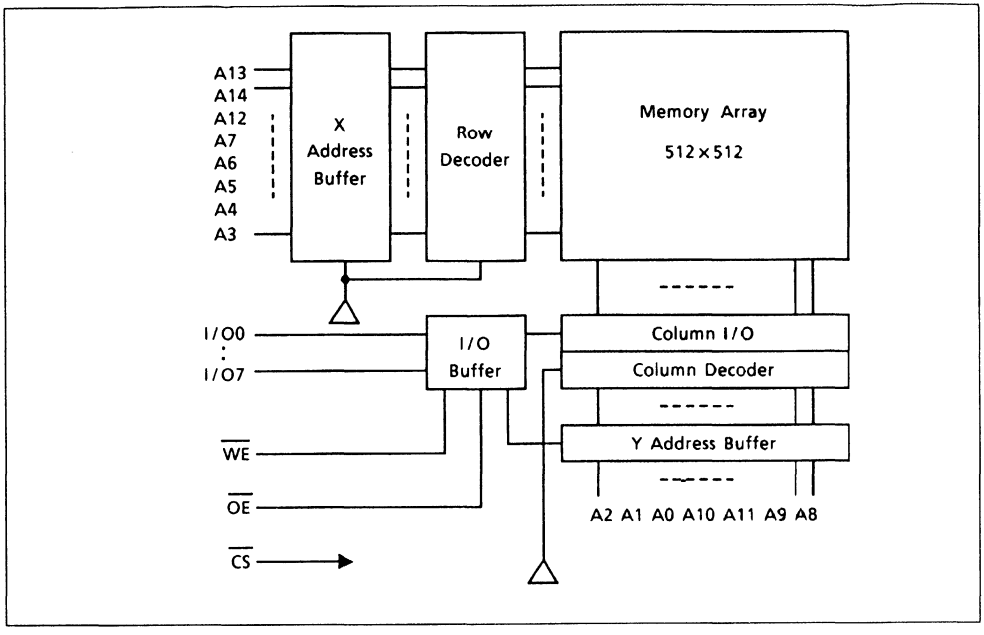
Ordering Information

Type No.	Access time	Package
HM62832P–35	35 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832P–45	45 ns	
HM62832LP–35	35 ns	
HM62832LP–45	45 ns	
HM62832JP–35	35 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832JP–45	45 ns	
HM62832LJP–35	35 ns	
HM62832LJP–45	45 ns	

Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −2.5 V for pulse width ≤ 10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L		I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 1	V
	V_{IL}	–0.5 *1	—	0.8	V

Note: 1. –2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Average operating power supply current	I_{CC}	—	60	120	mA	Min cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby V_{CC} current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V	
		—	3	100	µA		L-version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)

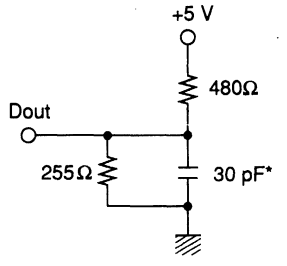
Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Add, $\overline{WE}$, $\overline{OE}$	Cin	—	—	6	pF	Vin = 0 V
	$\overline{CS}$	Cin ($\overline{CS}$)	—	—	8	pF	Vin = 0 V
Input/output capacitance		$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

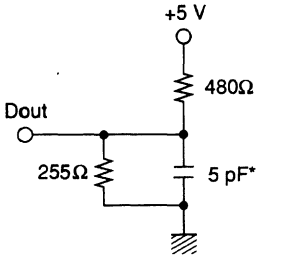
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Output load (A)



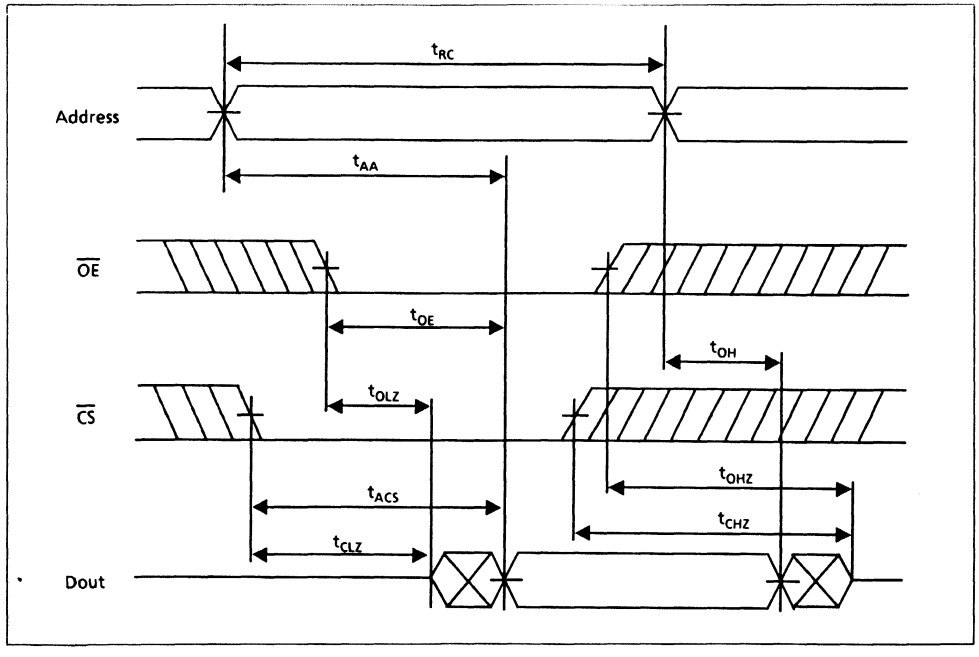
Output load (B)
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW})

* Including scope and jig.

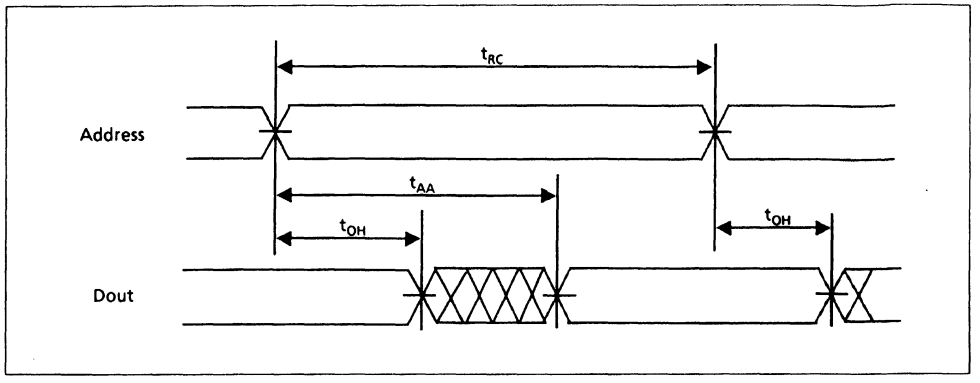
Read Cycle

Parameter	Symbol	HM62832–35		HM62832–45		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	35	—	45	—	ns
Address access time	t_{AA}	—	35	—	45	ns
Chip select access time	t_{ACS}	—	35	—	45	ns
Output enable to output valid	t_{OE}	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip selection to output in low Z	t_{CLZ}	5	—	5	—	ns
Output enable to output in low Z	t_{OLZ}	0	—	0	—	ns
Chip deselection to output in high Z	t_{CHZ}	0	15	0	20	ns
Output disable to output in high Z	t_{OHZ}	0	15	0	20	ns

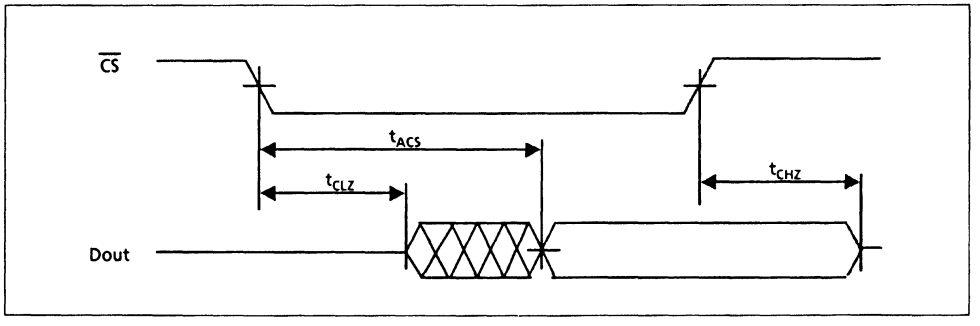
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1, *2, *4



Read Timing Waveform (3) *1, *3, *4



Notes: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.

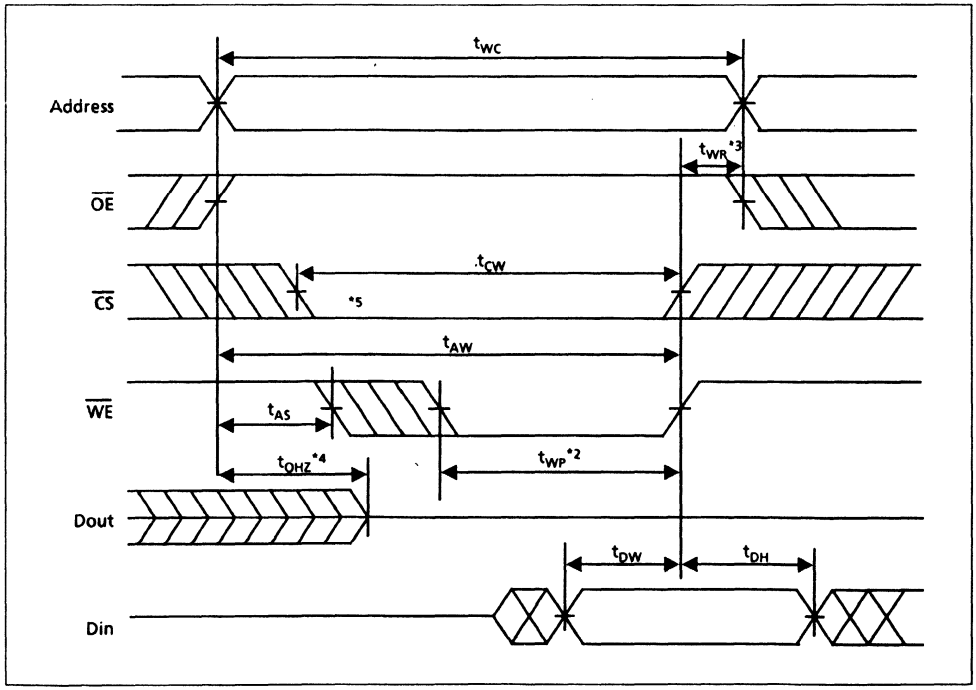
Write Cycle

		HM62832-35		HM62832-45		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time	t_{WC}	35	—	45	—	ns
Chip selection to end of write	t_{CW}	30	—	40	—	ns
Address valid to end of write	t_{AW}	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	ns

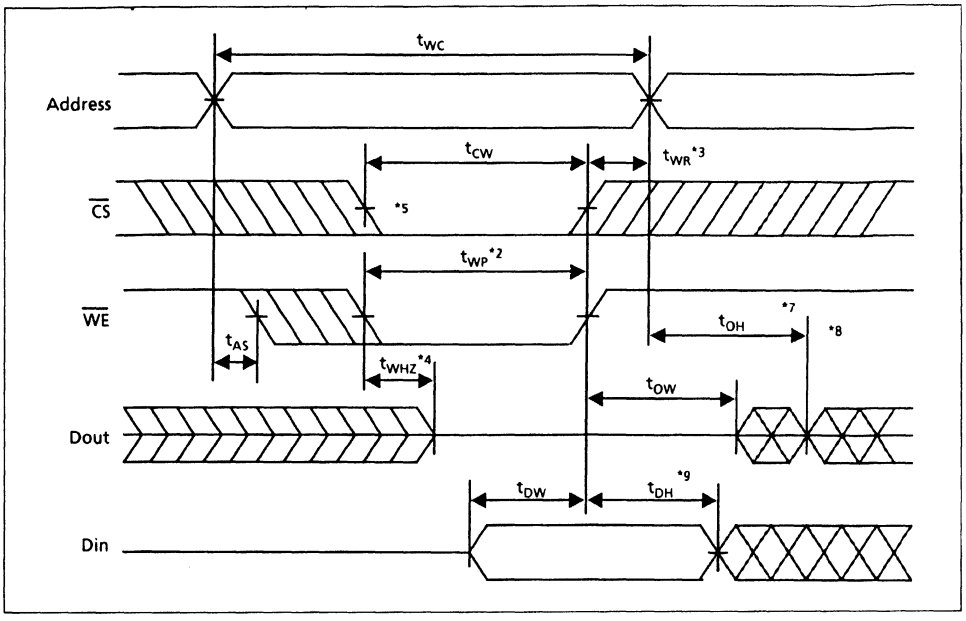
Write Cycle (cont)

Parameter	Symbol	HM62832–35 Min	HM62832–35 Max	HM62832–45 Min	HM62832–45 Max	Unit
Write pulse width	t_{WP}	20	—	25	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Write to output in high Z	t_{WHZ}	0	15	0	20	ns
Data to write time overlap	t_{DW}	15	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output disable to output in high Z	t_{OHZ}	0	15	0	20	ns
Output active from end of write	t_{OW}	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fixed)



Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the ealier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.
9. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

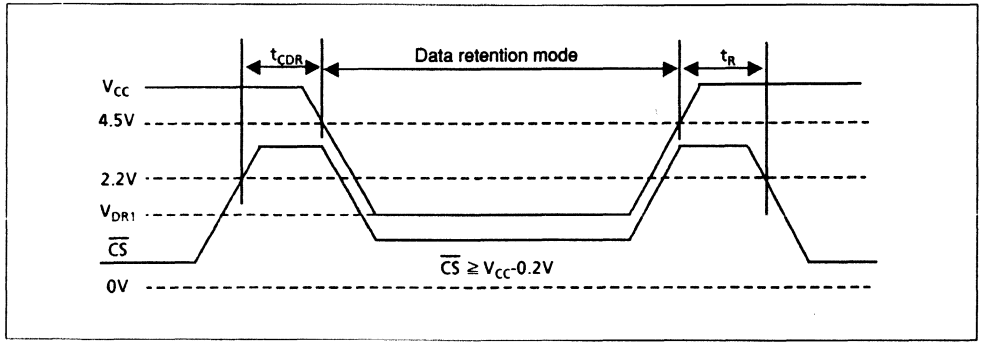
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2 V, Vin ≥ V_{CC} –0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50 *1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5 *1	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



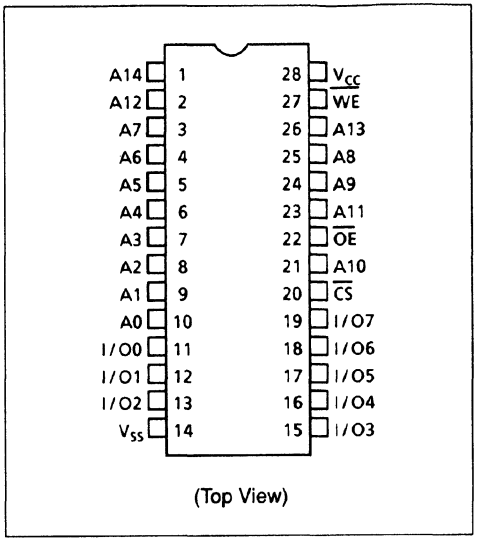
HM62832H Series — Preliminary

32768-Word × 8-Bit High Speed CMOS Static RAM

Features

- High speed: Fast access time 25/35 ns (max)
- Low power
  Active: 300 mW (typ)
  Standby: 10 µW (typ) (L-version)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output – Three state output
- Directly TTL compatible – All inputs and outputs

Pin Arrangement



(Top View)

Ordering Information

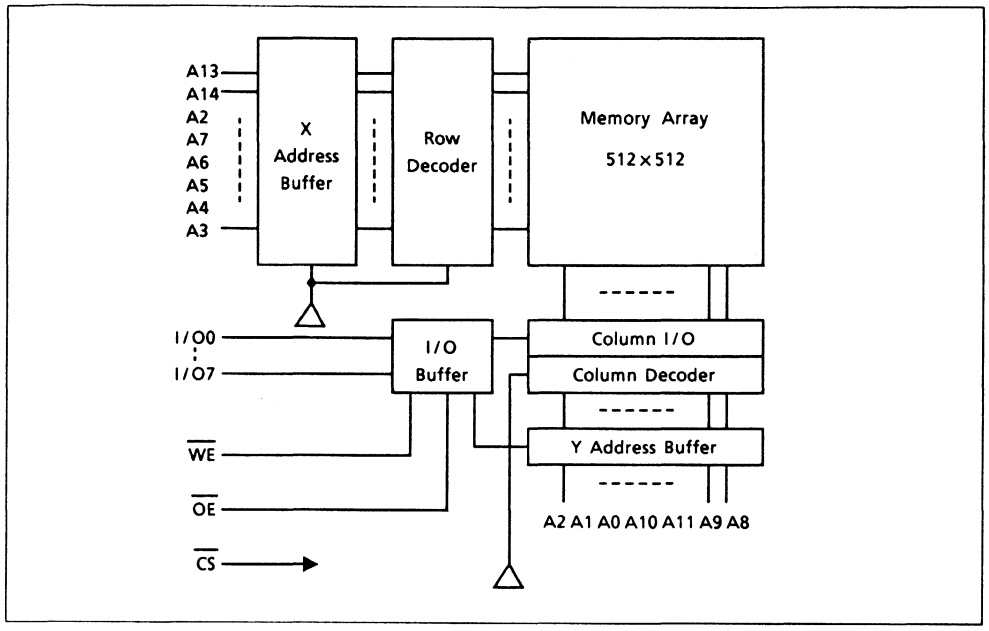
Type No.	Access time	Package
HM62832HP–25	25 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832HP–35	35 ns	
HM62832HLP–25	25 ns	
HM62832HLP–35	35 ns	
HM62832HJP–25	25 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832HJP–35	35 ns	
HM62832HLJP–25	25 ns	
HM62832HLJP–35	35 ns	

Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: 1. −2.5 V for pulse width ≤ 10 ns

Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	X	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read cycle (1) to (3)
L	H	L	Write	I_{CC}	Din	Write cycle (1)
L	L	L		I_{CC}	Din	Write cycle (2)

Note: 1. X: H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 1	V
	V_{IL}	–0.5 *1	—	0.8	V

Note: 1. –2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test conditions	Notes
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating power supply current	I_{CC}	—	60	120	mA	Min cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby power supply current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
Standby power supply current	I_{SB1}	—	0.02	2	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V, 0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} – 0.2 V	
		—	0.002	0.1	mA		L-version
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA	

Note: 1. Typical values are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1.0 MHz)

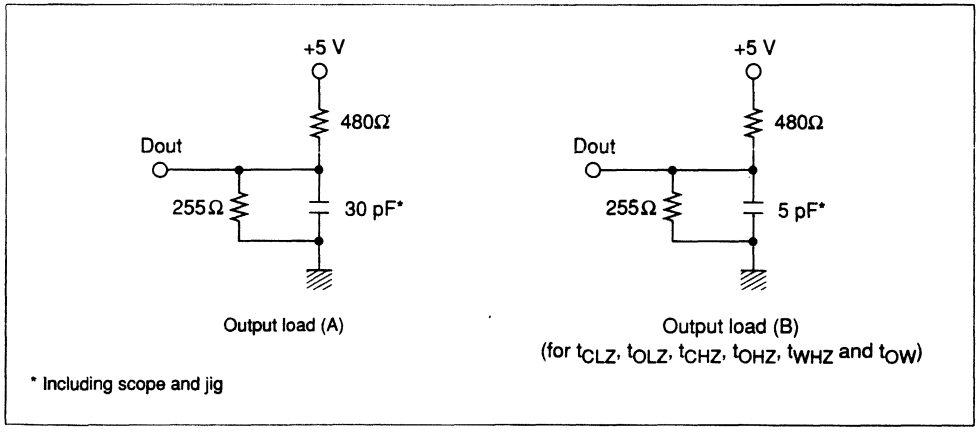
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



Read Cycle

Parameter	Symbol	HM62832H–25		HM62832H–35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip selection to output in low Z	t_{CLZ}	5	—	5	—	ns
Output enable to output in low Z	t_{OLZ}	0	—	0	—	ns
Chip deselection to output in high Z	t_{CHZ}	0	12	0	15	ns
Output enable to output in high Z	t_{OHZ}	0	12	0	15	ns

Write Cycle

Parameter	Symbol	HM62832H–25		HM62832H–35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	15	—	20	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	20	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Write to output in high Z	t_{WHZ}	0	12	0	15	ns
Data to write time overlap	t_{DW}	12	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output disable to output in high Z	t_{OHZ}	0	12	0	15	ns
Output active from end of write	t_{OW}	5	—	5	—	ns

Timing Waveforms

Refer to the HM62832 data sheet for timing waveforms.

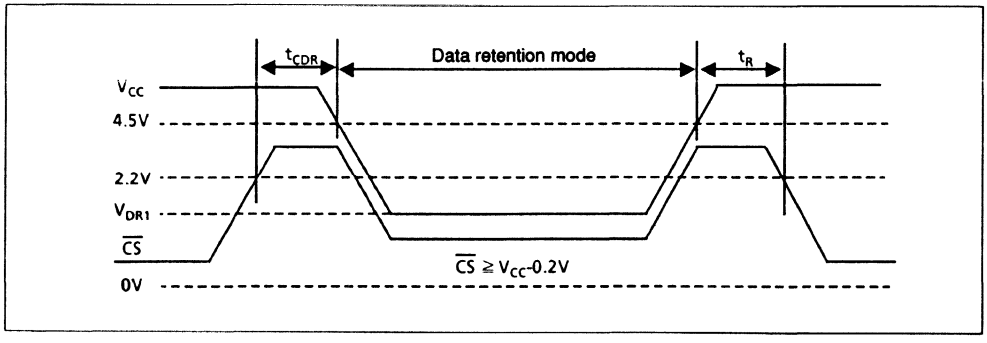
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC}$ –0.2 V, Vin ≥ V_{CC} –0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. V_{CC} = 3.0 V

Low V_{CC} Data Retention Timing Waveform



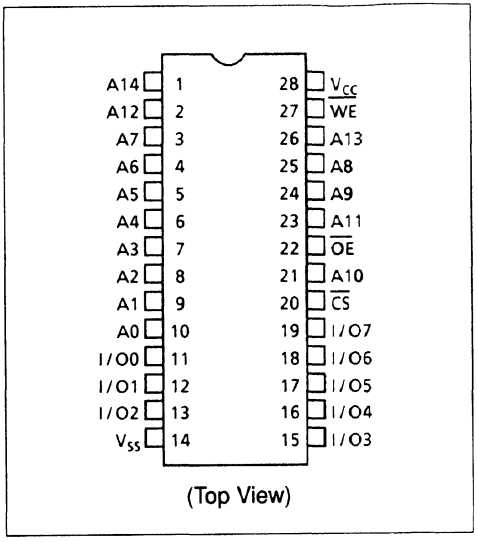
HM62832UH Series — Under Development

32768-Word × 8-Bit High Speed CMOS Static RAM

Features

- High speed: Fast access time 15/20 ns (max)
- Low power
  Standby: 10 µW (typ) (L-version)
  Operation: 400 mW (typ)
- Single 5 V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output – Three state output
- Directly TTL compatible – All inputs and outputs

Pin Arrangement



(Top View)

Ordering Information

Type No.	Access time	Package
HM62832UHP–15	15 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832UHP–20	20 ns	
HM62832UHLP–15	15 ns	
HM62832UHLP–20	20 ns	
HM62832UHJP–15	15 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832UHJP–20	20 ns	
HM62832UHLJP–15	15 ns	
HM62832UHLJP–20	20 ns	

Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM6208 Series
HM6208H Series

65536-Word × 4-Bit High Speed CMOS Static RAM

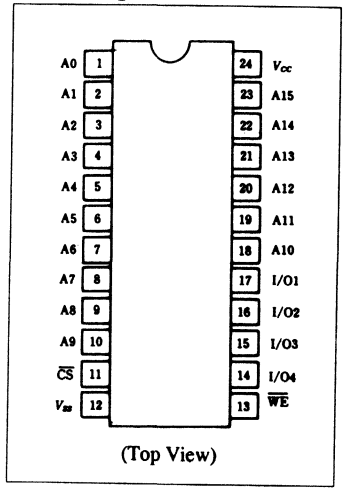
Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ)
  - 30 µW (typ) (L-version)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6208HP-25	25 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6208HP-35	35 ns	
HM6208P-35	35 ns	
HM6208P-45	45 ns	
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208LP-35	35 ns	
HM6208LP-45	45 ns	
HM6208HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HLJP-25	25 ns	
HM6208HLJP-35	35 ns	

Pin Arrangement

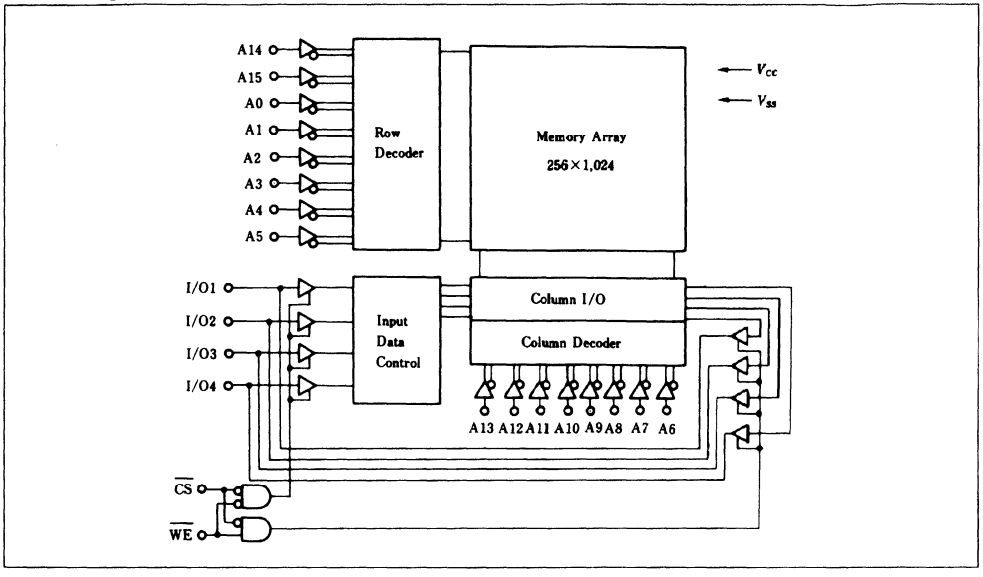


(Top View)

Pin Description

Pin Name	Function
A0 – A15	Address
I/O1 – I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	Din	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM6208H-25			HM6208-35 HM6208-45 HM6208H-35			Unit	Test Conditions	Note
		Min	Typ*1	Max	Min	Typ*1	Max			
Input leakage current	I_{LI}	—	—	2.0	—	—	2.0	µA	V_{CC}=Max Vin=Vss to Vcc	
Output leakage current	I_{LO}	—	—	10.0	—	—	10.0	µA	$\overline{CS}$=V_{IH} $V_{I/O}$=Vss to Vcc	
Operating power supply current	I_{CC}	—	60	120	—	50	100	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA Min cycle duty=100%	
	I_{CC1}	—	40	80	—	40	80	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA t_{cycle}=50 ns duty=100%	
Standby power supply current	I_{SB}	—	20	40	—	15	30	mA	$\overline{CS}$=V_{IH}, Min cycle	
Standby power supply current(1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$>Vcc -0.2 V 0 V≤Vin < 0.2 V or	
		—	0.006	0.1	—	0.006	0.1		Vin≥Vcc -0.2 V	L-Version
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL}=8 mA	
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH}=–4.0 mA	

Note: *1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	HM6208-35 HM6208-45		HM6208H-25 HM6208H-35		Unit	Test Conditions
		Min	Max	Min	Max		
Input capacitance	C_{in}	—	6	—	6	pF	V_{in}=0 V
Input/output capacitance	$C_{I/O}$	—	10	—	11	pF	$V_{I/O}$=0 V

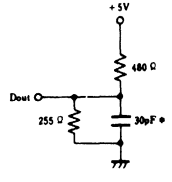
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

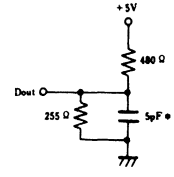
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



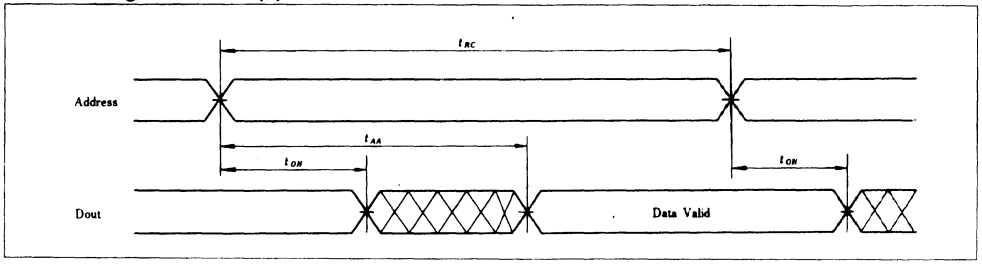
Note: * Including scope & jig.

Read cycle

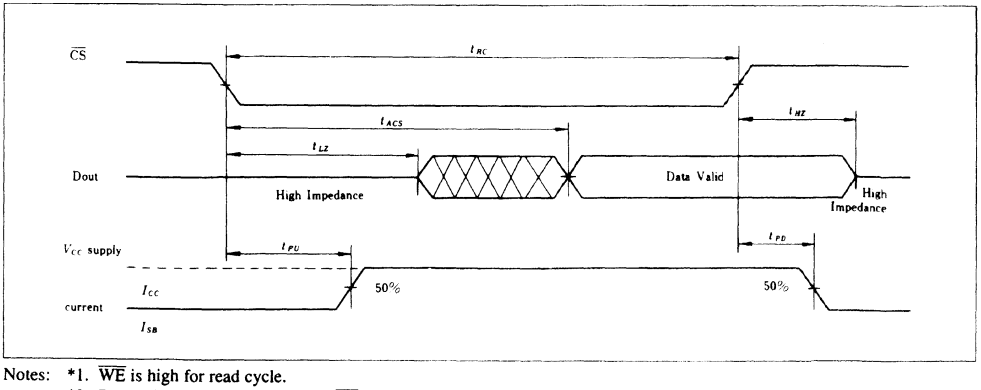
Item	Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	12	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	25	—	30	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



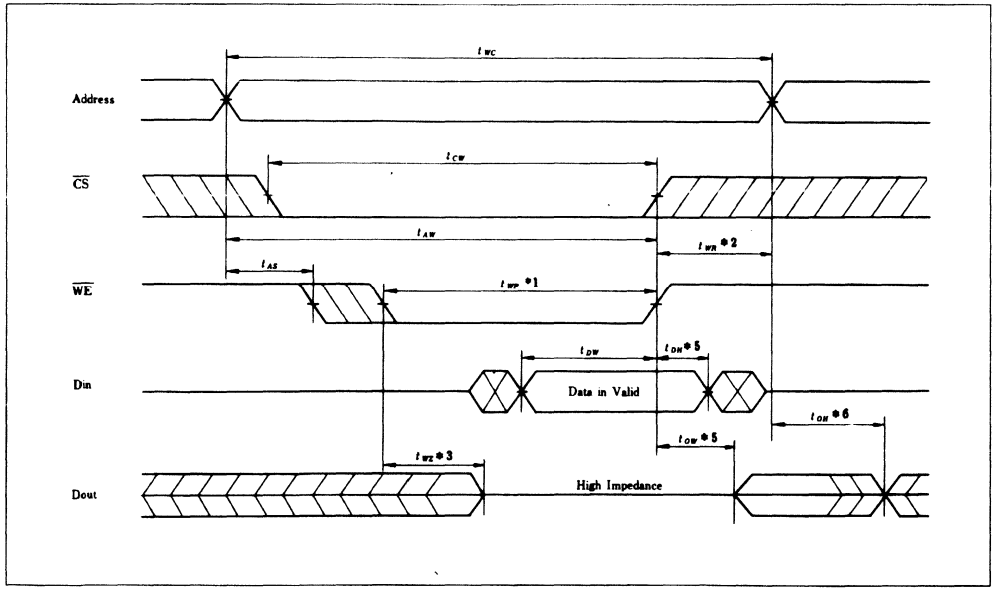
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

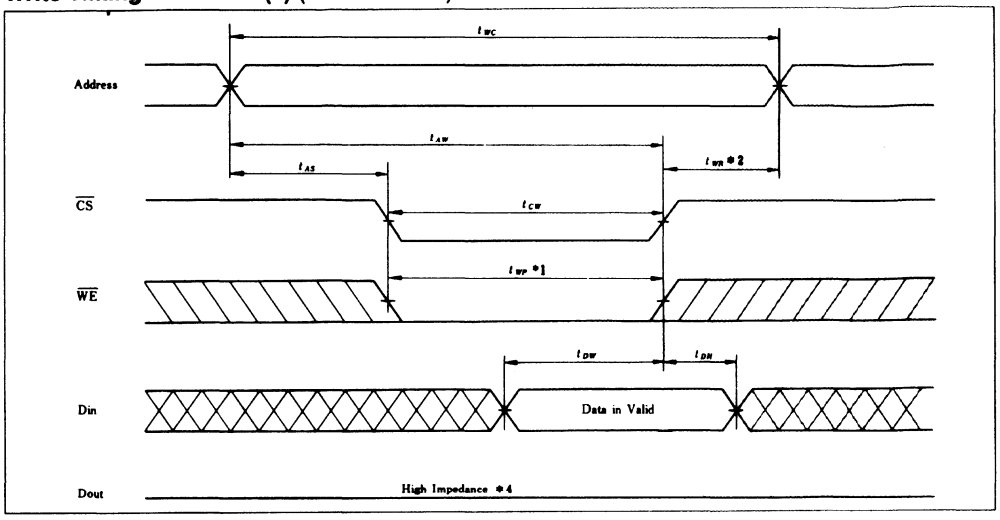
Item	Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit	Note
		Min	Max	Min	Max	Min	Max		
Write cycle time	twc	25	—	35	—	45	—	ns	
Chip selection to end of write	tcw	20	—	30	—	40	—	ns	
Address valid to end of write	taw	20	—	30	—	40	—	ns	
Address setup time	tas	0	—	0	—	0	—	ns	
Write pulse width	twp	20	—	25	—	30	—	ns	
Write recovery time	twr	3	—	3	—	3	—	ns	
Data valid to end of write	tdw	15	—	20	—	20	—	ns	
Data hold time	tdh	0	—	0	—	0	—	ns	
Write enabled to output in high-Z	twz*1	0	8	0	10	0	15	ns	
Output active from end of write	tow*1	0	—	0	—	0	—	ns	

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state. The input signals of the opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle.

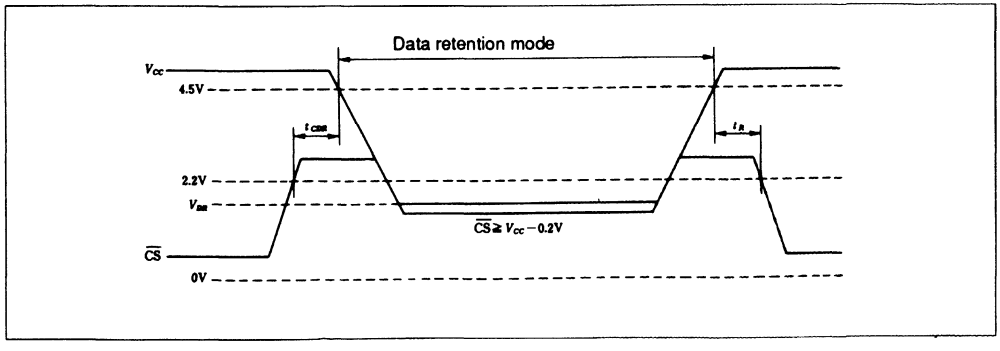
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V, Vin ≥ Vcc − 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50 *1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: *1. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform



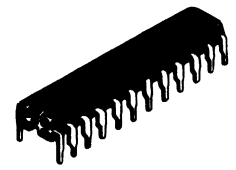
HM6708 Series

65536-word x 4-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 20/25ns (max.)
- Low Power Dissipation
  Operating: 350mW (typ.) (f = 50MHz)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

HM6708P



(DP-24NC)

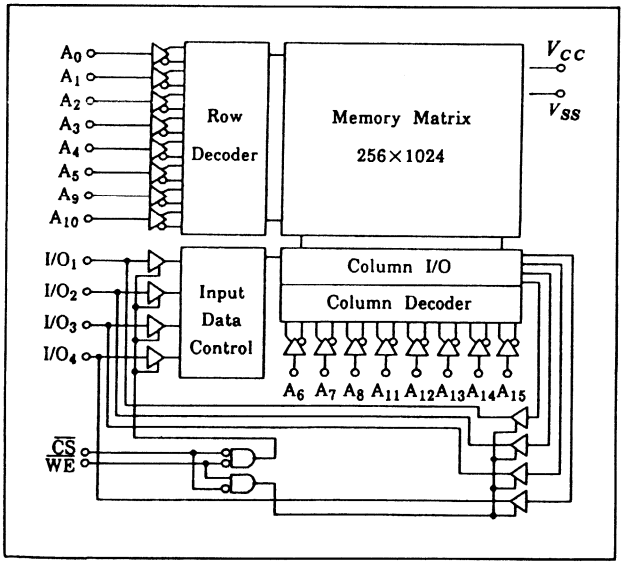
HM6708JP

(CP-24D)

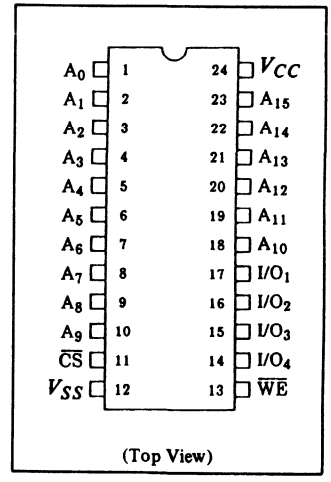
Ordering Information

Type No.	Access Time	Package
HM6708P-20	20ns	300mil 24 pin
HM6708P-25	25ns	Plastic DIP
HM6708JP-20	20ns	300 mil
HM6708JP-25	25ns	24 pin Plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0 V for pulse width 20ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle

DC and Operating Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC}-0.2$ V $V_{IN} \leqq 0.2$ V or $V_{IN} \geqq V_{CC}-0.2$V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4 mA

Capacitance (T_a = 25°C, f = 1 MHz)

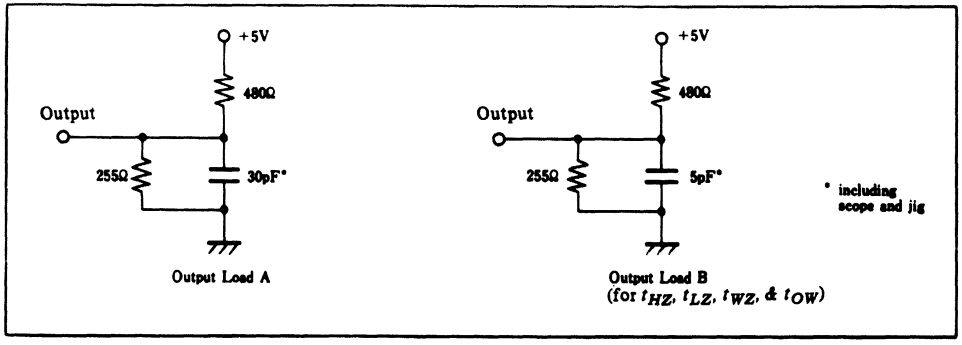
Item	Symbol	max.	Unit	Test Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0 V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C, unless otherwise noted)

AC Test Conditions

- Input pulse levels : V_{SS} to 3.0 V
- Input timing reference levels : 1.5 V
- Output Load : See Figure
- Input rise and fall times : 4 ns
- Output reference levels : 1.5 V

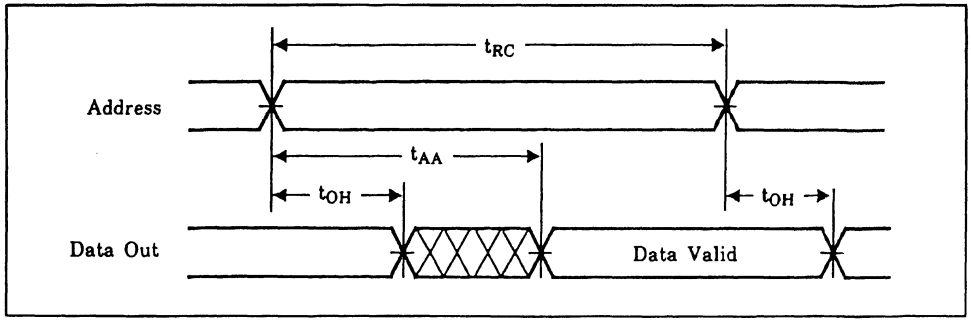


Read Cycle

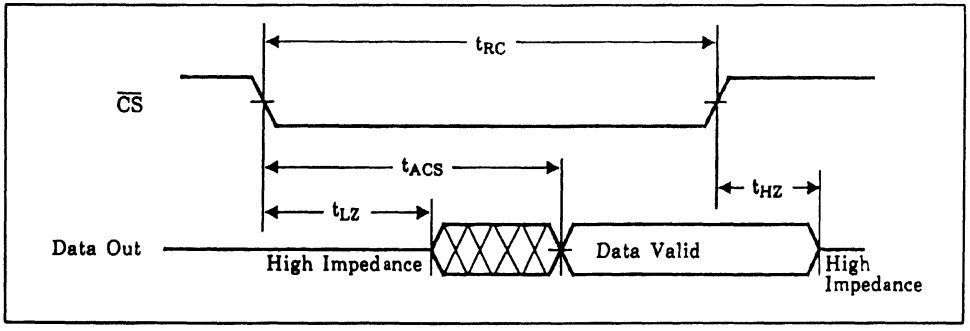
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	20	–	25	–	ns	–
Address Access Time	t_{AA}	–	20	–	25	ns	–
Chip Select Access Time	t_{ACS}	–	20	–	25	ns	–
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Chip Selection to Output in Low Z	t_{LZ}	0	–	0	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	10	ns	1, 2

Note) 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

Read Cycle-1*1,*2



Read Cycle-2*1,*3



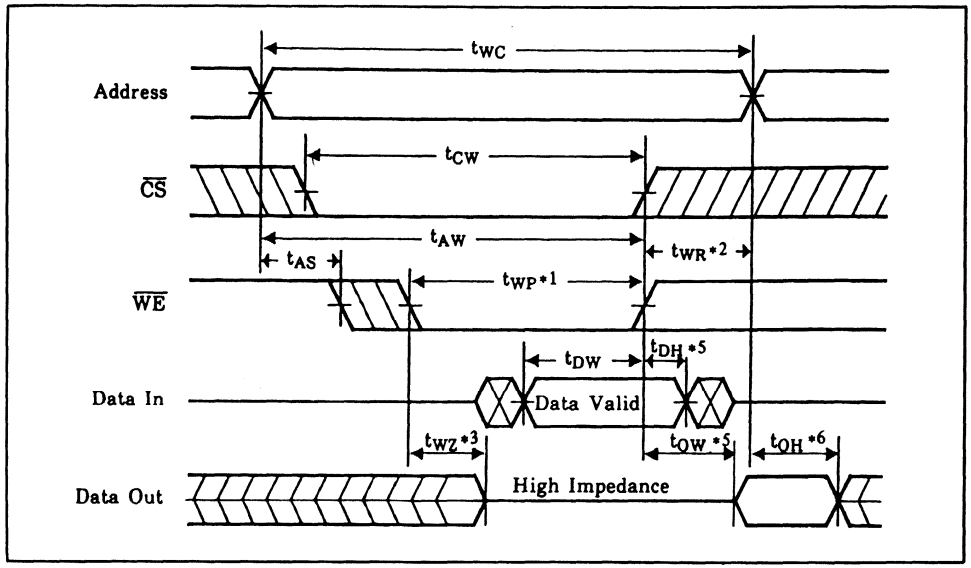
Notes) *1. $\overline{WE}$ is High for Read cycle.
*2. Device is continuously selected, $\overline{CS} = V_{IL}$.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

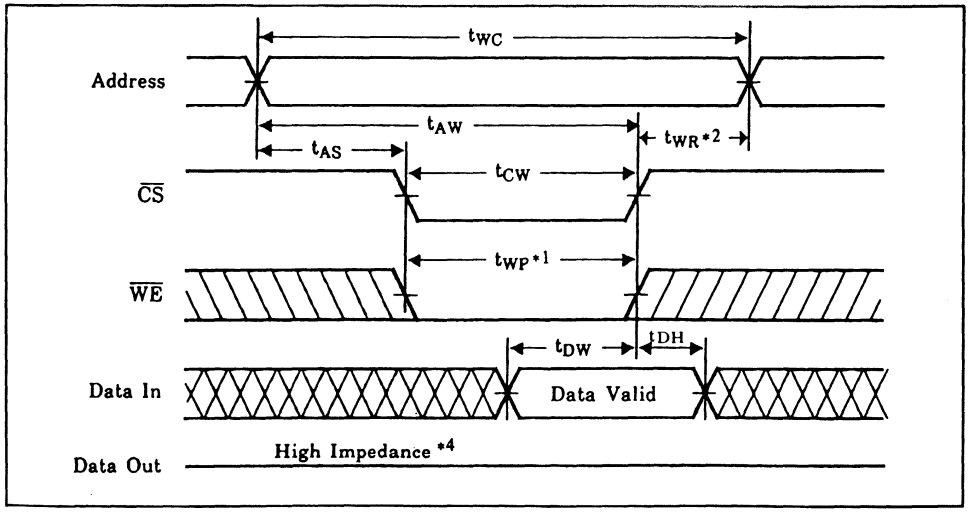
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	20	–	25	–	ns	2
Chip Selection to End of Write	t_{CW}	15	–	20	–	ns	–
Address Valid to End of Write	t_{AW}	15	–	20	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Write Pulse Width	t_{WP}	15	–	20	–	ns	–
Write Recovery Time	t_{WR}	1.5	–	3	–	ns	–
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	–
Data Hold Time	t_{DH}	0	–	0	–	ns	–
Write Enable to Output in High Z	t_{WZ}	0	8	0	10	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).
4. This parameter is sampled and not 100% tested.

Write Cycle-1 ($\overline{WE}$ Controlled)



Write Cycle-2 ($\overline{CS}$ Controlled)



Note) *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Output is the same phase of write data of this write cycle.

HM6709 Series — Preliminary

65536-word × 4-bit High Speed Hi-BICMOS Static RAM (with $\overline{OE}$)

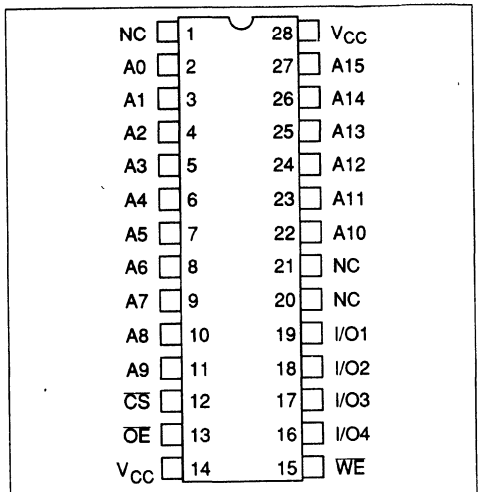
Features

- Super fast access time: 20/25 ns (max)
- Fast-$\overline{OE}$ access time: 10 ns (max)
- Low power dissipation: 350 mW (typ)
- + 5 V single supply
- Completely static memory
- No clock or timing strobe required
- Fully TTL compatible input and output
- 300 mil 28 pin SOJ

Ordering Information

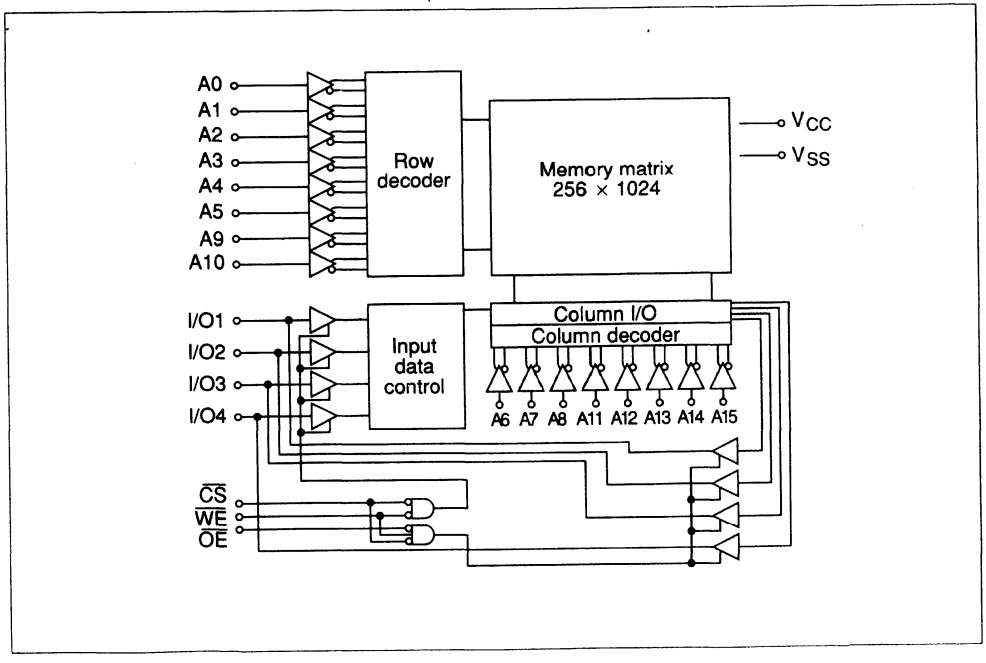
Type No.	Access Time	Package
HM6709JP-20	20ns	300 mil 28 pin plastic SOJ (CP-28DN)
HM6709JP-25	25 ns	

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage to V_{SS} pin	V_T	–0.5 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range (with bias)	Tstg (bias)	–10 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Recommended DC Operating Condtions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input high voltage	V_{IH}	2.2	—	6.0	V
Input low voltage	V_{IL}	–3.0*1	—	0.8	V

Note: *1 Pulse width: 20 ns, DC: –0.5 V

Truth Table

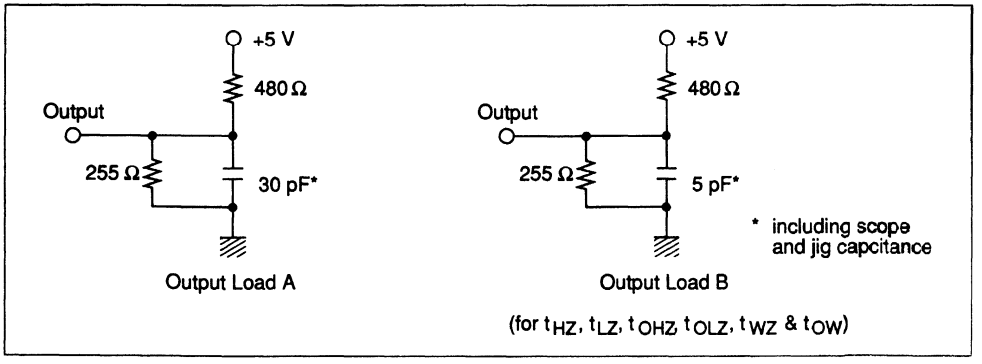
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} current	I/O pin	Ref. cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	H	Output disabled	I_{CC}, I_{CC1}	High-Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data out	Read cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data in	Write cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data in	Write cycle (5) (6)

DC and Operating Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	V_{CC} = 5.5 V, V_{IN} = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	—	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	I_{CC1}	—	—	120	mA	Min cycle, duty: 100%, $I_{I/O}$ = 0 mA
Standby power supply current	I_{SB}	—	—	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	—	—	10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4 mA

AC Test Conditions

- Input pulse levels : V_{SS} to 3.0 V
- Input rise and fall time : 4 ns
- Input and output reference levels : 1.5 V
- Output load : See figure



Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test conditons
Input capacitance	C_{IN}	—	—	6	pF	V_{IN} = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C, unless otherwise noted.)

Read Cycle

		HM6709JP-20		HM6709JP-25			
Item	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	20	—	25	—	ns	—
Address access time	t_{AA}	—	20	—	25	ns	—
Chip select access time	t_{ACS}	—	20	—	25	ns	—
Chip selection to output in low Z	t_{LZ}	0	—	0	—	ns	1, 2
Output enable to output valid	t_{OE}	0	10	0	10	ns	—
Output enable to output in low Z	t_{OLZ}	0	—	0	—	ns	1, 2
Chip deselection to output in high Z	t_{HZ}	0	8	0	10	ns	1, 2
Output hold from address change	t_{OH}	5	—	5	—	ns	—

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in load (B).

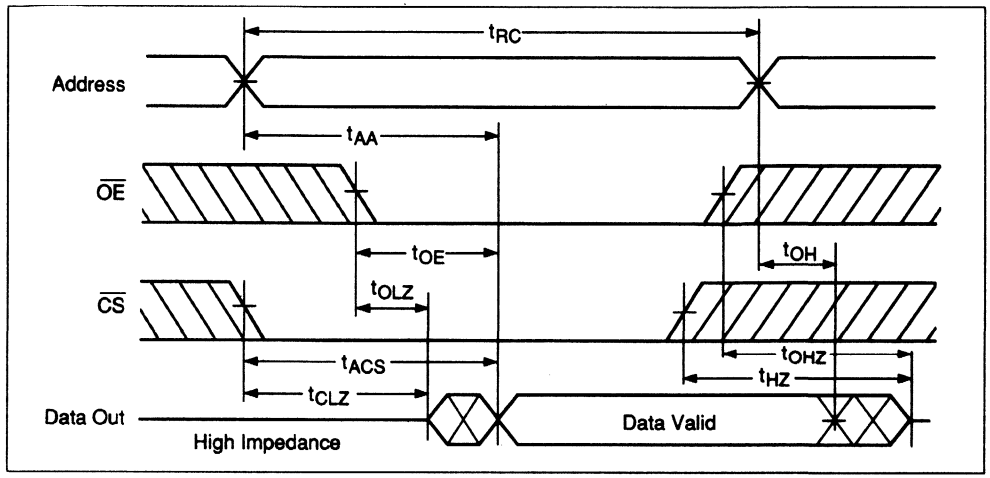
Write Cycle

Item	Symbol	HM6709JP-20 Min	HM6709JP-20 Max	HM6709JP-25 Min	HM6709JP-25 Max	Unit	Notes
Write cycle time	t_{WC}	20	—	25	—	ns	1
Chip selection to end of write	t_{CW}	15	—	20	—	ns	—
Address setup time	t_{AS}	0	—	0	—	ns	—
Address valid to end of write	t_{AW}	15	—	20	—	ns	—
Write pulse width	t_{WP}	15	—	20	—	ns	—
Write recovery time	t_{WR}	1.5	—	1.5	—	ns	—
Write to output in high Z	t_{WZ}	0	8	0	10	ns	2, 3
Data valid to end of write	t_{DW}	12	—	15	—	ns	—
Data hold time	t_{DH}	0	—	0	—	ns	—
Output disable to output in high Z	t_{OHZ}	0	8	0	10	ns	2, 3
Output active from end of write	t_{OW}	0	—	0	—	ns	2, 3

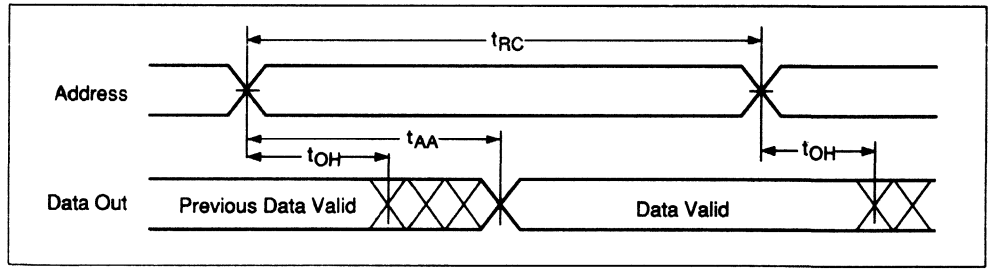
Notes: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 200 mV from steady state voltage with specified loading in load (B).

Timing Waveform

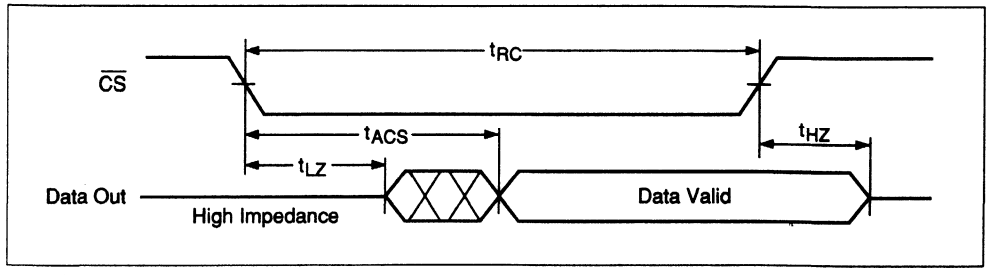
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

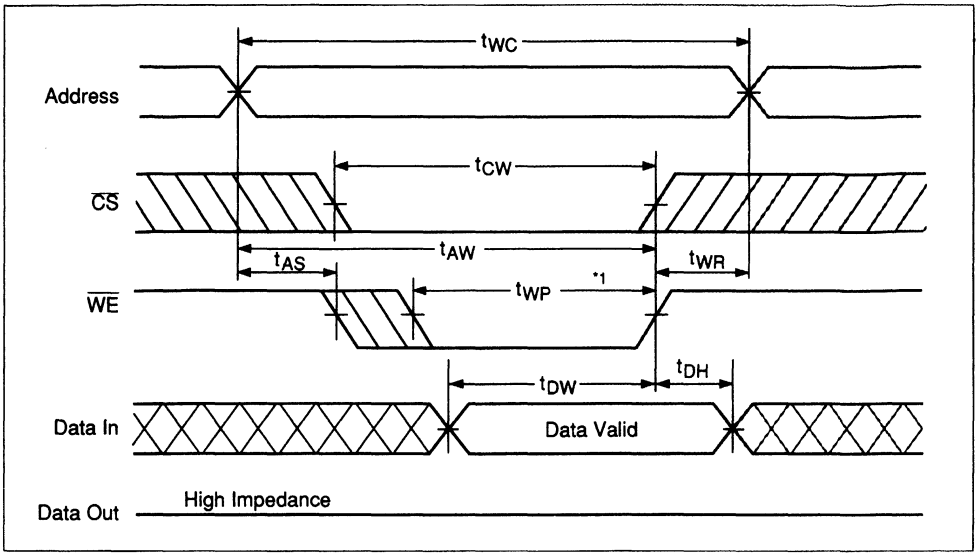


Read Cycle (3) *1, *3, *4

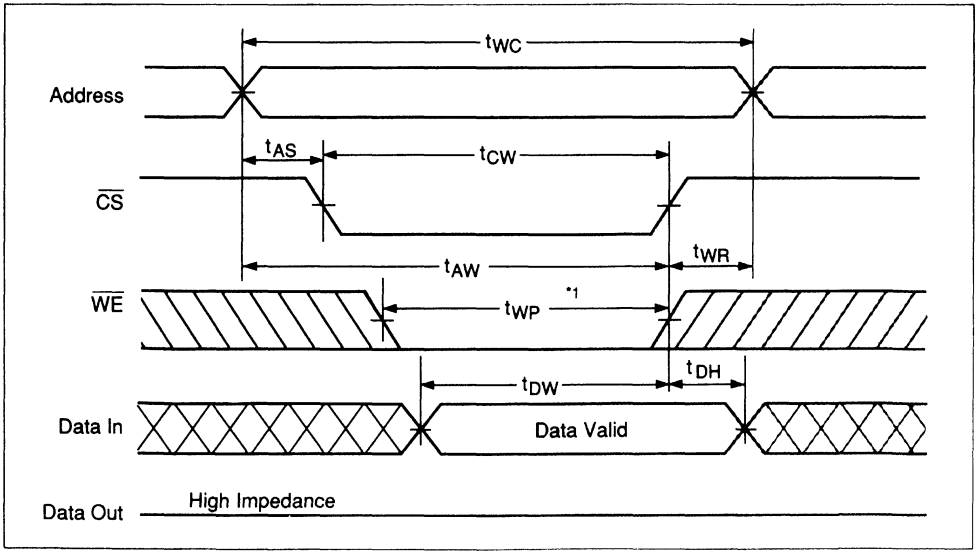


Notes: 1. $\overline{WE} = V_{IH}$
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$
4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

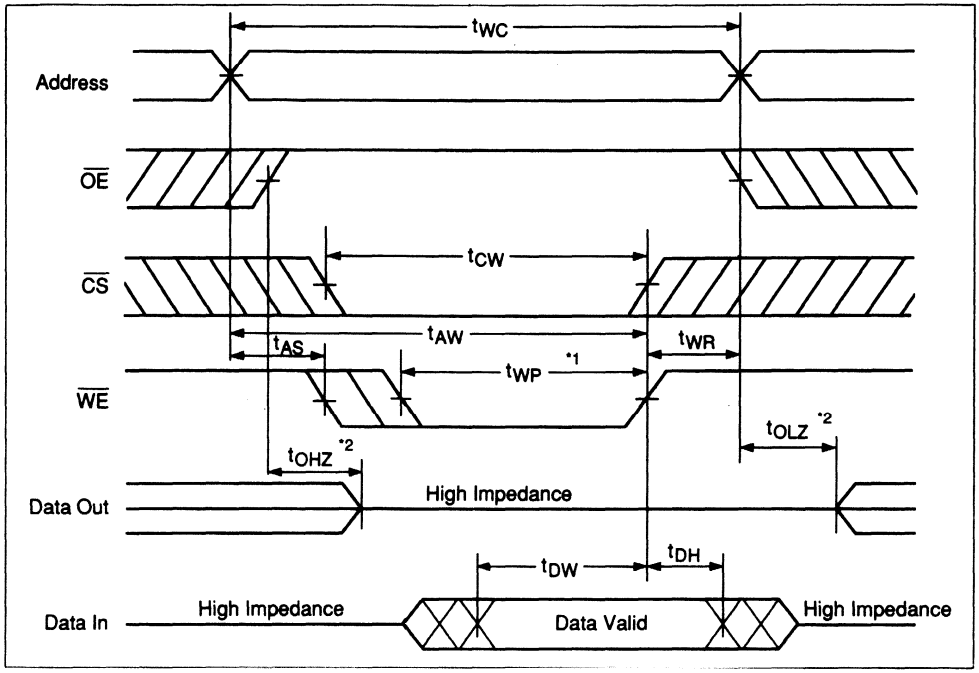
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



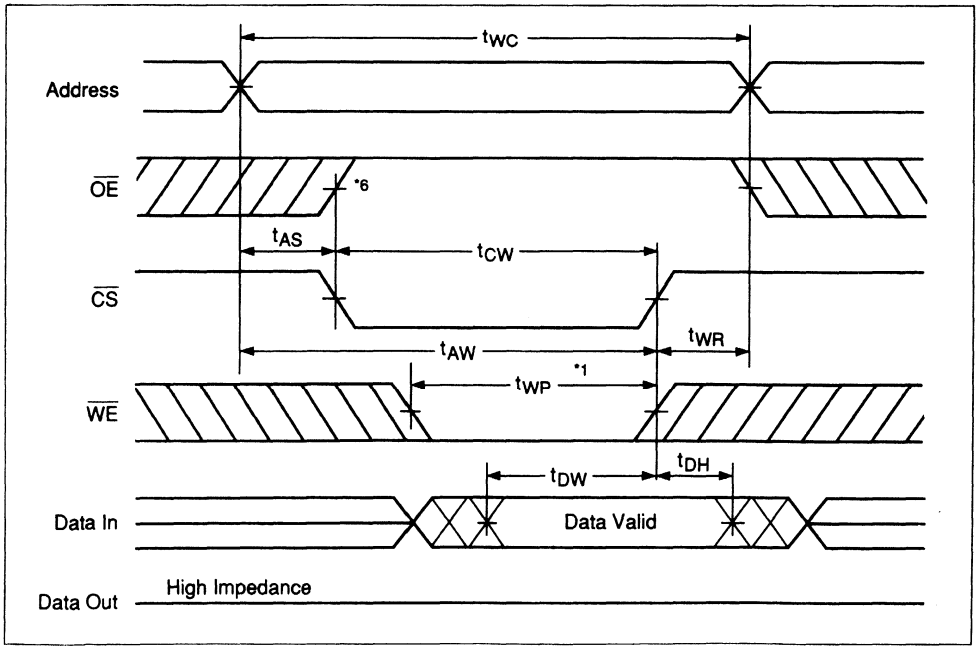
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



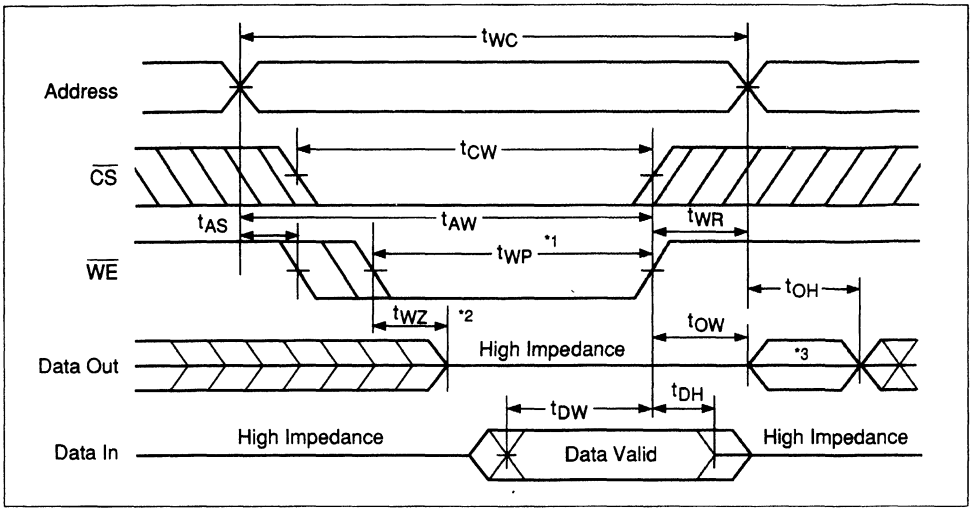
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



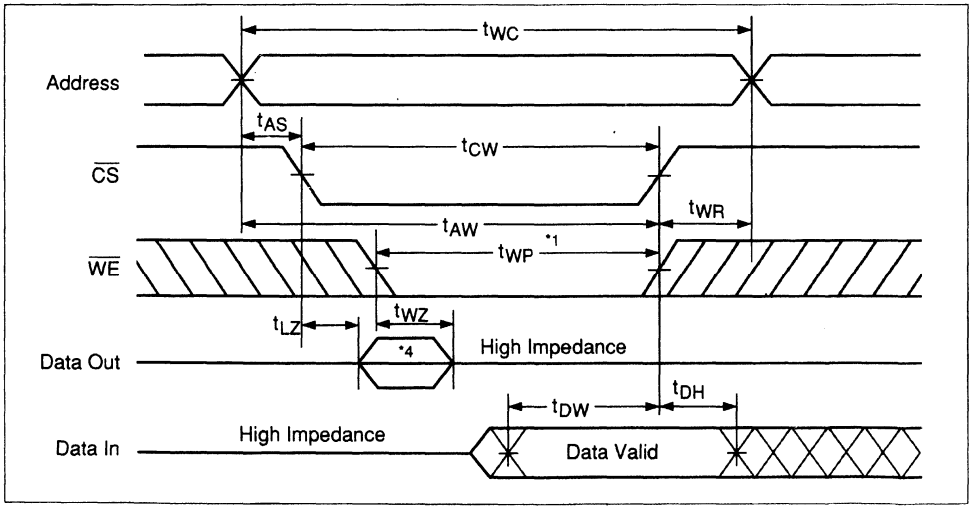
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of oppossite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state.Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6207 Series
HM6207H Series

262144-Word × 1-Bit High Speed CMOS Static RAM

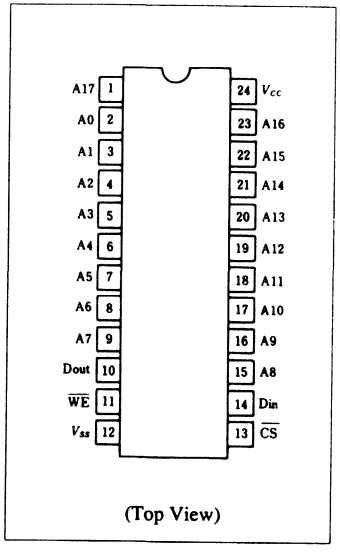
Features

- Single 5 V supply and high density 24-pin package
- High speed
  - Access time: 25/35/45 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ)
  - 30 µW (typ) (L-version)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible
  - All inputs and outputs
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6207HP-25	25 ns	300-mil
HM6207HP-35	35 ns	24-pin
HM6207P-35	35 ns	Plastic DIP
HM6207P-45	45 ns	(DP-24NC)
HM6207HLP-25	25 ns	
HM6207HLP-35	35 ns	
HM6207LP-35	35 ns	
HM6207LP-45	45 ns	
HM6207HJP-25	25 ns	300-mil
HM6207HJP-35	35 ns	24-pin
HM6207HLJP-25	25 ns	SOJ
HM6207HLJP-35	35 ns	(CP-24D)

Pin Arrangement

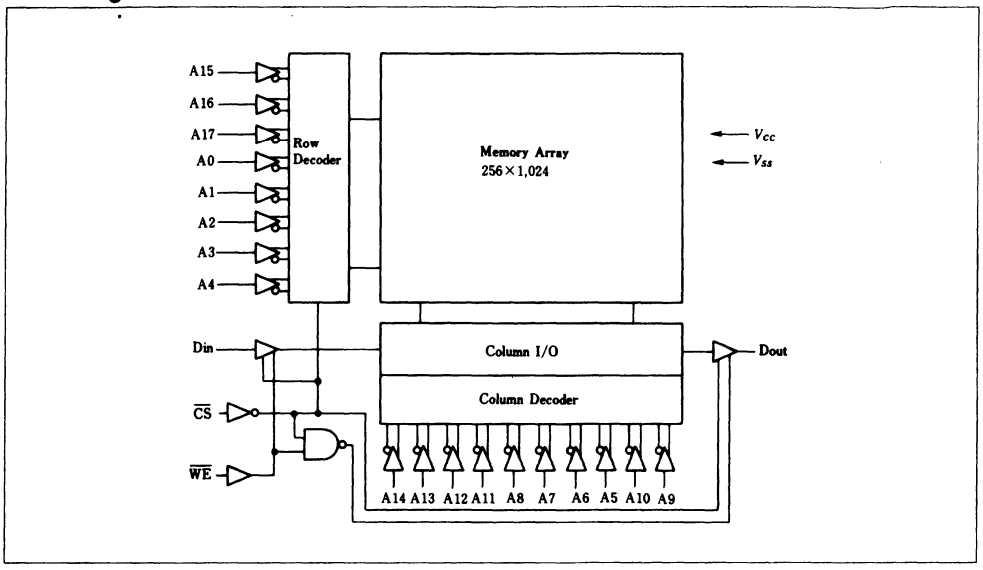


(Top View)

Pin Description

Pin Name	Function
A0 – A17	Address
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	High-Z	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM6207H-25			HM6207-35 HM6207-45 HM6207H-35			Unit	Test Conditions	Note
		Min	Typ*1	Max	Min	Typ*1	Max			
Input leakage current	I_{LI}	—	—	2.0	—	—	2.0	µA	V_{CC}=Max Vin=Vss to V_{CC}	
Output leakage current	I_{LO}	—	—	10.0	—	—	10.0	µA	$\overline{CS}$=V_{IH} $V_{I/O}$=Vss to V_{CC}	
Operating power supply current	I_{CC}	—	60	120	—	50	100	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA Min cycle duty=100%	
	I_{CC1}	—	40	80	—	40	80	mA	$\overline{CS}$=V_{IL}, $I_{I/O}$=0 mA tcycle=50 ns duty=100%	
Standby power supply current	I_{SB}	—	20	40	—	15	30	mA	$\overline{CS}$=V_{IH}, Min cycle	
Standby power supply current(1)	I_{SB1}	—	0.02	2.0	—	0.02	2.0	mA	$\overline{CS}$>V_{CC} -0.2 V 0 V≤Vin< 0.2 V or	
		—	0.006	0.1	—	0.006	0.1		Vin≥V_{CC} -0.2 V	L-Version
Output low voltage	V_{OL}	—	—	0.4	—	—	0.4	V	I_{OL}=8 mA	
Output high voltage	V_{OH}	2.4	—	—	2.4	—	—	V	I_{OH}=-4.0 mA	

Note: *1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	Vout = 0 V

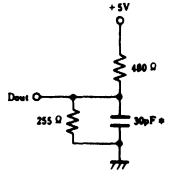
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

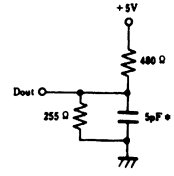
- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B)

(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



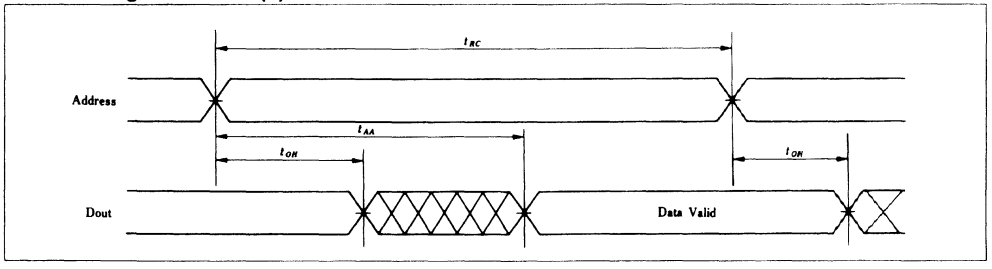
Note: * Including scope & jig.

Read cycle

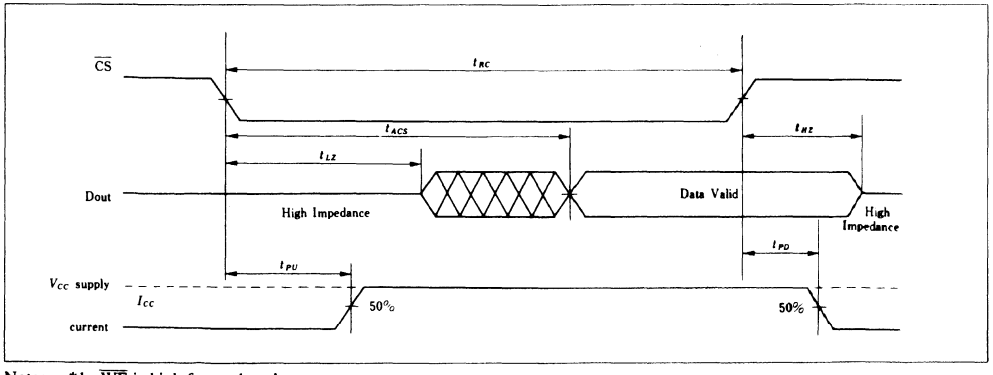
Item	Symbol	HM6207H-25		HM6207-35 HM6207H-35		HM6207-45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
Chip select access time	t_{ACS}	—	25	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	12	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	15	—	25	—	30	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



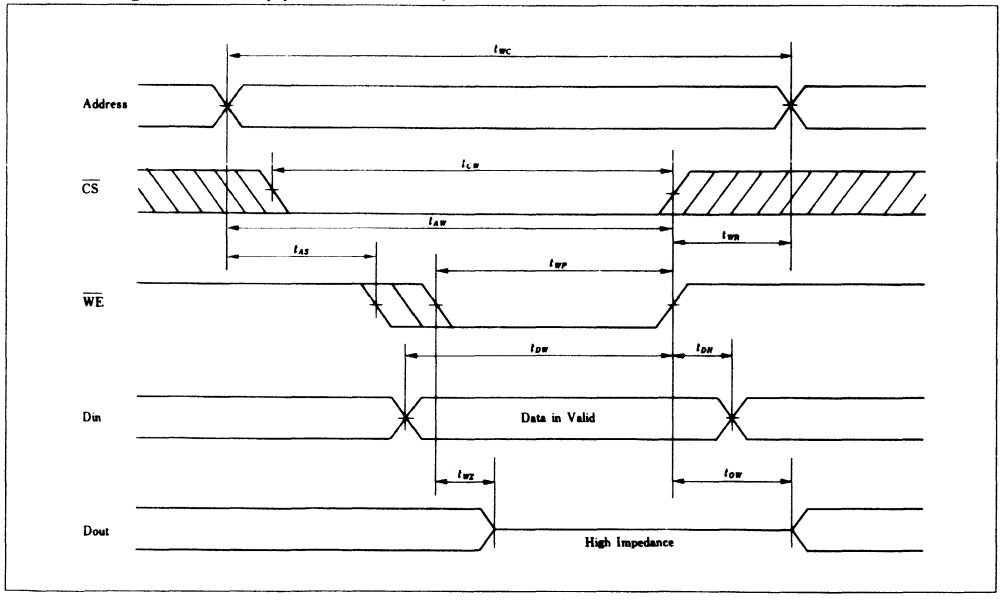
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

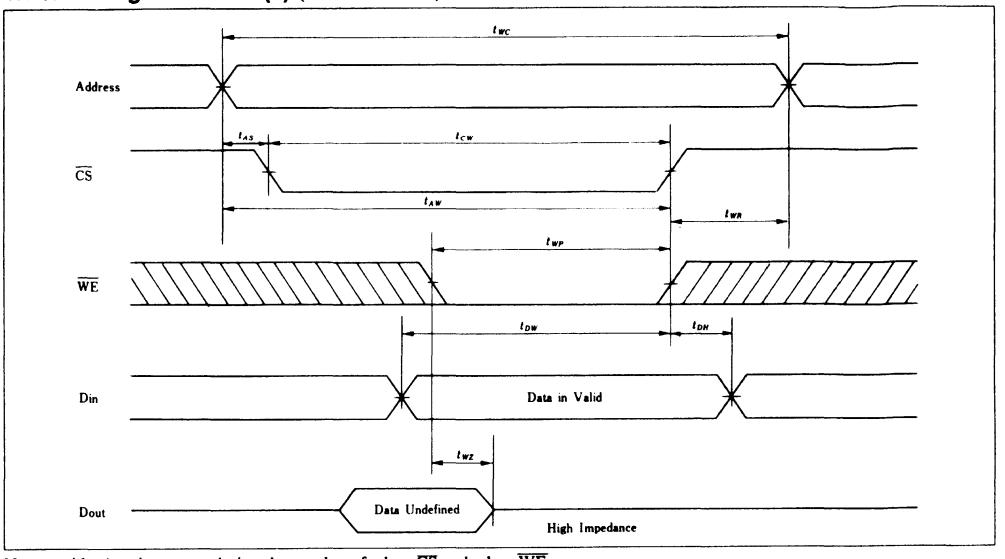
Item	Symbol	HM6207H-25		HM6207-35 HM6207H-35		HM6207-45		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	twc	25	—	35	—	45	—	ns
Chip selection to end of write	tcw	20	—	30	—	40	—	ns
Address valid to end of write	taw	20	—	30	—	40	—	ns
Address setup time	tas	0	—	0	—	0	—	ns
Write pulse width	twp	20	—	25	—	25	—	ns
Write recovery time	twr	3	—	3	—	3	—	ns
Data valid to end of write	tdw	15	—	20	—	20	—	ns
Data hold time	tdh	0	—	0	—	0	—	ns
Write enabled to output in high-Z	twz*1	0	8	0	10	0	15	ns
Output active from end of write	tow*1	0	—	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

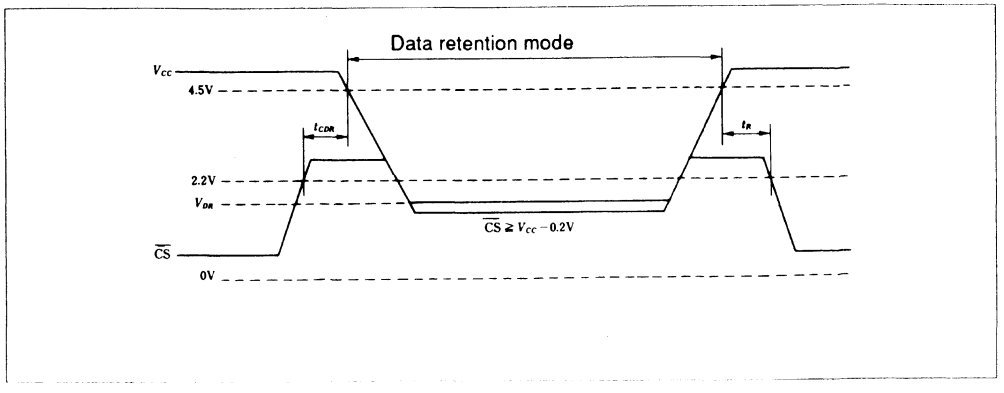
Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ V_{CC} – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	2	50*1	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: *1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform



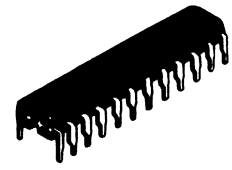
HM6707 Series

262144-word x 1-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 20/25ns (max.)
- Low Power Dissipation
  Operating: 350mW (typ.) (f = 50MHz)
- +5V Single Supply
- Completely Static Memory
- No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

HM6707P



(DP-24NC)

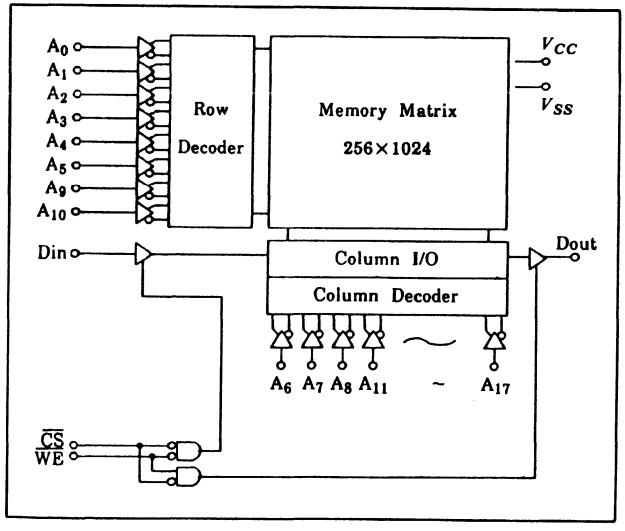
HM6707JP

(CP-24D)

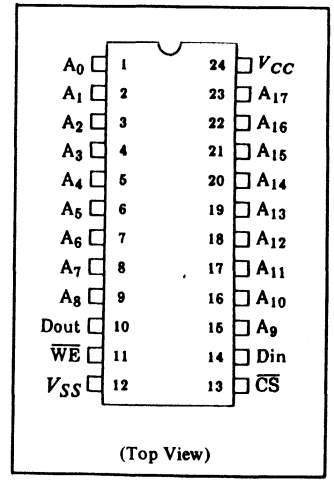
Ordering Information

Type No.	Access Time	Package
HM6707P-20	20ns	300mil 24 pin
HM6707P-25	25ns	Plastic DIP
HM6707JP-20	20ns	300 mil
HM6707JP-25	25ns	24 pin Plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.5*1	–	0.8	V

Note) *1 : -3.0 V for pulse width 20ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	D_{out}
L	L	Write	I_{CC}, I_{CC1}	High Z

DC and Operating Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC}=5.5 V, V_{IN}=V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH}, V_{OUT}=V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, I_{OUT}=0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty : 100%, I_{OUT}=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC}−0.2 V V_{IN} ≦ 0.2 V or V_{IN} ≧ V_{CC}−0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

Capacitance (T_a = 25°C, f = 1 MHz)

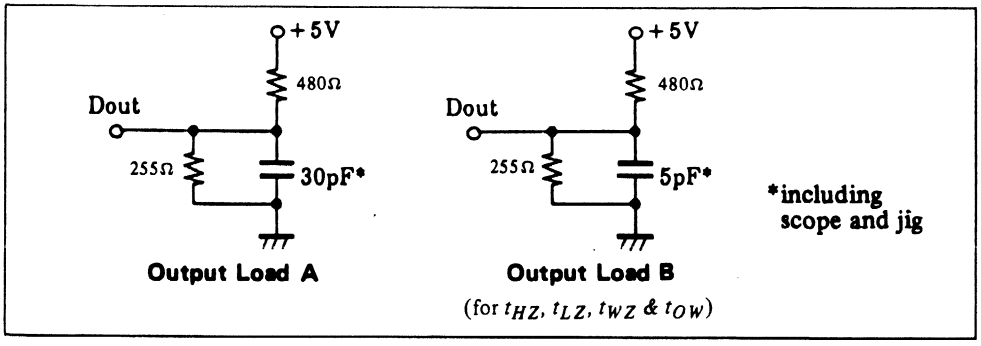
Item	Symbol	max.	Unit	Test Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0 V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0 V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C, unless otherwise noted)

AC Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels : 1.5 V
- Output Load : See Figure
- Input rise and fall times : 4 ns
- Output reference levels : 1.5 V

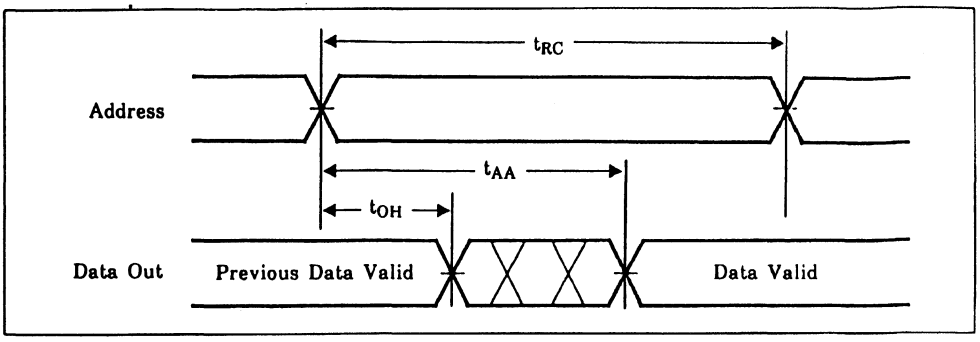


Read Cycle

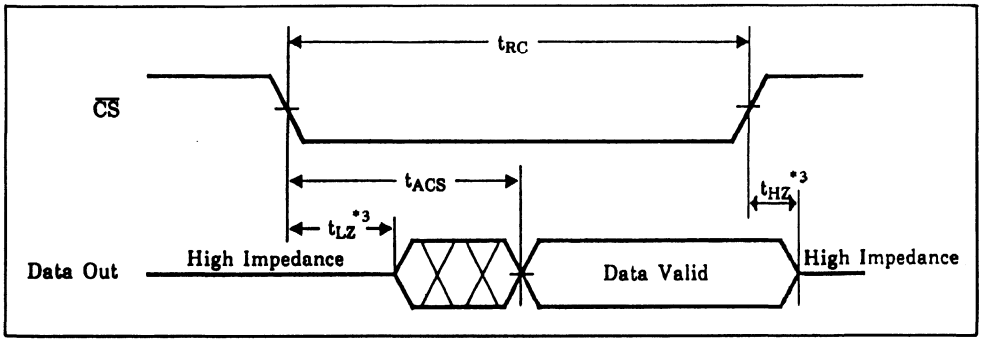
Item	Symbol	HM6707-20		HM6707-25		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	20	–	25	–	ns	–
Address Access Time	t_{AA}	–	20	–	25	ns	–
Chip Select Access Time	t_{ACS}	–	20	–	25	ns	–
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	15	ns	1, 2

Note) 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

Read Cycle-1*1



Read Cycle-2*2



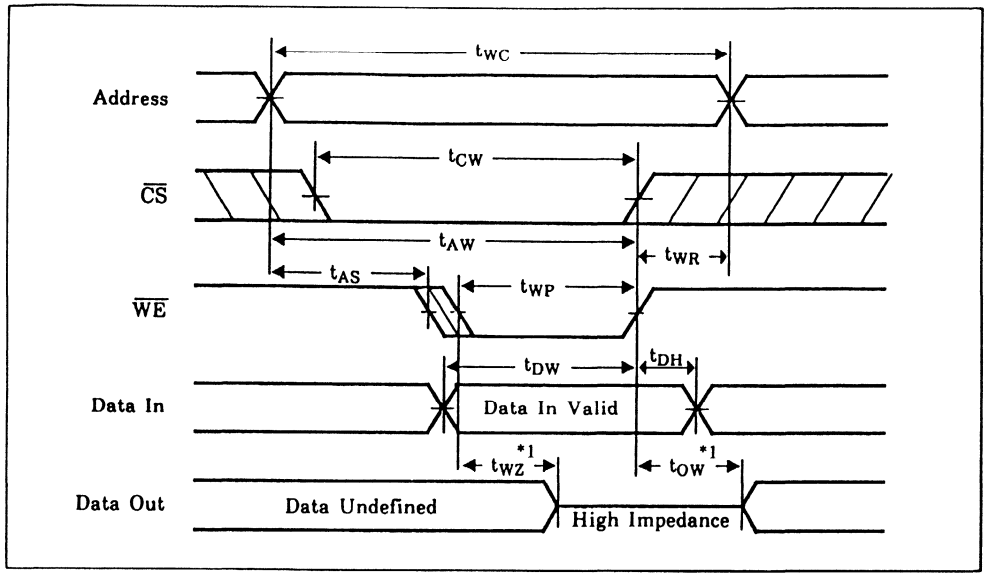
Notes) *1. $\overline{WE}$ is high and $\overline{CS}$ is low for Read cycle.
*2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
*3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

Write Cycle

Item	Symbol	HM6707-20		HM6707-25		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	20	–	25	–	ns	2
Chip Selection to End of Write	t_{CW}	15	–	20	–	ns	–
Address Valid to End of Write	t_{AW}	15	–	20	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Write Pulse Width	t_{WP}	15	–	20	–	ns	–
Write Recovery Time	t_{WR}	1.5	–	3	–	ns	–
Data Valid to End of Write	t_{DW}	15	–	20	–	ns	–
Data Hold Time	t_{DH}	0	–	0	–	ns	–
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

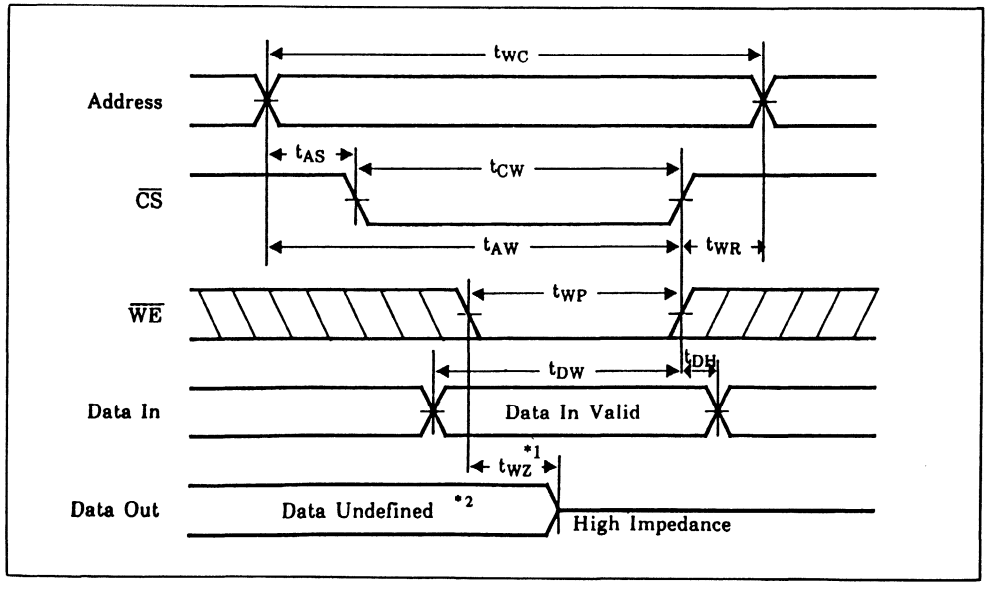
Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).
4. This parameter is sampled and not 100% tested.

Write Cycle-1 ($\overline{WE}$ Controlled)



Note) *1. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).

Write Cycle-2 ($\overline{CS}$ Controlled)



Note) *1. Transition is measured ±200 mV from steady state voltage with specified loading in Load (B).
*2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer remains in a high impedance state.

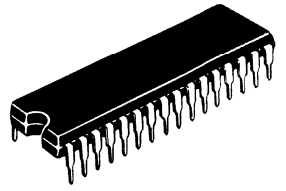
HM628128 Series

131072-Word × 8-Bit High Speed CMOS Static RAM

The Hitachi HM628128 is a CMOS static RAM organized 128-kword x 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

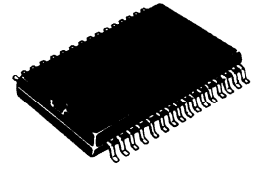
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, is available for high density mounting.

HM628128P Series



(DP-32)

HM628128FP Series



(FP-32D)

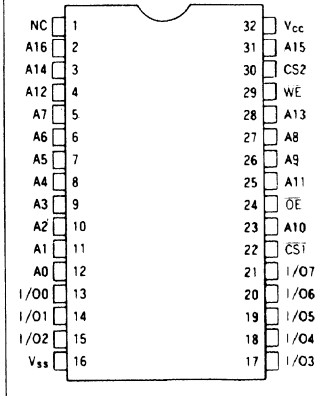
Features

- High speed: Fast access time 70/85/100/120 ns (max.)
- Low power
  - Standby: 10 μW (typ) (L-/L-SL version)
  - Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-/L-SL version)
  - 2 chip selection for battery back up

Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
Vcc	Power supply
Vss	Ground

Pin Arrangement



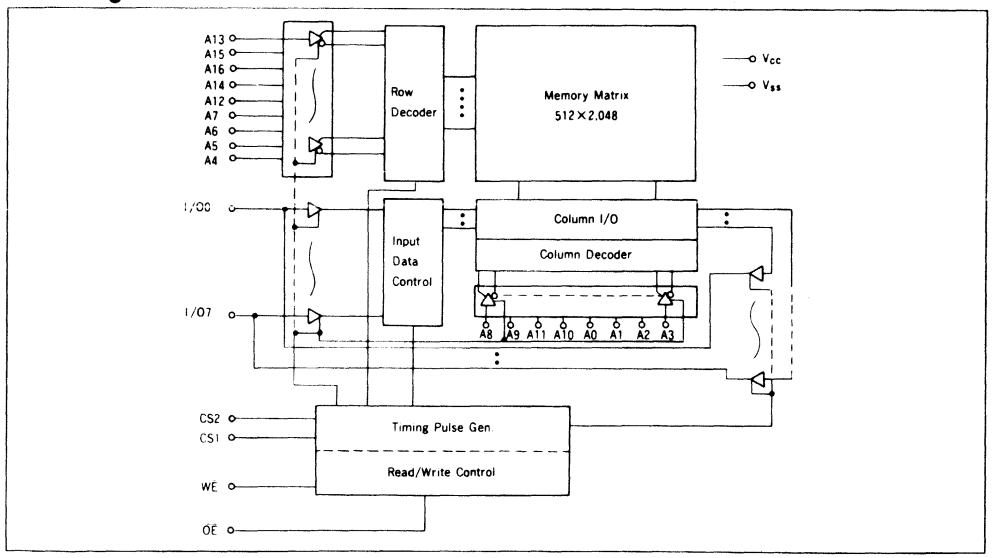
(Top View)

Ordering Information

Type No.	Access Time	Package
HM628128P-7	70 ns	600 mil 32-pin plastic DIP (DP-32)
HM628128P-8	85 ns	
HM628128P-10	100 ns	
HM628128P-12	120 ns	
HM628128LP-7	70 ns	
HM628128LP-8	85 ns	
HM628128LP-10	100 ns	
HM628128LP-12	120 ns	
HM628128LP-7SL	70 ns	
HM628128LP-8SL	85 ns	
HM628128LP-10SL	100 ns	
HM628128LP-12SL	120 ns	

Type No.	Access Time	Package
HM628128FP-7	70 ns	525 mil 32-pin plastic DIP (FP-32D)
HM628128FP-8	85 ns	
HM628128FP-10	100 ns	
HM628128FP-12	120 ns	
HM628128LFP-7	70 ns	
HM628128LFP-8	85 ns	
HM628128LFP-10	100 ns	
HM628128LFP-12	120 ns	
HM628128LFP-7SL	70 ns	
HM628128LFP-8SL	85 ns	
HM628128LFP-10SL	100 ns	
HM628128LFP-12SL	120 ns	

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
×	H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	
×	×	L	×		I_{SB}, I_{SB1}	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V	
Input low (logic 0) voltage	V_{IL}	−0.3*1	—	0.8	V	

Note: *1. −3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$= Vss to Vcc
Operating power supply current: DC	I_{CC}	—	15	35	mA	$\overline{CS1}$= V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$= 0 mA
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	I_{CC2}	—	15	30	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS1}$ ≤ 0.2 V, CS2 ≥Vcc − 0.2 V V_{IH} ≥ Vcc − 0.2V, V_{IL} ≤ 0.2V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}
Standby power supply current (1): DC	I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V $\overline{CS1}$ ≥ Vcc − 0.2 V, CS2 ≥ Vcc − 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		—	2*2	100*2	µA	
		—	2*3	50*3	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Notes: *1. Typical values are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted)

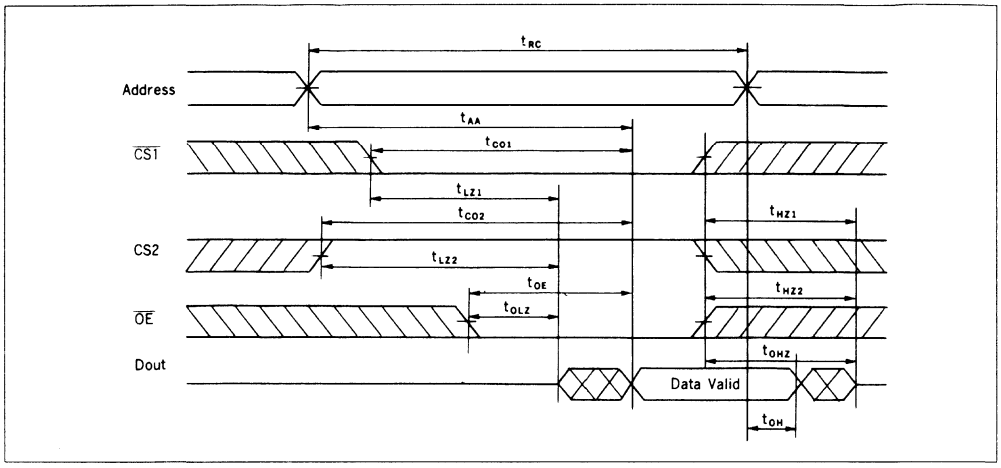
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100pF) (Including scope & jig)

Read Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns	
Chip selection ($\overline{CS1}$) to output valid	t_{CO1}	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	t_{CO2}	—	70	—	85	—	100	—	120	ns	
Output enable ($\overline{OE}$) to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns	
Chip selection ($\overline{CS1}$) to output in low-Z	t_{LZ1}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Chip selection (CS2) to output in low-Z	t_{LZ2}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Output enable ($\overline{OE}$) to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	*1, *2, *3
Chip deselection ($\overline{CS1}$) to output in high-Z	t_{HZ1}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Chip deselection (CS2) to output in high-Z	t_{HZ2}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output disable ($\overline{OE}$) to output in high-Z	t_{OHZ}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

Read Timing Waveform*4

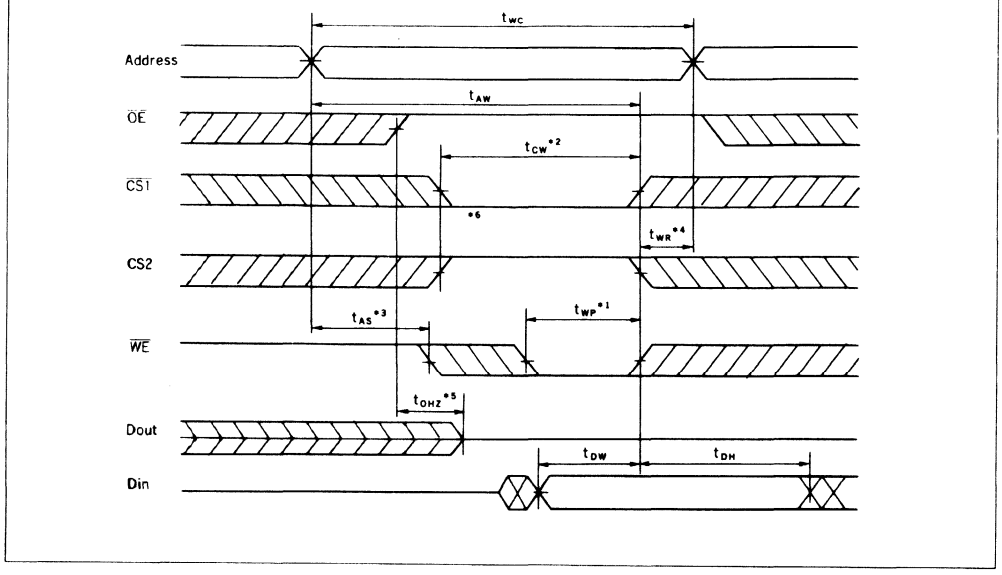


Notes: *1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
*2. At any given temperature and voltage condition, tHZ max is less than tLZ min both for a given device and from device to device.
*3. This parameter is sampled and not 100% tested.
*4. $\overline{WE}$ is high for read cycle.

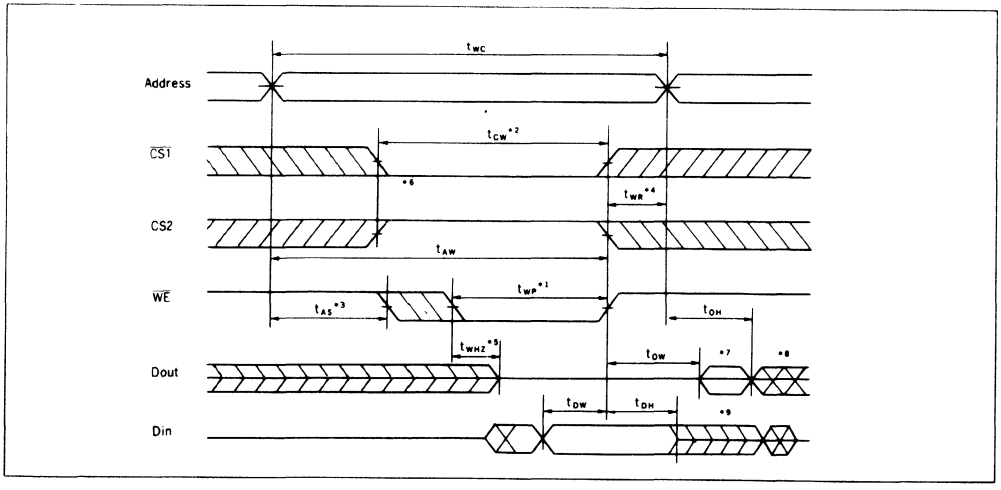
Write Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	twc	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	tcw	60	—	75	—	80	—	85	—	ns	
Address setup time	tAS	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	taw	60	—	75	—	80	—	85	—	ns	
Write pulse width	twp	50	—	55	—	60	—	70	—	ns	
Write recovery time	twR	5	—	5	—	5	—	10	—	ns	
		10	—	10	—	10	—	15	—	ns	*11
Write to output in high-Z	twHZ	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	tDW	30	—	35	—	40	—	45	—	ns	
Write hold from write time	tDH	0	—	0	—	0	—	0	—	ns	
Output active from end of write	tow	5	—	5	—	5	—	5	—	ns	*10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fix)



Notes: *1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

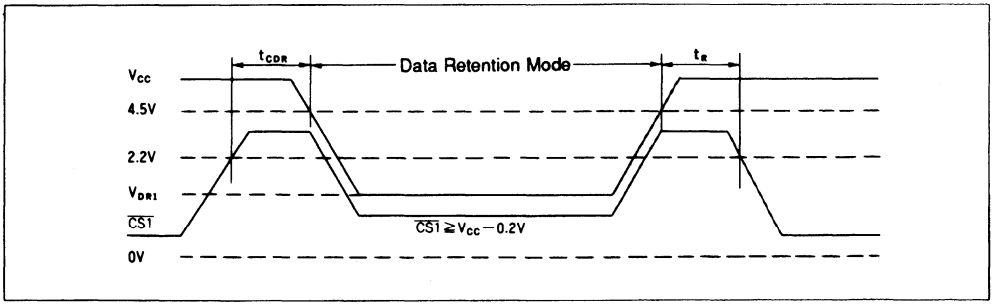
*6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
*7. Dout is the same phase of the latest written data in this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
*10. This parameter is sampled and not 100% tested.
*11. This value is measured from CS2 going low to the end of write cycle.

Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

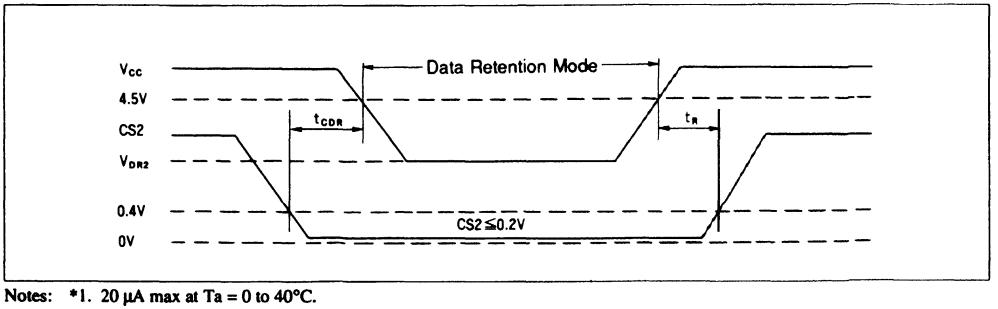
(This characteristics is guaranteed only for L-and L-SL version.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions*3
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq Vcc - 0.2$ V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V Vin ≥ 0 V
Data retention current		—	1	50*1	µA	Vcc = 3.0 V, Vin ≥ 0 V $\overline{CS1} \geq Vcc - 0.2$ V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		—	1	15*2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation recovery time	t_R	5	—	—	ms	

Low Vcc Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)

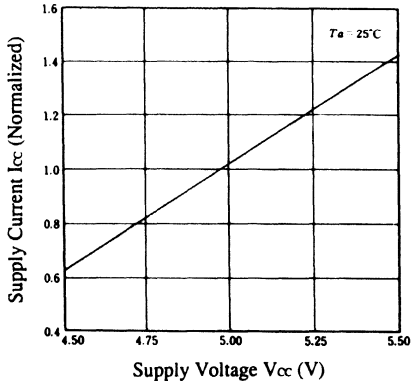


Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)

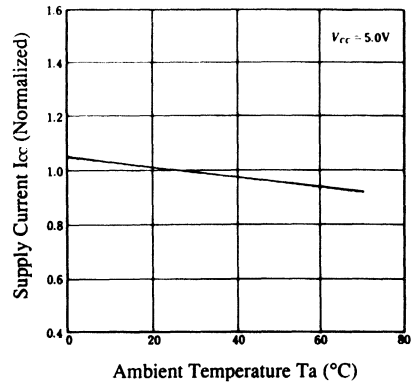


Notes: *1. 20 µA max at Ta = 0 to 40°C.
*2. 3 µA max at Ta = 0 to 40°C.
*3. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

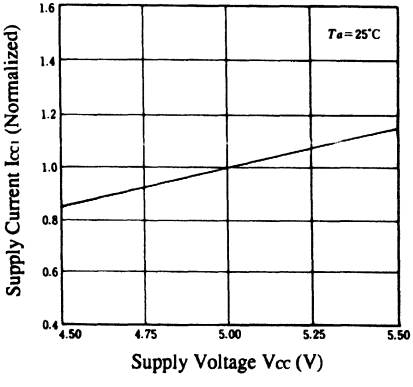
Supply Current vs. Supply Voltage (1)



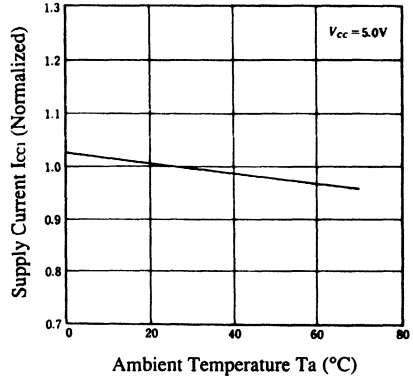
Supply Current vs. Ambient Temperature (1)



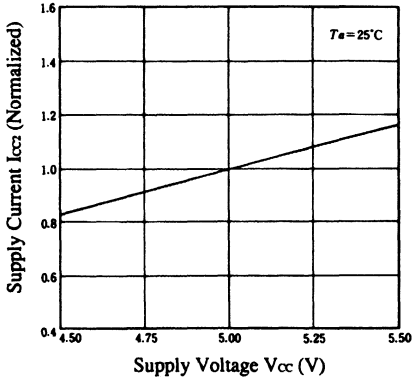
Supply Current vs. Supply Voltage (2)



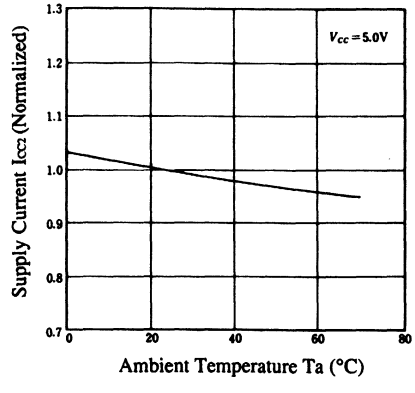
Supply Current vs. Ambient Temperature (2)



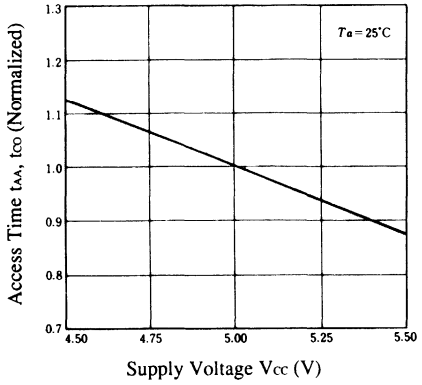
Supply Current vs. Supply Voltage (3)



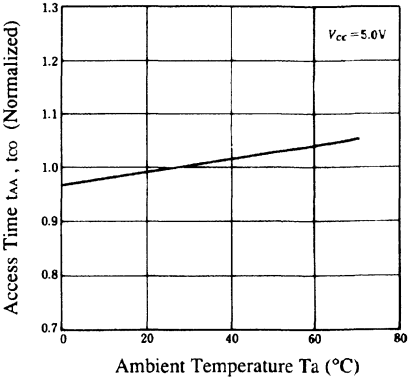
Supply Current vs. Ambient Temperature (3)



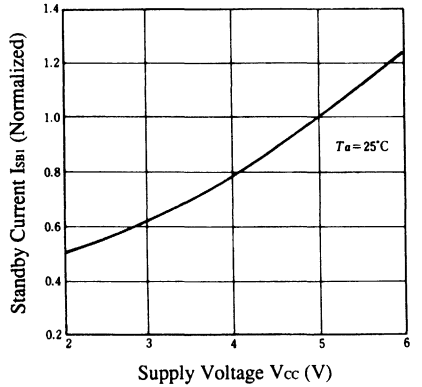
Access Time vs. Supply Voltage



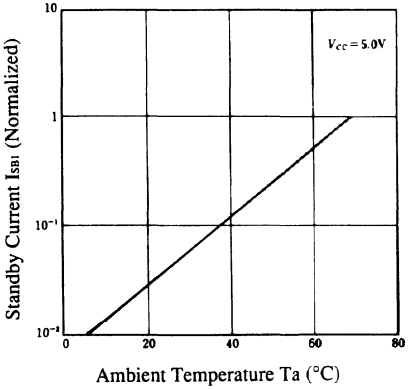
Access Time vs. Ambient Temperature



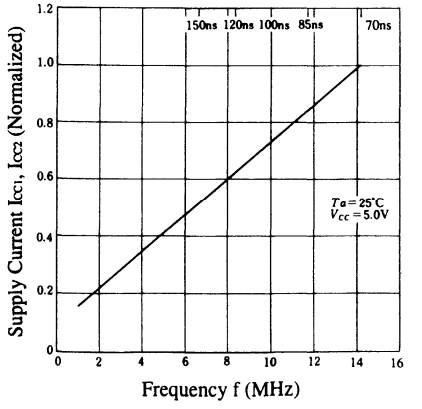
Standby Current vs. Supply Voltage



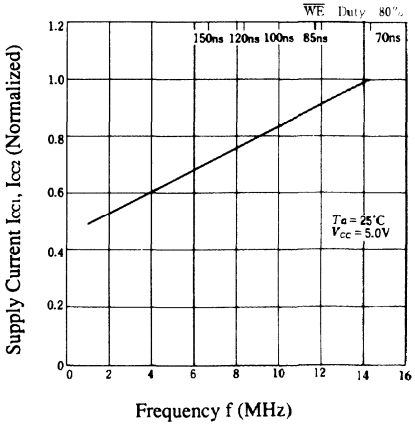
Standby Current vs. Ambient Temperature



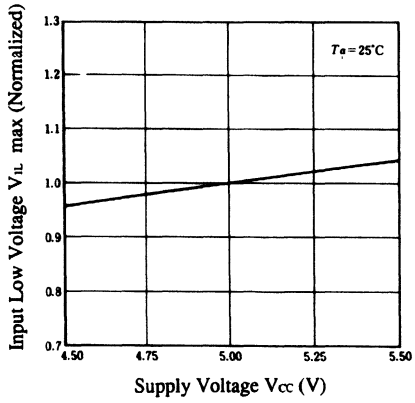
Supply Current vs. Frequency (Read)



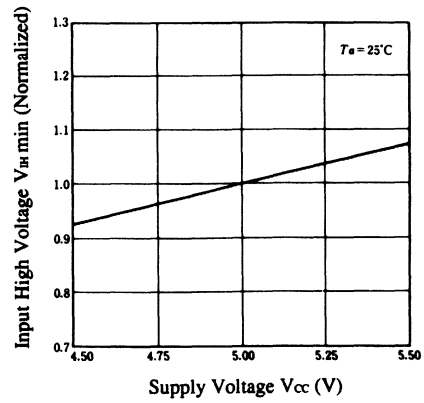
Supply Current vs. Frequency (Write)



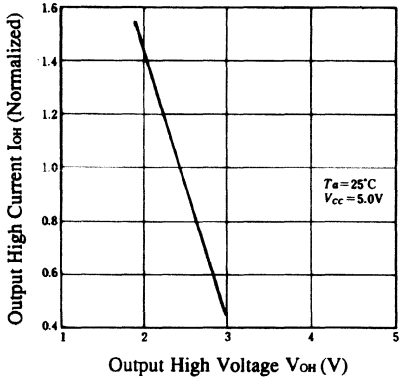
Input Low Voltage vs. Supply Voltage



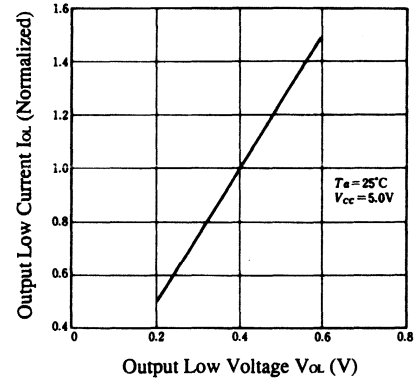
Input High Voltage vs. Supply Voltage



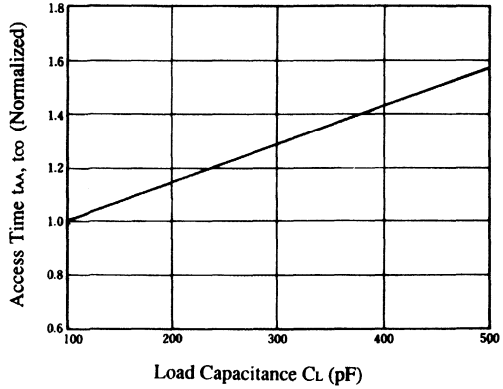
Output High Current vs. Output High Voltage



Output Low Current vs. Output Low Voltage



Access Time vs. Load Capacitance

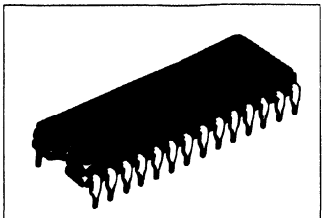


HM624256 Series

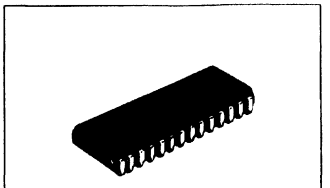
262144-Word × 4-Bit High Speed CMOS Static RAM

The Hitachi HM624256 is a high speed 1M static RAM organized as 256-kword x 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624256, packaged in a 400-mil plastic DIP and SOJ is available for high density mounting.



(DP-28C)



(CP-28D)

Features

- Single 5 V supply and high density 28-pin package (SOJ)
- High speed: Fast access time 35/45 ns (max)
- Low power
  - Operation: 350 mW (typ)
  - Standby: 100 μW (typ)
- Completely static memory:
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

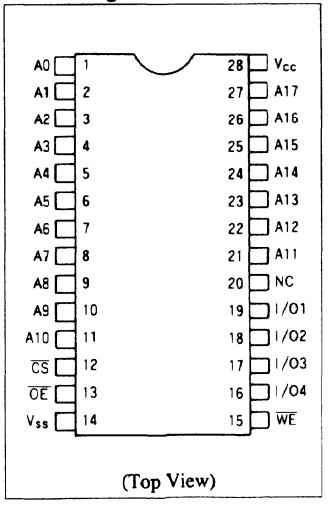
Ordering Information

Type No.	Access Time	Package
HM624256P-35	35 ns	400-mil 28-pin plastic DIP (DP-28C)
HM624256P-45	45 ns	
HM624256LP-35	35 ns	
HM624256LP-45	45 ns	
HM624256JP-35	35 ns	400-mil 28-pin plastic SOJ (CP-28D)
HM624256JP-45	45 ns	
HM624256LJP-35	35 ns	
HM624256LJP-45	45 ns	

Pin Description

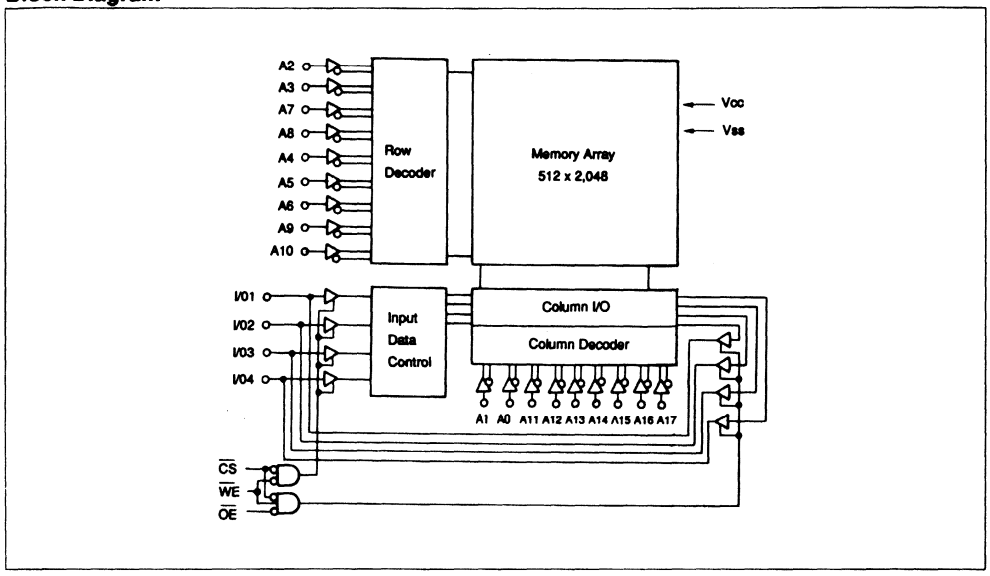
Pin Name	Function
A0 – A17	Address
I/O1 – I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Pin Arrangement



(Top View)

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	Icc	Dout	Read cycle (1) – (3)
L	H	L	Write	Icc	Din	Write cycle (1)
L	L	L	Write	Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +85	°C

Note: *1. V_T min. = –2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min. = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = Vss to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = Vss to V_{CC}
Operating power supply current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min cycle
Standby power supply current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ Vin ≤ 0.2 V or
	I_{SB1}*2	—	4*2	200*2	µA	Vin ≥ V_{CC} – 0.2V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.
*2. LP, LJP Version

Capacitance (Ta = 25°C, f = 1MHz)

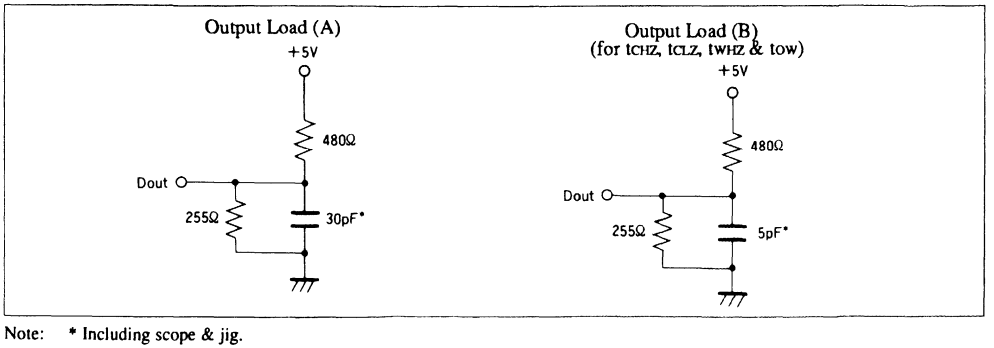
Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	11	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to+70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

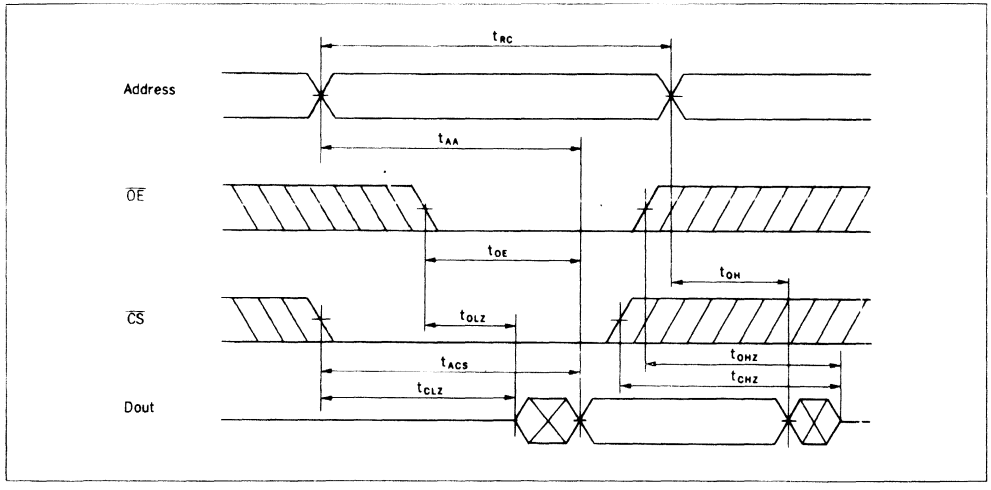


Note: * Including scope & jig.

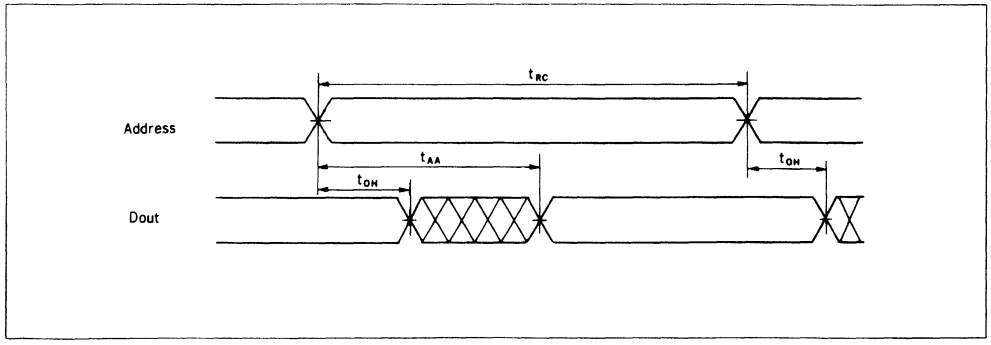
Read Cycle

Item	Symbol	HM624256-35		HM624256-45		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	35	—	45	—	ns
Address access time	t_{AA}	—	35	—	45	ns
Chip select access time	t_{ACS}	—	35	—	45	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	18	—	23	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	20	0	20	ns
Chip disable to output in high-Z	t_{OHZ}*1	0	10	0	15	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	30	—	30	ns

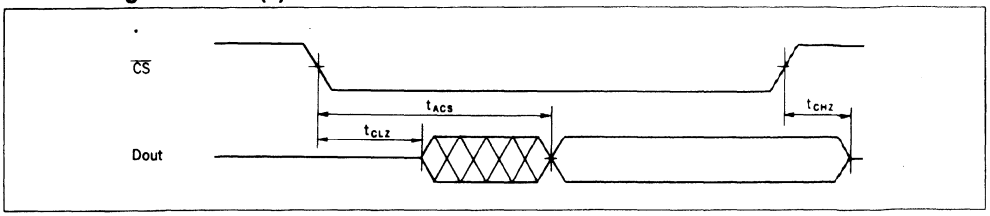
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *2, *3, *5



Read Timing Waveform (3) *1, *2, *4, *5

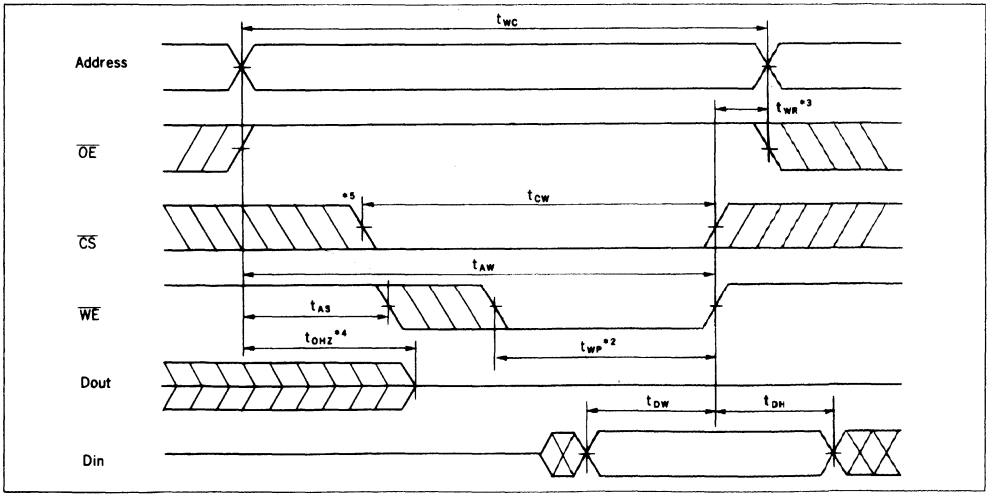


Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$=VIL.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. $\overline{OE}$=VIL.

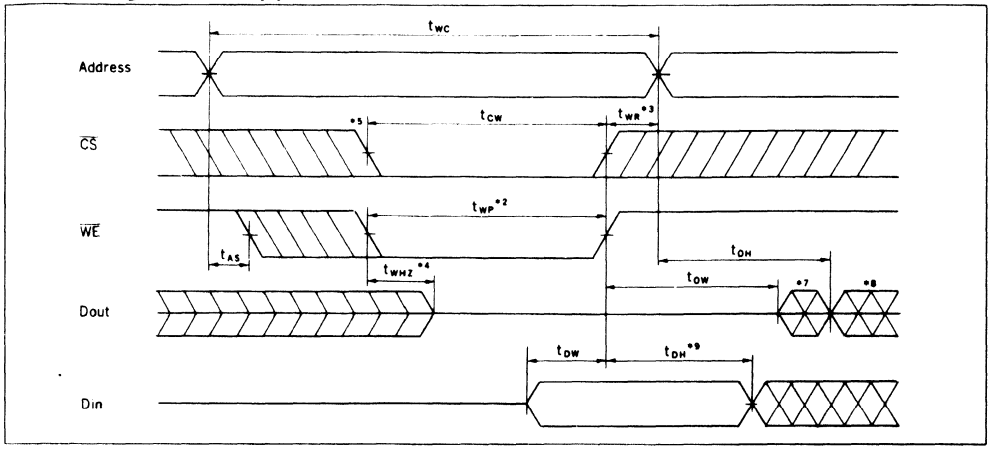
Write Cycle

Parameter	Symbol	HM624256-35		HM624256-45		Unit
		Min	Max	Min	Max	
Write cycle time	tWC	35	—	45	—	ns
Chip selection to end of write	tCW	30	—	40	—	ns
Address valid to end of write	tAW	30	—	40	—	ns
Address setup time	tAS	0	—	0	—	ns
Write pulse width	tWP	25	—	30	—	ns
Write recovery time	tWR	3	—	3	—	ns
Output disable to output in high-Z*1	tOHZ	0	10	0	15	ns
Write to output in high-Z*1	tWHZ	0	15	0	15	ns
Data to write time overlap	tDW	20	—	25	—	ns
Data hold from write time	tDH	0	—	0	—	ns
Output active from end of write*1	tOW	0	—	0	—	ns

Write Timing Waveform (1)



Write Timing Waveform (2) *6



Notes: *1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.
*2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
*3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
*5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
*6. $\overline{OE}$ is continuously low. ($\overline{OE}$=VIL)
*7. Dout is the same phase of write data of this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

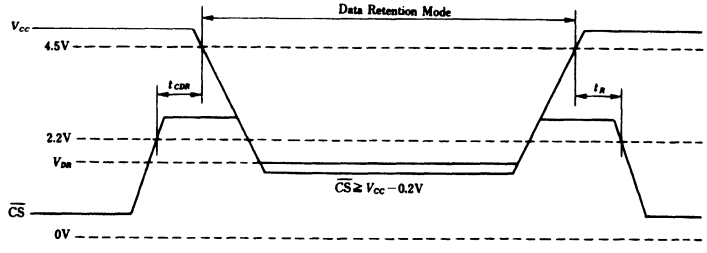
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

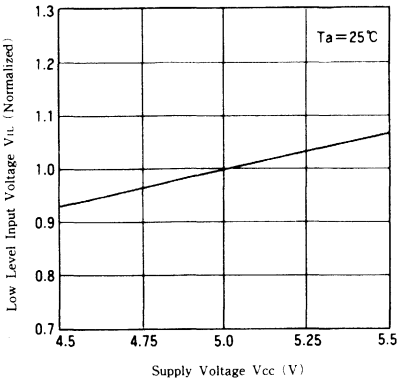
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	VDR	2	—	—	V	$\overline{CS}$ ≥ Vcc – 0.2 V,
Data retention current	ICCDR	—	2	100*1	µA	Vin ≥ Vcc – 0.2 V or
Chip deselect to data retention time	tCDR	0	—	—	ns	0 V ≤ Vin ≤ 0.2 V
Operation recovery time	tR	5	—	—	ms	

Note: *1. Vcc = 3.0 V.

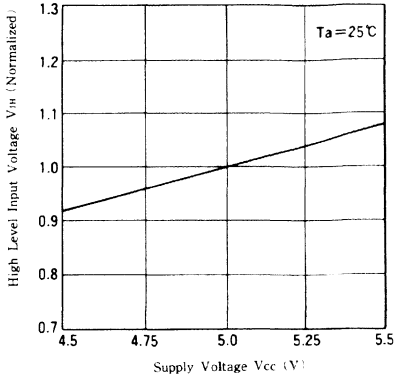
Low Vcc Data Retention Timing Waveform



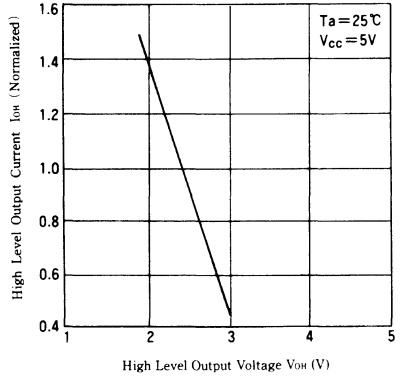
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



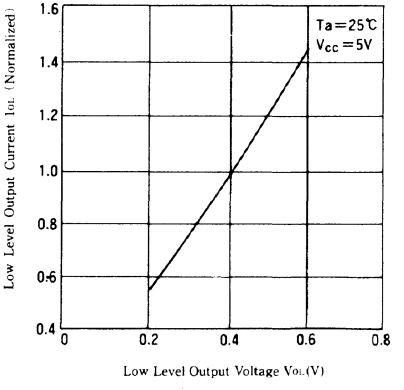
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



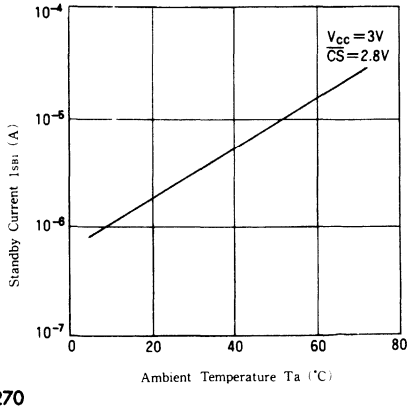
HIGH LEVEL OUTPUT CURRENT VS. HIGH LEVEL OUTPUT VOLTAGE



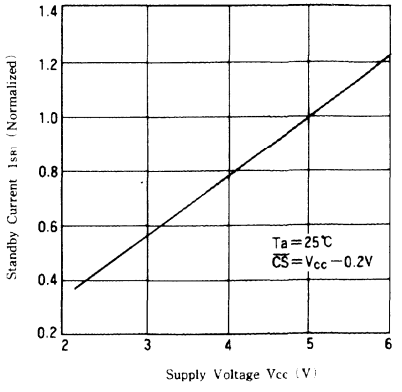
LOW LEVEL OUTPUT CURRENT VS. LOW LEVEL OUTPUT VOLTAGE



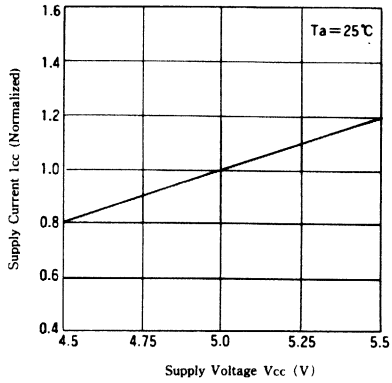
STANDBY CURRENT VS. AMBIENT TEMPERATURE



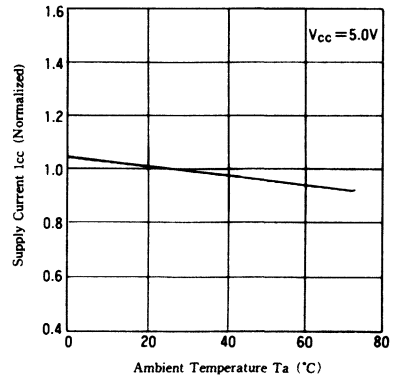
STANDBY CURRENT VS. SUPPLY VOLTAGE



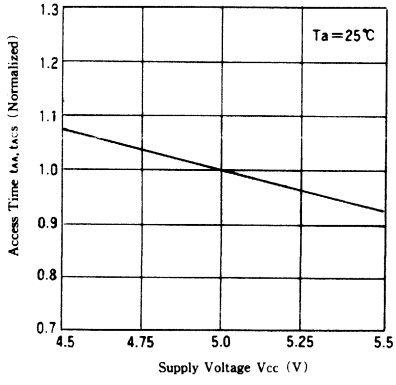
SUPPLY CURRENT VS. SUPPLY VOLTAGE



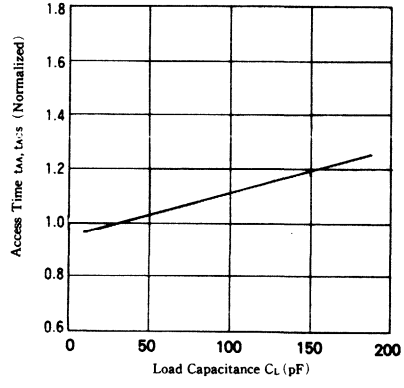
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



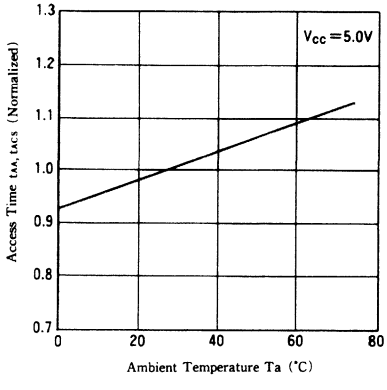
ACCESS TIME VS. SUPPLY VOLTAGE



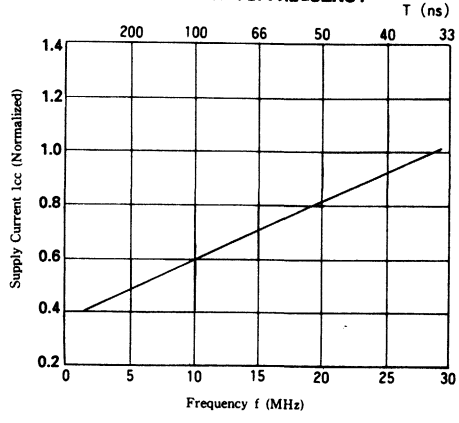
ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. AMBIENT TEMPERATURE



SUPPLY CURRENT VS. FREQUENCY



HM624257 Series

262144-Word × 4-Bit High Speed CMOS Static RAM

The Hitachi HM624257 is a high speed 1M Static RAM organized as 256-kword x 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624257, packaged in a 400-mil plastic SOJ is available for high density mounting.

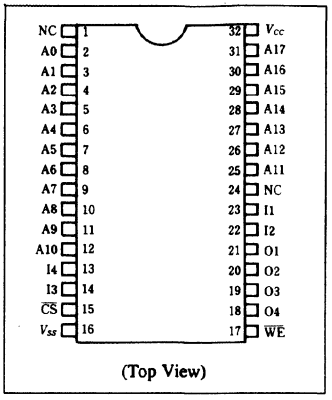
Features

- Single 5 V supply and high density 32 pin package (SOJ)
- High speed
  - Access time: 35 ns/45 ns (max)
- Low power dissipation
  - Active mode: 350 mW (typ)
  - Standby mode: 100 µW (typ)
- Completely static memory required
  - No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM624257JP-35	35 ns	400-mil
HM624257JP-45	45 ns	32-pin
HM624257LJP-35	35 ns	plastic SOJ
HM624257LJP-45	45 ns	(CP-32D)

Pin Arrangement

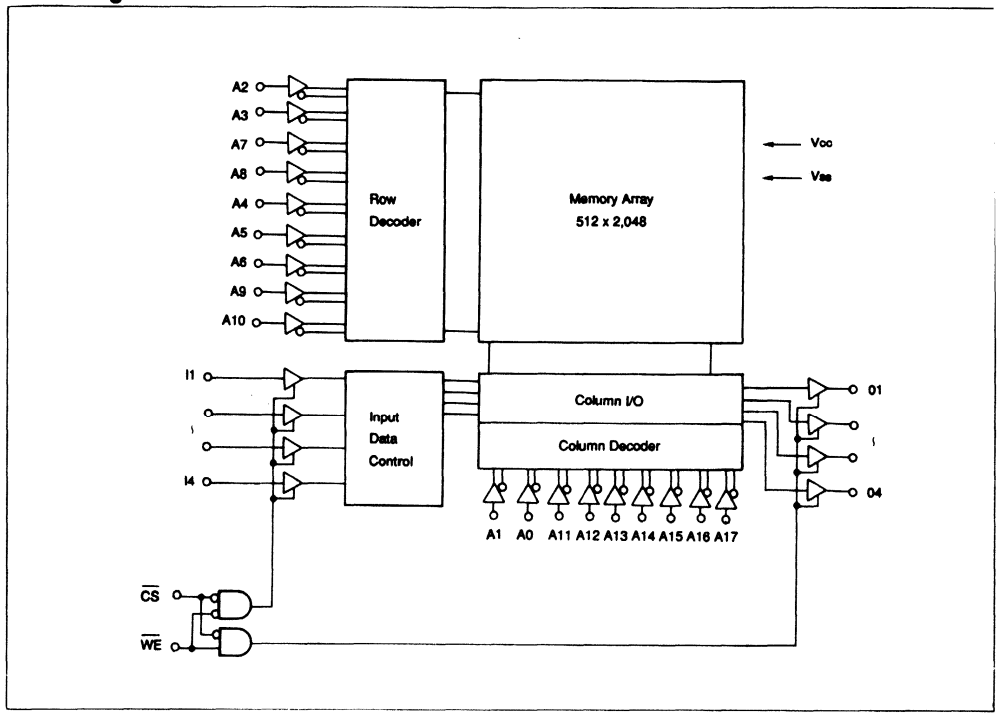


(Top View)

Pin Description

Pin Name	Function
A0 – A17	Address
I1 – I4	Data input
O1 – O4	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.0V for pulse width ≤ 10 ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle (1)–(2)
L	L	Write	Icc	High-Z	Write cycle (1)–(2)

Note: ×; H or L

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = Max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} Vout = V_{SS} to V_{CC}
Operating power supply current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, Iout = 0 mA, min cycle
Standby power supply current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby power supply current (1)	I_{SB1}*2	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} –0.2 V
	I_{SB1}*3	—	4*3	200*3	µA	0 V ≤ Vin ≤ 0.2 V or Vin ≥ V_{CC} –0.2 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at V_{CC} = 5.0 V, Ta = 25°C and specified loading.
*2. JP-version
*3. LJP-version

Capacitance (Ta = 25°C, f = 1MHz)

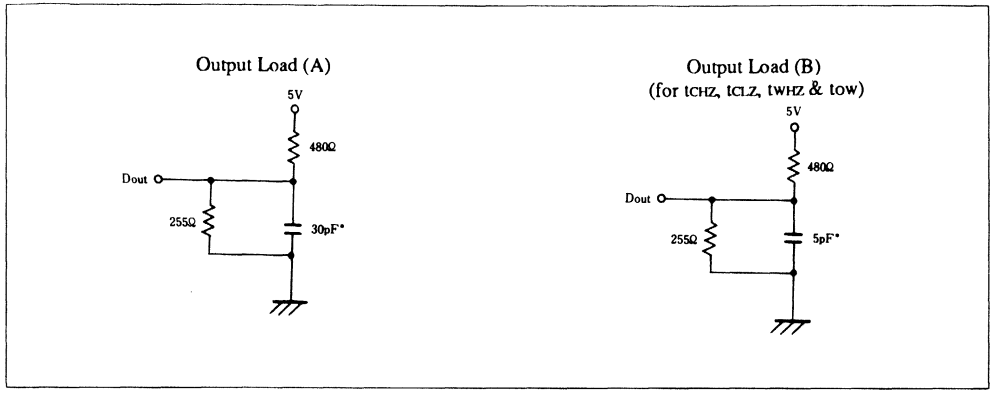
Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	11	pF	Vout = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures



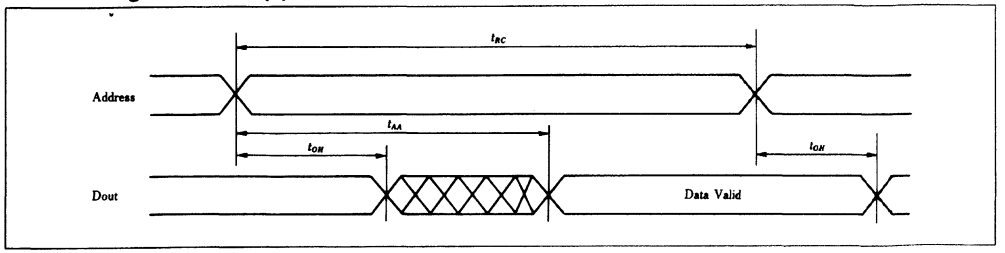
Note: * Including scope & Jig.

Read Cycle

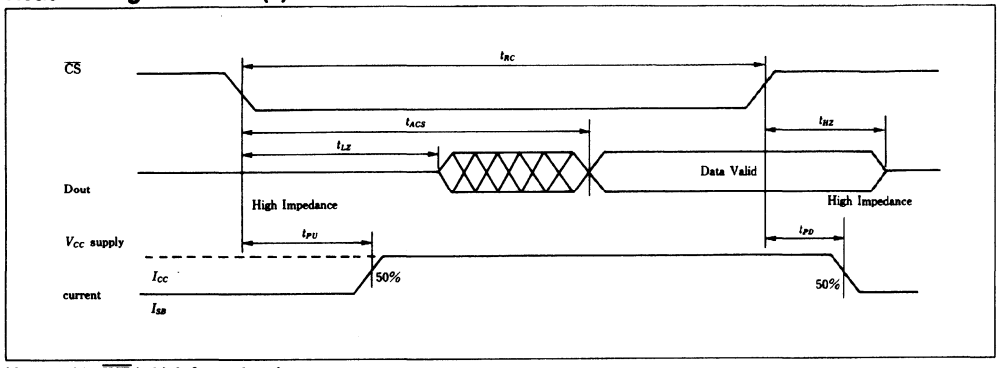
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	35	—	45	—	ns
Address access time	t_{AA}	—	35	—	45	ns
Chip select access time	t_{ACS}	—	35	—	45	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip selection to output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in High-Z	t_{HZ}*1	0	20	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	30	—	30	ns

Note: *1. Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1 *2



Read Timing Waveform (2) *1 *3



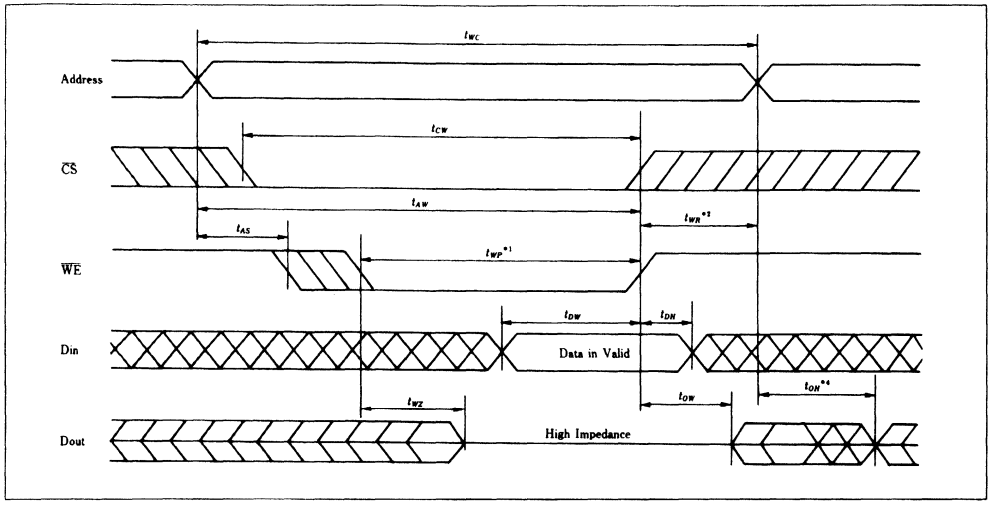
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

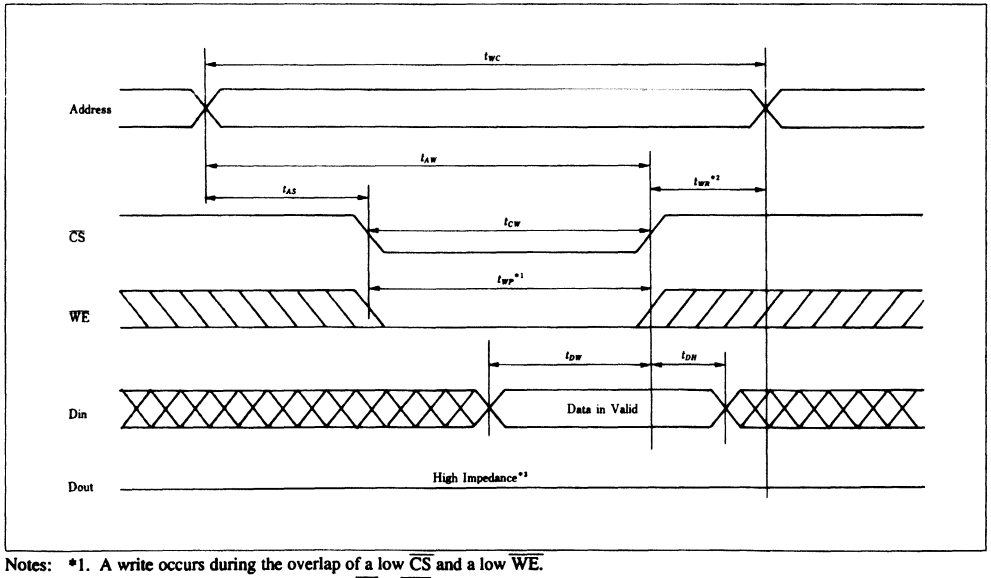
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	35	—	45	—	ns
Chip selection to end of write	t_{CW}	30	—	40	—	ns
Address valid to end of write	t_{AW}	30	—	40	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	25	—	30	—	ns
Write recovery time	t_{WR}	3	—	3	—	ns
Data valid to end of write	t_{DW}	20	—	25	—	ns
Data hold time	t_{DH}	3	—	3	—	ns
Write enabled to output in High-Z	t_{WZ}*1	0	15	0	20	ns
Output active from end of write	t_{OW}*1	5	—	5	—	ns

Note: *1. Transistion is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. If the $\overline{CS}$ low Transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

*4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

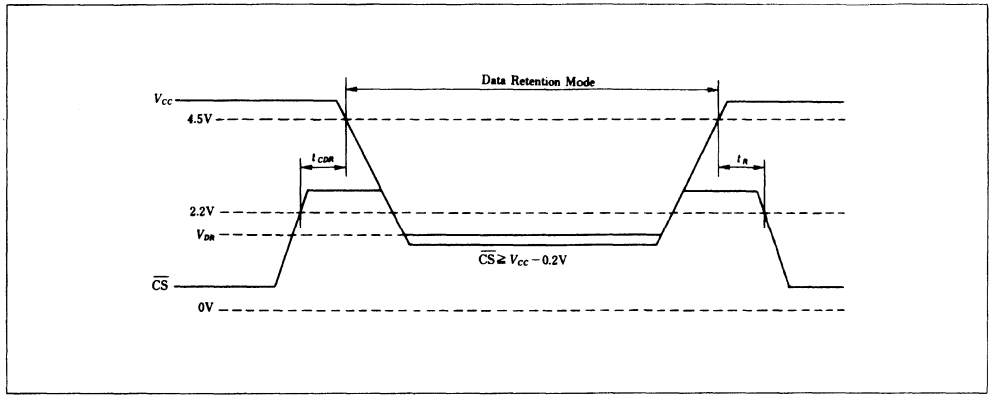
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

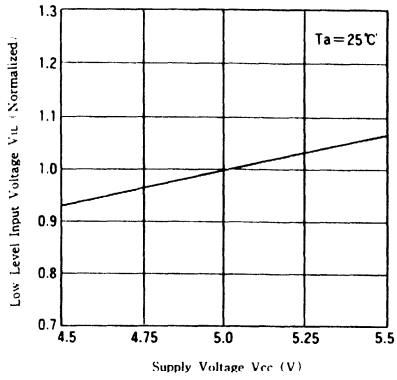
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V,
Data retention current	I_{CCDR}	—	2	100*1	µA	Vin ≥ Vcc – 0.2 V or
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	0 V ≤ Vin ≤ 0.2 V
Operation recovery time	t_R	5	—	—	ms	

Note: *1. Vcc = 3.0V.

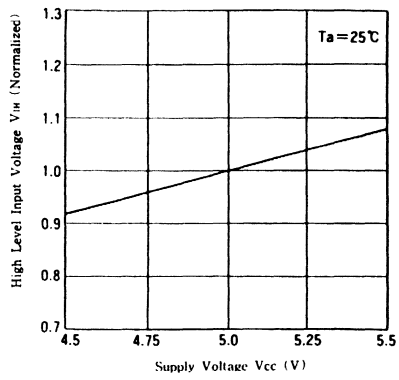
Low Vcc Data Retention Timing Waveform



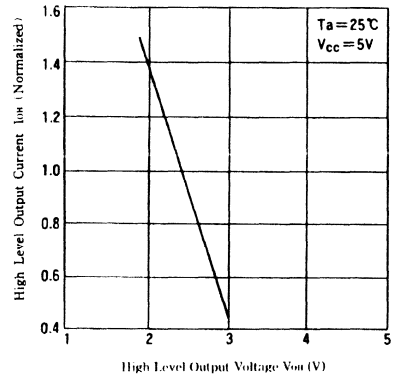
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



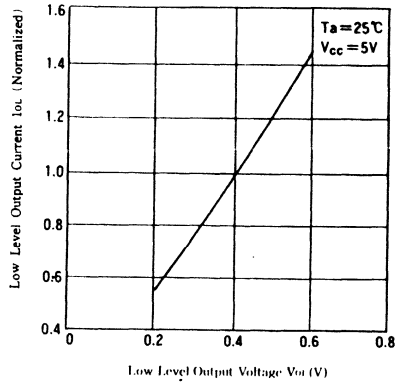
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



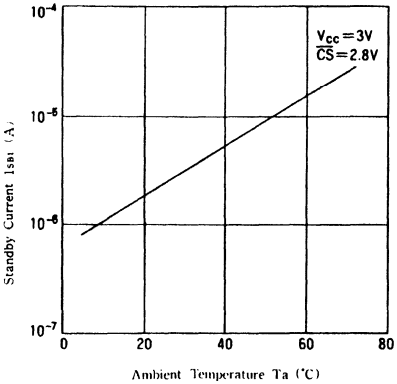
HIGH LEVEL OUTPUT CURRENT VS. HIGH LEVEL OUTPUT VOLTAGE



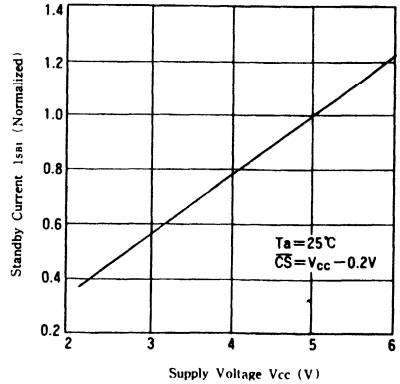
LOW LEVEL OUTPUT CURRENT VS. LOW LEVEL OUTPUT VOLTAGE



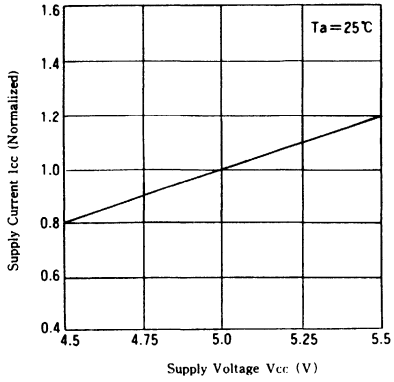
STANDBY CURRENT VS. AMBIENT TEMPERATURE



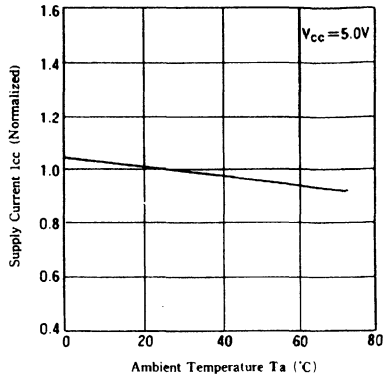
STANDBY CURRENT VS. SUPPLY VOLTAGE



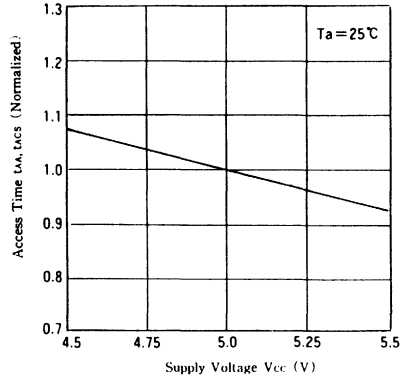
SUPPLY CURRENT VS. SUPPLY VOLTAGE



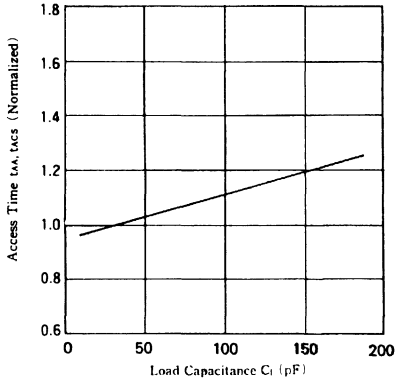
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



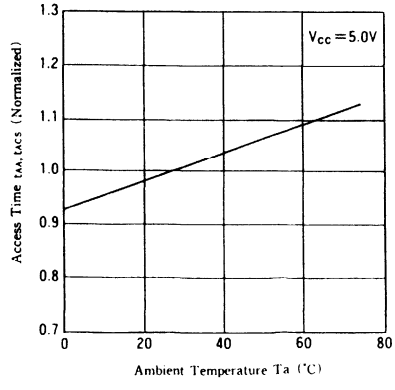
ACCESS TIME VS. SUPPLY VOLTAGE



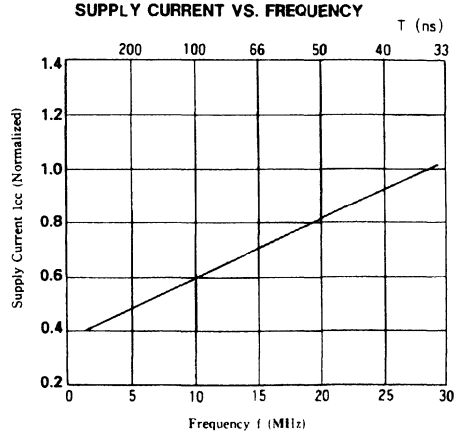
ACCESS TIME VS. LOAD CAPACITANCE



ACCESS TIME VS. AMBIENT TEMPERATURE

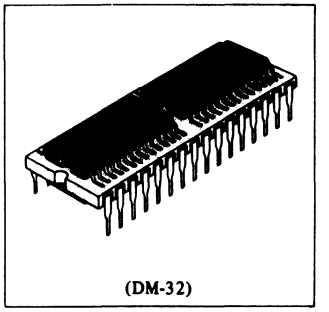


SUPPLY CURRENT VS. FREQUENCY



HM66203 Series

131072-word x 8-bit High Density CMOS Static RAM Module



(DM-32)

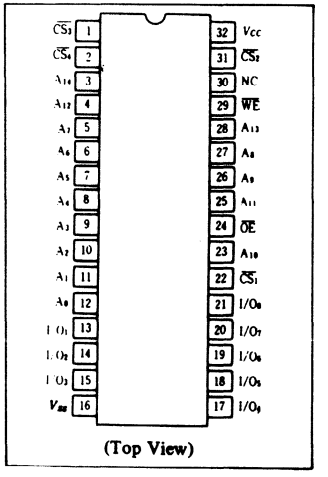
Features

- High Density Industry Standard 32 Pin DIP Mounting 4pcs of 256k Static RAM (SOP; HM62256FP/LFP).
- Single +5V Supply.
- High speed: Fast Access Time 100/120/150ns max.
- Equal Access and Cycle Time.
- Completely Static RAM: No Clock or Timing Strobe Required.
- Low Power
  - Standby: 40μW typ. (L-version)
  - Operation: 50mW typ. (f = 1MHz)
- Capability of Battery Back-up Operation (L-version).
- Common Data Input and Output, Three State Outputs.
- Directly TTL Compatible: All Inputs and Outputs.

Ordering Information

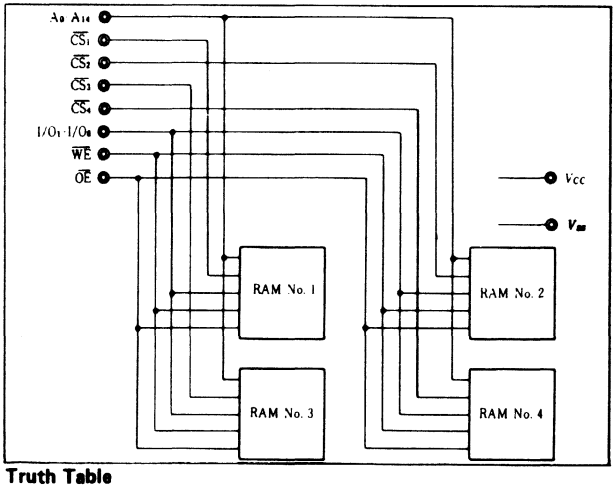
Type No.	Access Time	Package
HM66203-10	100ns	600 mil 32 pin DIP
HM66203-12	120ns	
HM66203-15	150ns	
HM66203L-10	100ns	
HM66203L-12	120ns	
HM66203L-15	150ns	

Pin Arrangement



(Top View)

Functional Block Diagram



Pin Description

Pin Name	Function
A0–A14	Address
I/O1–I/O8	Input/output
$\overline{CS1}$–$\overline{CS4}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Truth Table

Mode	$\overline{CSi}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not Selected (Power Down)	H*1	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L*2	H	L	D_{out}	I_{CC}	Read Cycle (1) to (3)
Write	L*2	L	H	D_{in}	I_{CC}	Write Cycle (1)
	L*2	L	L	Din	I_{CC}	Write Cycle (2)

Note) *1. X: Don't Care (H or L); i = 1, 2, 3, 4 All chips are not selected.
*2. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding.
Only one chip should be selected.
Two or more chips must not be selected at one time.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.0V for pulse width ≦ 50ns

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	min.	typ. *1	max.	Unit	Notes
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	8	μA	
		V_{IN} = V_{SS} to 3.5V	–	–	2	μA	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS_n}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–	–	8	μA	*2
		$\overline{CS_n}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to 3.5V	–	–	2		
Operating Power Supply Current: DC	I_{CC}	$\overline{CSN}$ = V_{IL}, $I_{I/O}$ = 0mA	–	10	25	mA	*3
Average Operating Power Supply Current (1)	I_{CC1}	MIN. cycle	–	42	80	mA	HM66203/L −10
		duty = 100%	–	37	80		HM66203/L −12
		$I_{I/O}$ = 0mA	–	35	80		HM66203/L −15
Average Operating Power Supply Current (2)	I_{CC2}	$\overline{CSN}$ = V_{IL}, V_{IH} = V_{CC}, V_{IL} = 0V, $I_{I/O}$ = 0mA, f = 1MHz	–	10	15	mA	*3
Standby Power Supply Current: DC	I_{SB}	$\overline{CSn}$ = V_{IH}	–	2	12	mA	*2
Standby Power Supply Current (1): DC	I_{SB1}	$\overline{CS_n}$ ≧ V_{CC} − 0.2V, 0V ≦ V_{IN}	–	8	400	μA	HM66203L Series
			–	0.16	8	mA	HM66203 Series
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V	
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4	–	–	V	

Note) *1. Typical values are at V_{CC} = 5.0V, T_a = +25°C and specified loading.
*2. $\overline{CSn}$; All chips are not selected.
*3. $\overline{CSN}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.

Capacitance (T_a = 25°C, f = 1.0MHz)

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	45	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	–	50	pF

Note) This parameter is sampled and not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

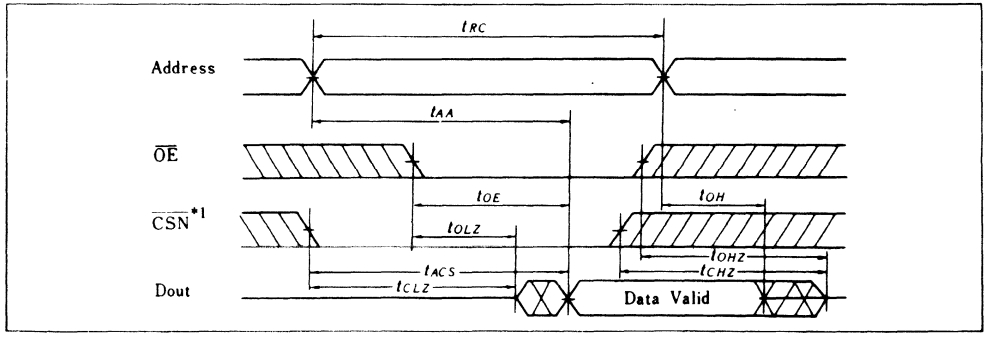
AC Test Conditions

- Input pulse levels . . . . . 0.8V to 2.4V
- Input rise and fall times 5ns
- Input and Output timing reference level 1.5V
- Output load . . . . . 1 TTL Gate and C_L (100pF) (Including scope & jig)

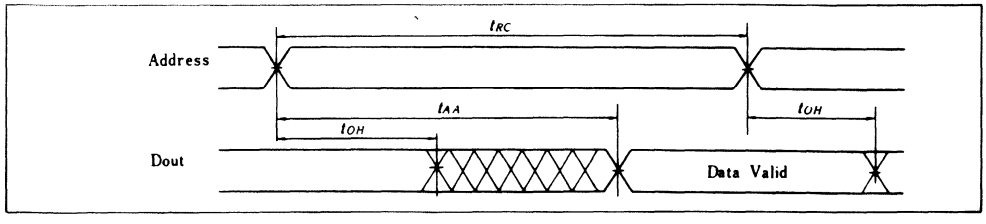
Read Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns

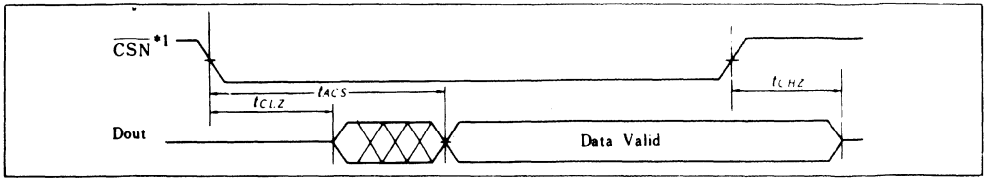
Timing Waveform of Read Cycle No. 1 *2



Timing Waveform of Read Cycle No. 2 *1,*2,*3,*5



Timing Waveform of Read Cycle No. 3 *2,*4,*5

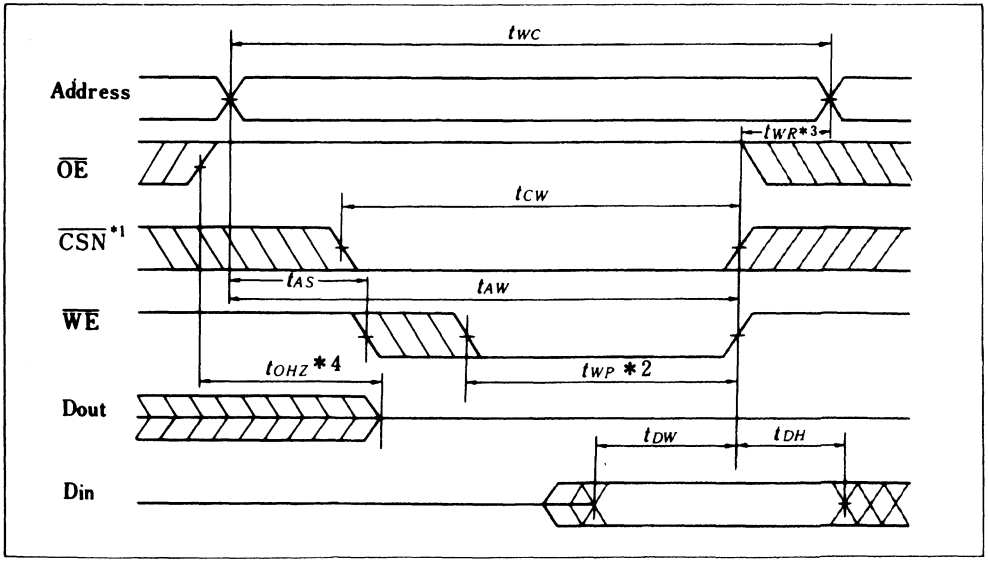


Note) *1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CSN} = V_{IL}$.
*4. Address should be valid prior to or coincident with $\overline{CSN}$ transition low.
*5. $\overline{OE} = V_{IL}$

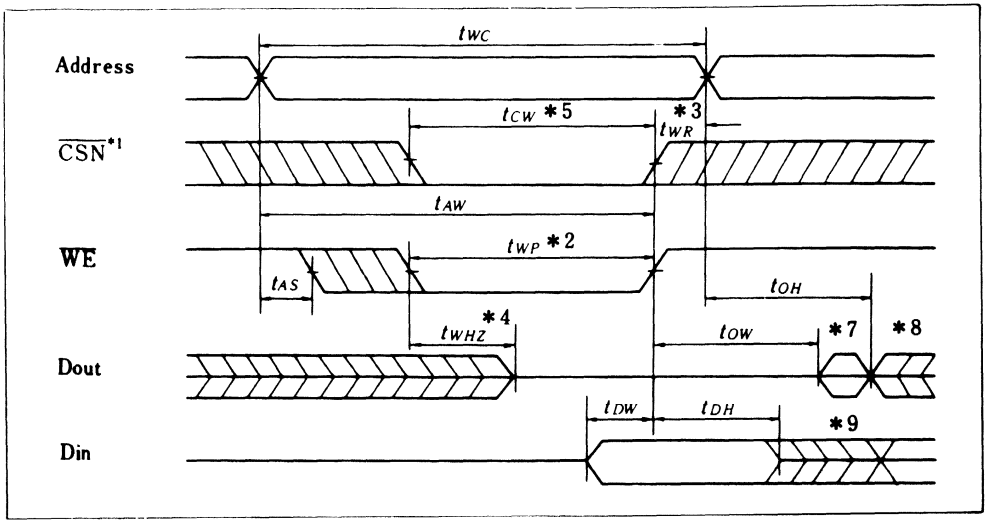
Write Cycle

Parameter	Symbol	HM66203-10		HM66203-12		HM66203-15		Unit
		min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	90	–	100	–	120	–	ns
Address Valid to End of Write	t_{AW}	90	–	100	–	120	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	75	–	90	–	110	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

Timing Waveform of Write Cycle (1) ($\overline{OE}$ Clock)



Timing Waveform of Write Cycle (2) ($\overline{OE}$ Low Fixed)*6



Notes)
*1. $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{CS4}$ pins are used for chip decoding. Only one chip should be selected. Two or more chips must not be selected at one time.
*2. A write occurs during the overlap (t_{WP}) of a low $\overline{CSN}$ and a low $\overline{WE}$.
*3. t_{WR} is measured from the earlier of $\overline{CSN}$ or $\overline{WE}$ going high to the end or write cycle.
*4. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
*5. If the $\overline{CSN}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, output remain in a high impedance state.
*6. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*7. Dout should be held in phase of the written data during this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CSN}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

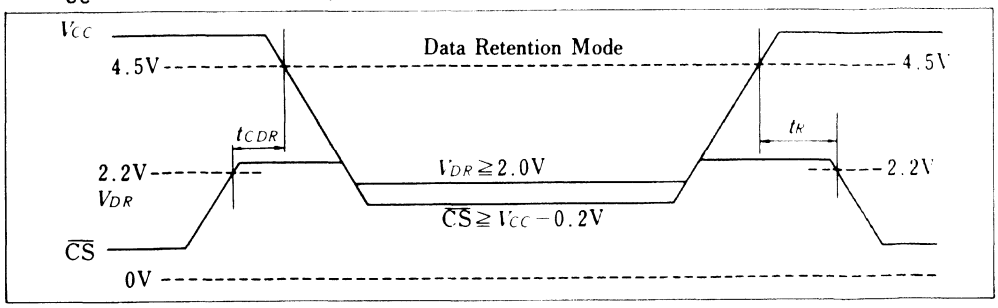
Low V_{CC} Data Retention Characteristics (T_a = 0°C to +70°C)

(Data retention characteristics is guaranteed only for HM66203L Series.)

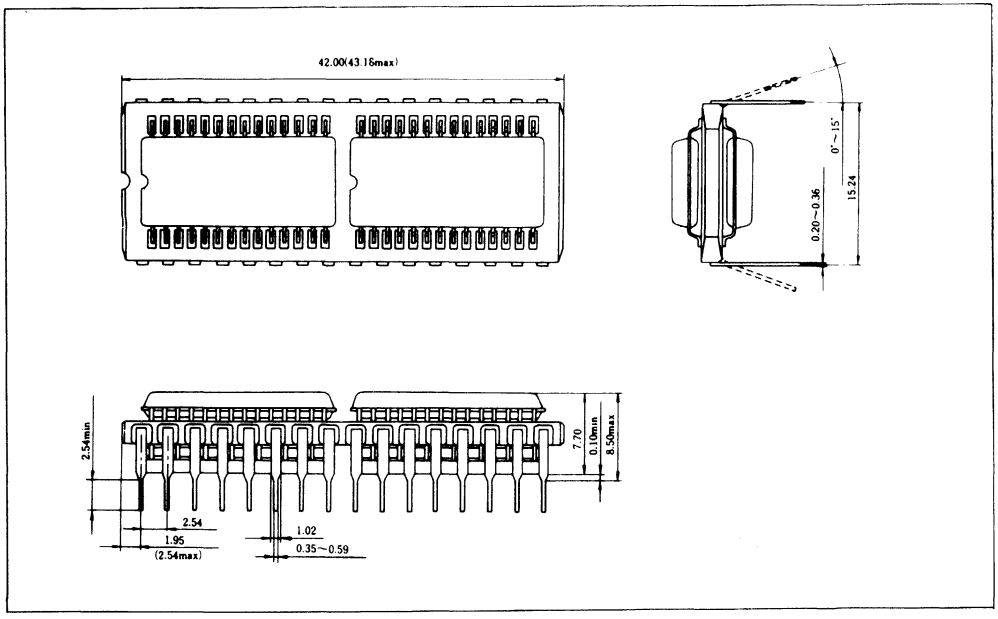
Parameter	Symbol	min.	typ.	max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CSn} \geqq V_{CC} - 0.2V$
Data Retention Current	I_{CCDR}	–	–	200	μA	V_{CC} = 3.0V $\overline{CSn} \geqq 2.8V$*2, $0V \leqq V_{IN}$
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See Retention Waveform
Operation Recovery Time	t_R	[1] t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.
*2. $\overline{CSn}$: All chips are not selected.

Low V_{CC} Data Retention Waveform



Package Outline (Unit: mm)



HM66204 Series

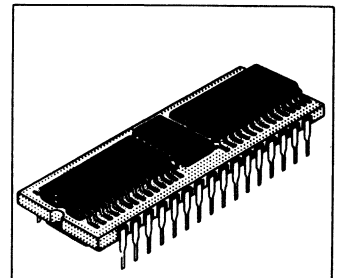
131072-word x 8-bit High Density CMOS Static RAM Module

The HM66204 is a high density 1 M-bit static RAM module consisted of 4 pieces of HM62256FP/LFP products (SOP type 256k static RAM) and a HD74HC138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66204 is the standard 600 mil width 32 pin dual-in-line package. Its pin arrangement is completely compatible with 1 M-bit monolithic static RAM.

The HM66204 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66204 makes high density mounting possible with no surface mount technology.

These features make the HM66204 ideally suited for high density compacted memory systems.



(DM-32A)

Features

- High density 32 pin DIP
  - Mounting 4 pcs. of 256k static RAM (SOP; HM62256FP/LFP) and CMOS decoder logic (SOP; HD74HC138FP equivalent)
- Pin compatible with 1M monolithic static RAM
- High speed
  - Fast access time 120 ns/150 ns (maximum)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby 40 μW (typical) (L-version)
  - Operation 50 mW(typical) (f = 1 MHz)
- Common data input and output, three state outputs
- Capable of battery backup operation (L-version)

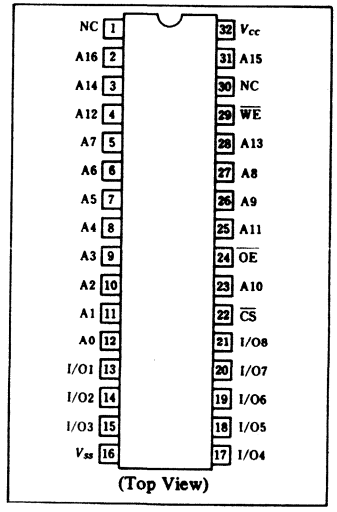
Ordering Information

Part No.	Access Time	Package
HM66204-12	120 ns	600-mil 32-pin DIP
HM66204-15	150 ns	
HM66204L-12	120 ns	
HM66204L-15	150 ns	

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C
Power dissipation	P_T	1.0	W

Pin Arrangement

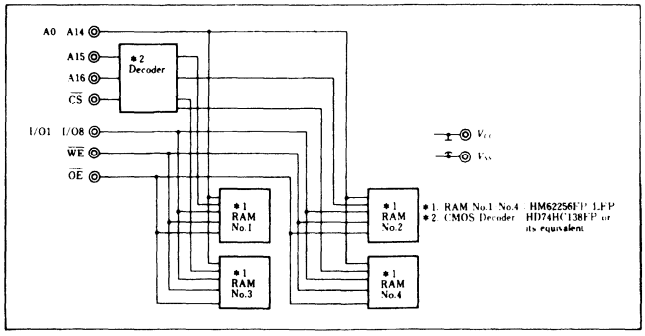


(Top View)

Pin Description

Pin Name	Function
A0 - A16	Address
I/O1 - I/O8	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Mode Selection

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not selected (Power down)	H	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note) X = Don't care (H or L)

Electrical Characteristics

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) Voltage	V_{IH}	3.85*1	–	6.0	V	A15, A16, $\overline{CS}$
		2.2	–	6.0	V	Others except A15, A16, $\overline{CS}$
Input low (logic 0) Voltage	V_{IL}	–0.5	–	0.8	V	

Note) *1. V_{IH} min is determined by V_{CC} x 0.7.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions	Notes
Input leakage current	$\|I_{LI}\|$	–	–	8	μA	V_{in} = V_{SS} to V_{CC}	
		–	–	2	μA	V_{in} = V_{SS} to 3.5V	
Output leakage current	$\|I_{LO}\|$	–	–	8	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	
		–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to 3.5V	
Operating power supply current: DC	I_{CC}	–	10	25	mA	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0mA	
Average operating power supply current (1)	I_{CC1}	–	37	80	mA	MIN. cycle duty = 100%	–12
		–	35	80		$I_{I/O}$ = 0mA	–15
Average operating power supply current (2)	I_{CC2}	–	10	15	mA	$\overline{CS}$ = V_{IL}, V_{IH} = V_{CC} V_{IL} = 0V, $I_{I/O}$ = 0mA f = 1MHz	
Standby power supply current: DC	I_{SB}	–	2	12	mA	$\overline{CS}$ = V_{IH}	
Standby power supply current (1): DC	I_{SB1}	–	8	400	μA	$\overline{CS}$ ≥ V_{CC}–0.2V A15·A16 ≥ V_{CC} – 0.2V	HM66204L Series
		–	0.16	8	mA	or 0V ≦ A15·A16 ≦ 0.2V	
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 2.1 mA	
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = –1.0 mA	

Note) *1. Typical values are at V_{CC} = 5.0V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	–	45	pF	Vin = 0V
Input/output capacitance	$C_{I/O}$	–	–	50	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

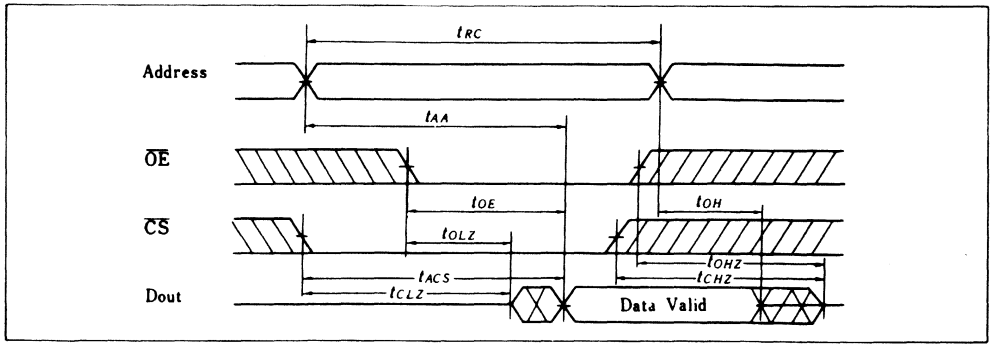
AC Test Conditions

- Input pulse levels:
  0.8V to 4.0V... $\overline{CS}$, A15, A16
  0.8V to 2.4V... Other pin except $\overline{CS}$, A15, A16
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5V
- Output load: 1 TTL Gate and C_L (100pF) (Including scope & jig)

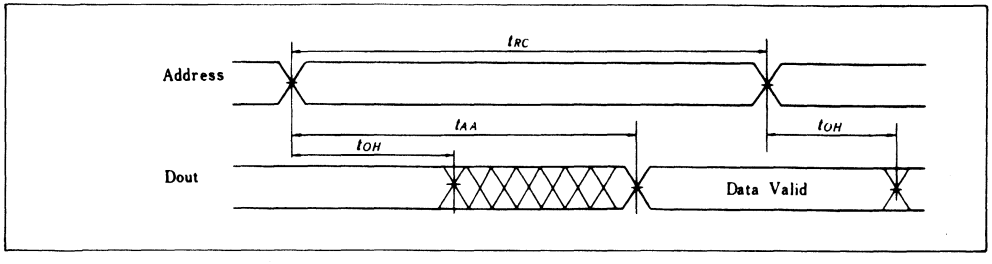
Read Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Read cycle time	t_{RC}	120	–	150	–	ns
Address access time	t_{AA}	–	120	–	150	ns
Chip select access time	t_{ACS}	–	120	–	150	ns
Output enable to output valid	t_{OE}	–	60	–	70	ns
Output hold from address change	t_{OH}	10	–	10	–	ns
Chip selection to output in low Z	t_{CLZ}	10	–	10	–	ns
Output enable to output in low Z	t_{OLZ}	5	–	5	–	ns
Chip deselection to output in high Z	t_{CHZ}	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns

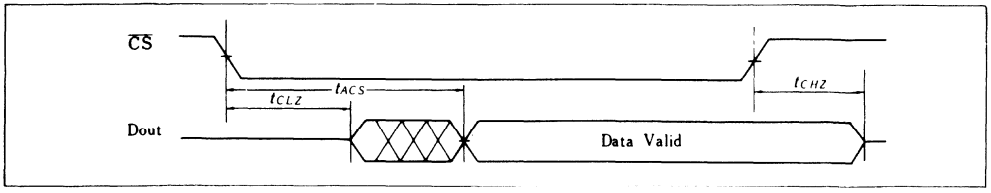
Read Cycle Timing No. 1 *1



Read Cycle Timing No. 2 *1,*2,*4



Read Cycle Timing No. 3 *1, *3, *4

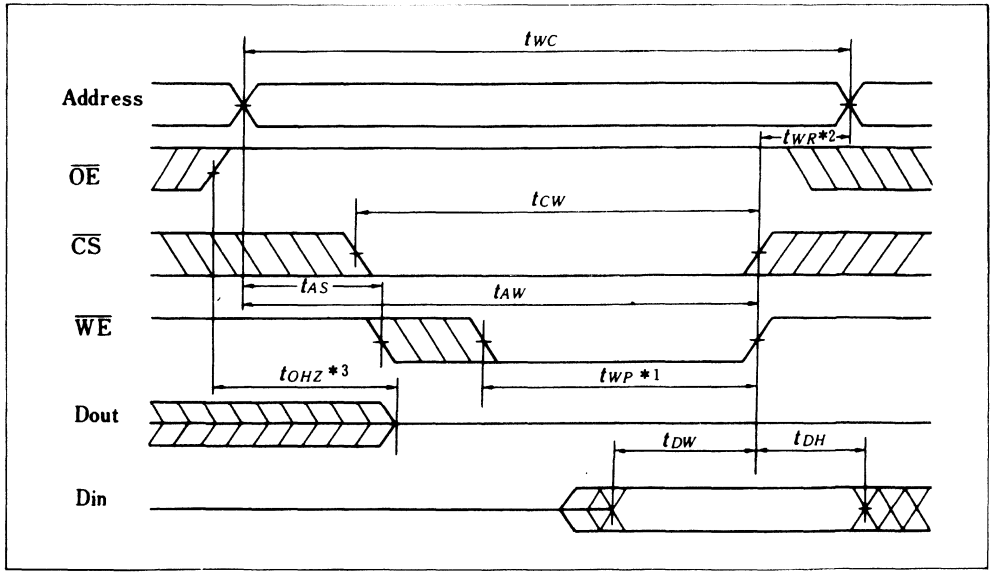


Notes) *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

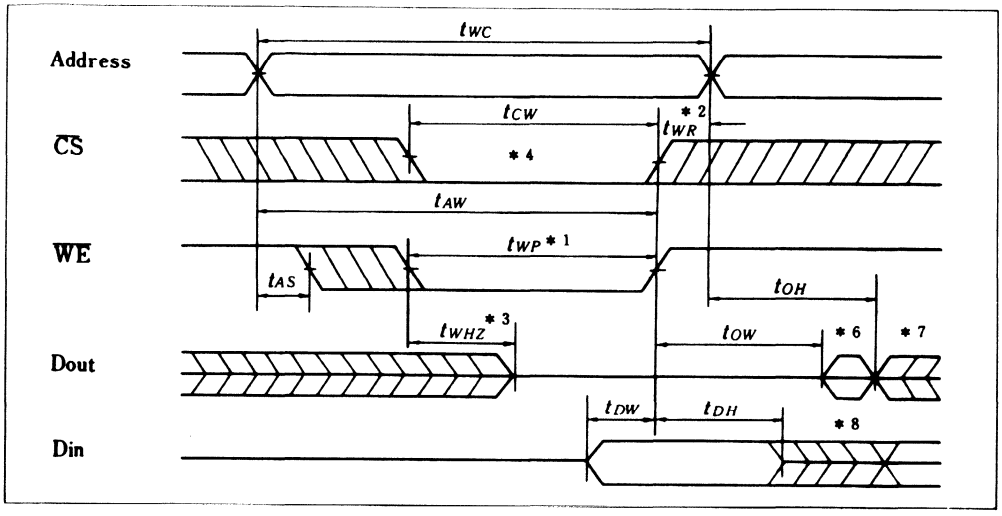
Write Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Write cycle time	t_{WC}	120	–	150	–	ns
Chip selection to end of write	t_{CW}	100	–	120	–	ns
Address valid to end of write	t_{AW}	100	–	120	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	90	–	110	–	ns
Write recovery time	t_{WR}	5	–	5	–	ns
Write to output in high Z	t_{WHZ}	0	40	0	50	ns
Data to write time overlap	t_{DW}	50	–	60	–	ns
Data hold from write time	t_{DH}	0	–	0	–	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns
Output active from end of write	t_{OW}	5	–	5	–	ns

Write Cycle Timing No. 1 ($\overline{OE}$ Clock)



Write Cycle Timing No. 2*5 ($\overline{OE}$ Low Fixed)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state.
The input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
*6. D_{out} should be held in phase of the written data during this write cycle.
*7. D_{out} is the read data of next address.
*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

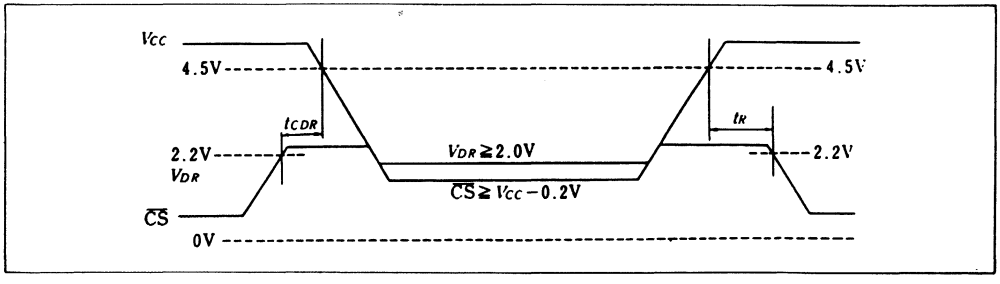
Low V_{CC} Data Retention Characteristics (Ta = 0°C to +70°C)

Data retention characteristics is guaranteed only for L version.

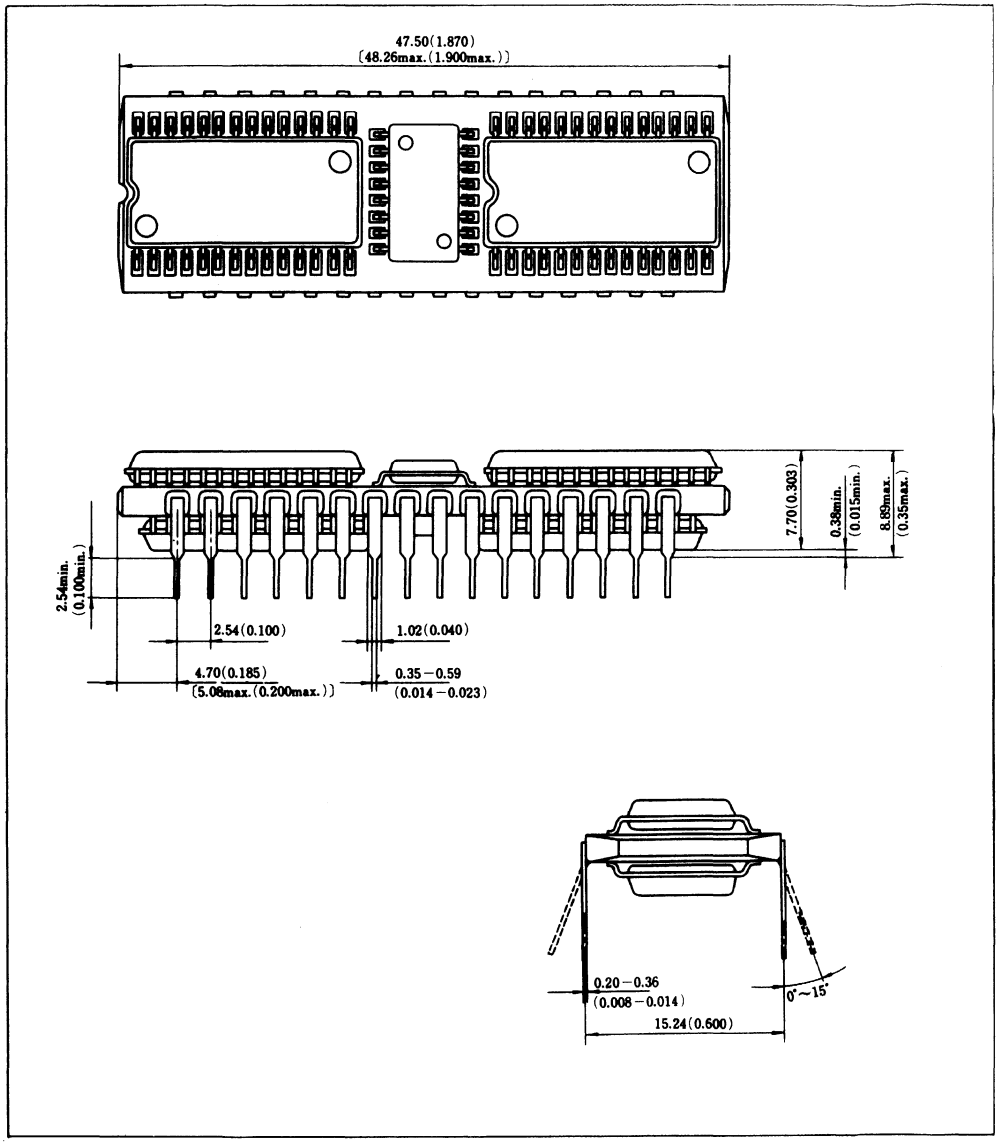
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC}-0.2V$ A15, A16 $\geq V_{CC}-0.2V$ or A15, A16 $\leq 0.2V$
Data retention current	I_{CCDR}	–	–	200	μA	V_{CC} = 3.0V, $\overline{CS} \geq 2.8V$ A15·A16 $\geq 2.8V$ or $0V \leqq$ A15·A16 $\leqq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Package Dimensions; Unit: mm (inch)



MOS
PSEUDO
STATIC
RAM

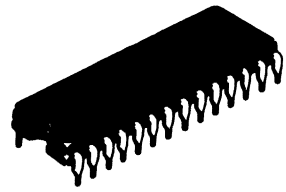
HM65256B Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

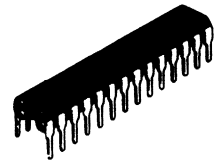
- Single 5V (±10%)
- High Speed
  - Access Time
  - $\overline{CE}$ Access Time 100/120/150/200ns
  - Address Access Time 50/60/75/100ns
  - (in Static Column Mode)
  - Cycle Time
  - Random Read/Write Cycle Time 160/190/235/310ns
  - Static Column Mode Cycle Time 55/65/80/105ns
- Low Power
  - 175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  - Address Refresh
  - Automatic Refresh
  - Self Refresh

HM65256BP Series



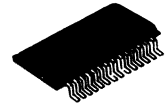
(DP-28)

HM65256BSP Series



(DP-28N)

HM65256BFP Series

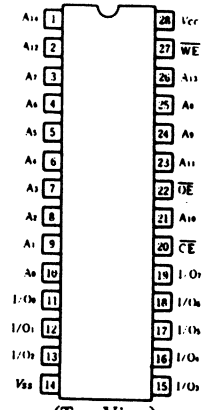


(FP-28DA)

■ ORDERING INFORMATION

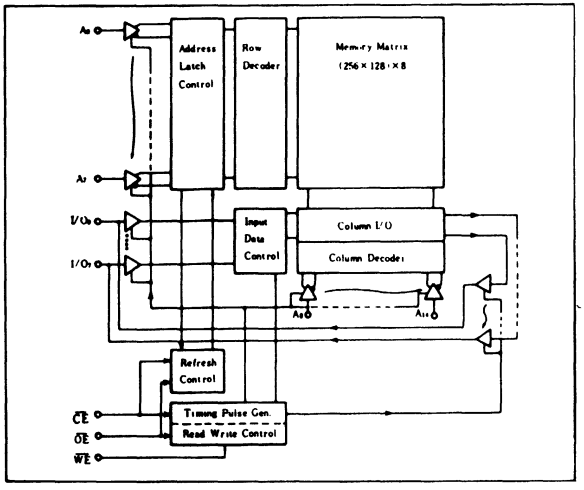
Type No.	Access Time	Package
HM65256BP-10	100ns	600 mil 28 pin Plastic DIP
HM65256BP-12	120ns	
HM65256BP-15	150ns	
HM65256BP-20	200ns	
HM65256BLP-10	100ns	
HM65256BLP-12	120ns	
HM65256BLP-15	150ns	
HM65256BLP-20	200ns	
HM65256BSP-10	100ns	300 mil 28 pin Plastic DIP
HM65256BSP-12	120ns	
HM65256BSP-15	150ns	
HM65256BSP-20	200ns	
HM65256BLSP-10	100ns	
HM65256BLSP-12	120ns	
HM65256BLSP-15	150ns	
HM65256BLSP-20	200ns	
HM65256BFP-10T	100ns	28 pin Plastic SOP
HM65256BFP-12T	120ns	
HM65256BFP-15T	150ns	
HM65256BFP-20T	200ns	
HM65256BLFP-10T	100ns	
HM65256BLFP-12T	120ns	
HM65256BLFP-15T	150ns	
HM65256BLFP-20T	200ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	mode
L	L	H	Low Z	Read
L	x	L	High Z	Write
L	H	H	High Z	–
H	L	x	High Z	Refresh
H	H	x	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width $\leqq$ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Conditions	HM65256B Series			HM65256BL Series			Unit
			min.	typ.	max.	min.	typ.	max.	
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0mA, t_{cyc} = min.	–	35	65	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}	–	1	2	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \geq V_{CC}-0.2V$	–	–	–	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}	–	1	2	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \leq 0.2V$	–	–	–	–	50	100	µA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, Vin = V_{SS} to V_{CC}	–10	–	10	–10	–	10	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	–10	–	10	µA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = –1 mA	2.4	–	–	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	Cin	Vin = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level . . . . . V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load . . . . . 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	235	–	310	–	ns
Static Column Mode Read or Write Cycle	t_{RSC}	55	–	65	–	80	–	105	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	–	200	ns
Address Access Time	t_{AA}	–	50	–	60	–	75	–	100	ns
Output Enable Access Time	t_{OEA}	–	40	–	50	–	60	–	75	ns
Chip Disable to Output in High Z	t_{CHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	30	–	35	–	40	–	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable Pulse Width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	50	–	60	–	75	–	100	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	20	–	20	–	25	–	30	–	ns
Column Address Hold Time	t_{CAH}	100	–	120	–	150	–	200	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns
Output Enable Hold Time	t_{OHC}	0	–	0	–	0	–	0	–	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	–	0	–	0	–	0	–	ns
Output Hold Time from Column Address	t_{OH}	5	–	5	–	5	–	10	–	ns
Write Command Pulse Width	t_{WP}	25	–	25	–	30	–	35	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	200	–	ns
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	0	–	ns

(to be continued)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Column Address Hold Time after Write	t_{AHW}	0	–	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	20	–	25	–	30	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	50	–	60	–	75	–	100	–	ns
Refresh Precharge Time	t_{FP}	30	–	30	–	30	–	30	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	160	–	190	–	235	–	310	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	–	10000	–	10000	–	10000	–	ns
Refresh Reset Time for Self Refresh	t_{FRS}	160	–	190	–	235	–	310	–	ns
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.

(2) t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T=5ns, and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

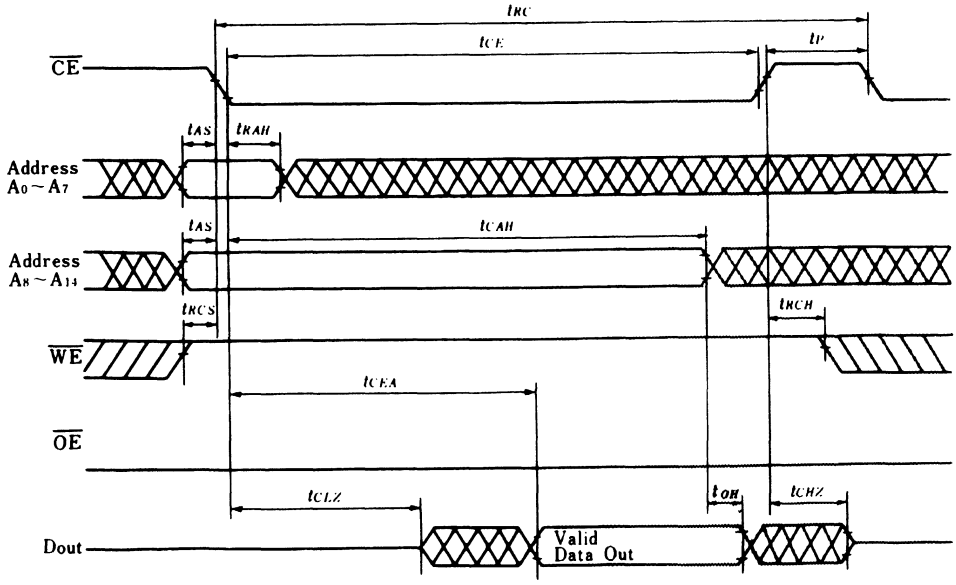
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

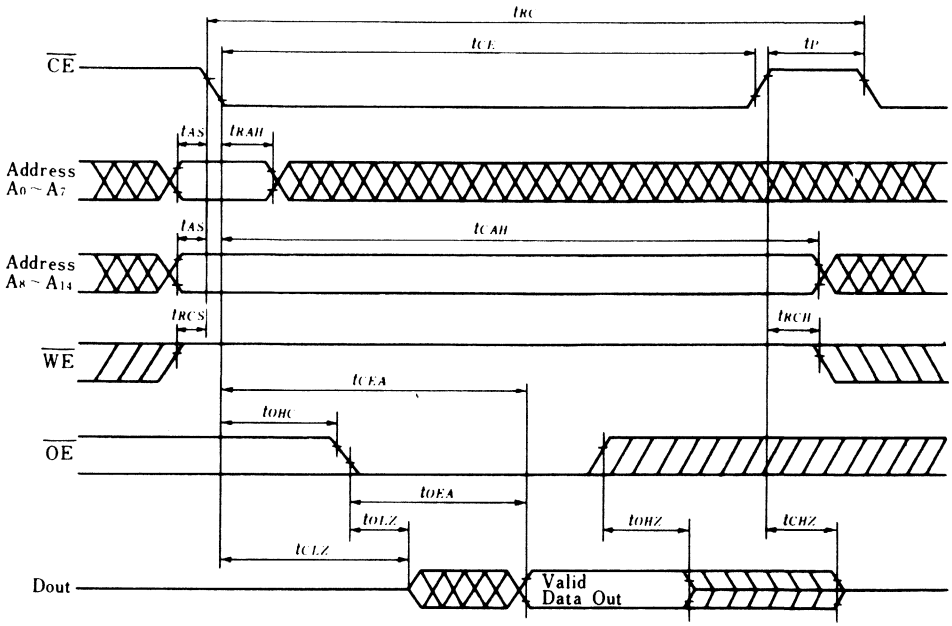
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

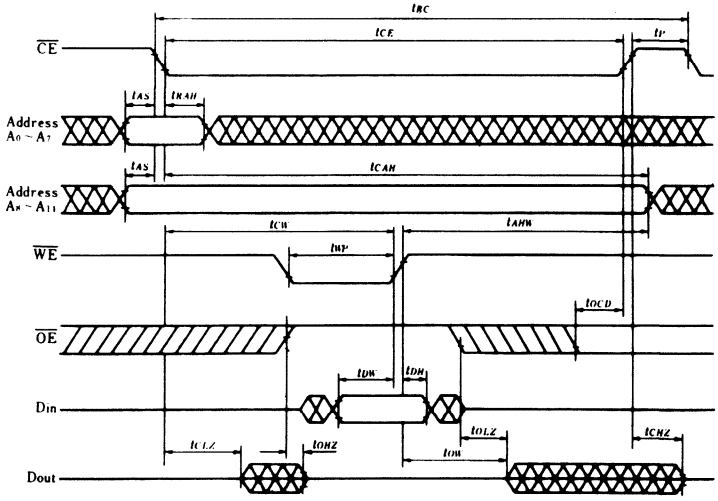
• Read Cycle No. 1 ($\overline{CE}$ controlled)



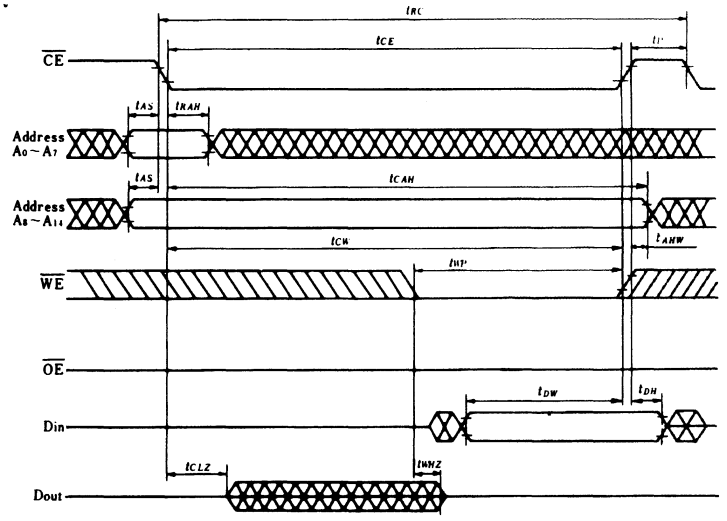
- **Read Cycle No. 2 ($\overline{OE}$ controlled)**



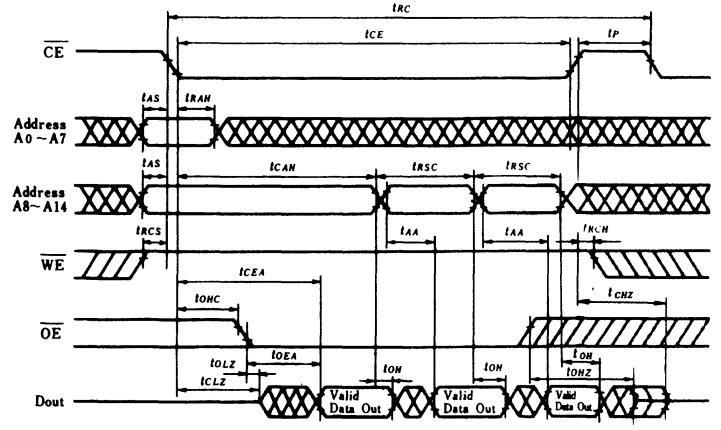
- **Write Cycle No. 1 ($\overline{OE}$ Clock)**



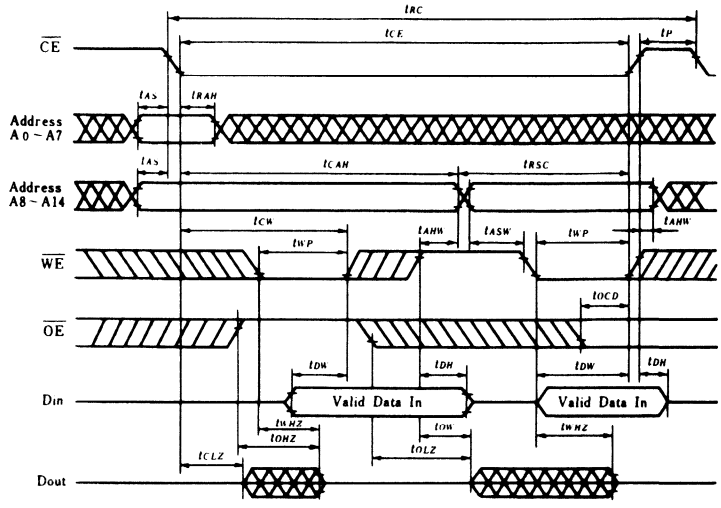
- **Write Cycle No. 2 ($\overline{OE}$ low fix)**



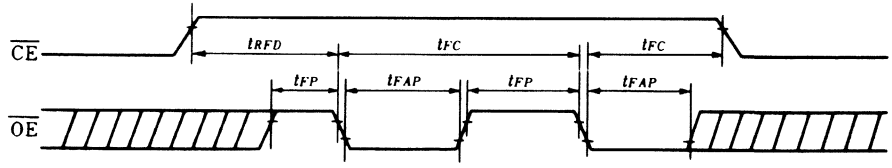
- **Static Column Mode Read Cycle**



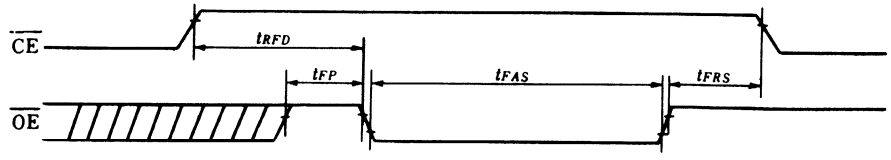
- **Static Column Mode Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



HM658128 Series

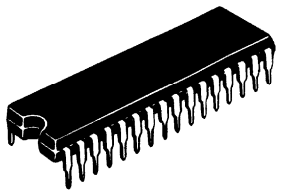
131072-word x 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128 is a pseudo-static RAM organized as 131,072-word x 8-bit. HM658128 realizes low power consumption and high speed access time by employing 1.3μm CMOS process technology.

The HM658128 supports 3 refresh functions: Address Refresh, Auto Refresh and Self Refresh. Low power version dissipates only 0.5mW (typ.) in Self Refresh Mode and retains the data with battery backup for short time. Self Refresh Mode is guaranteed only for L-version.

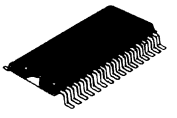
The HM658128 is pin-compatible with 256k-bit PSRAM and static RAM.

HM658128P Series



(DP-32)

HM658128FP Series



(FP-32D)

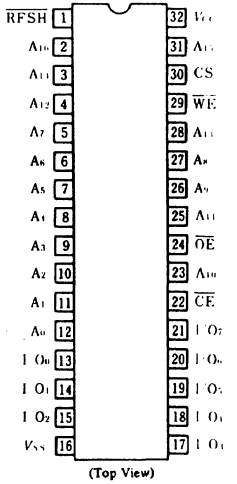
■ FEATURES

- Single 5V (±10%)
- High Speed
  - ○ Access Time
    $\overline{CE}$ Access Time . . . 100/120/150ns
  - ○ Cycle Time
    Random Read/Write Cycle Time . . . 180/210/250ns
- Low Power . . . 200mW typ. (Active)
  0.5mW (standby)
- All inputs and outputs TTL compatible
- Non Multiplexed Address
- 512 Refresh Cycles (8ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh (Only for L-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658128DP-10 HM658128DP-12 HM658128DP-15	100ns 120ns 150ns	600 mil 32 pin Plastic DIP
HM658128LP-10 HM658128LP-12 HM658128LP-15	100ns 120ns 150ns	
HM658128DFP-10 HM658128DFP-12 HM658128DFP-15	100ns 120ns 150ns	32 pin Plastic SOP
HM658128LFP-10 HM658128LFP-12 HM658128LFP-15	100ns 120ns 150ns	

■ PIN ARRANGEMENT

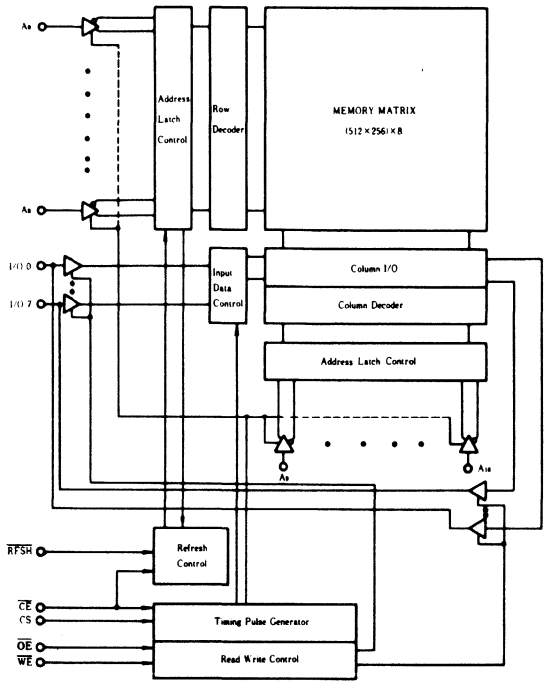


(Top View)

■ PIN DESCRIPTION

Symbol	Pin Name
A0 – A16	Address Inputs
I/O – I/O7	Data Input/Output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
CS	Chip Select
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low Z	Read
L	H	X	X	L	High Z	Write
L	H	X	H	H	High Z	–
L	L	X	X	X	High Z	CS Standby
H	X	L	X	X	High Z	Refresh*1
H	X	H	X	X	High Z	Standby

Note) *1. Self refresh is guaranteed only for L-version.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0 t_{cyc} = min.	–	40	75	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	–	1	2	mA
Standby Power Supply Current	I_{SB2}	$\overline{CE}$ ≥ V_{CC} −0.2V $\overline{RFSH}$ ≥ V_{CC} −0.2V	–	100	200	μA
Operating Power Supply Current in Self Refresh Mode*1	I_{CC2}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	–	1	2	mA
	I_{CC3}	$\overline{CE}$ ≥ V_{CC} −0.2V $\overline{RFSH}$ ≤ 0.2V	–	100	200	μA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	−10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
	V_{OH}	I_{OH} = −1mA	2.4	–	–	V

Note) *1. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	10	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level ..... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load ..... 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	180	–	210	–	250	–	ns
Random Read Modify Write Cycle Time	t_{RWC}	240	–	280	–	330	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	ns
Output Enable Access Time	t_{OEA}	–	30	–	40	–	50	ns
Chip Disable to Output in High Z	t_{CHZ}	–	30	–	35	–	40	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	35	–	40	–	ns
Output Disable to Output in HighZ	t_{OHZ}	–	25	–	30	–	35	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Enable Pulse Width	t_{CE}	100n	1μ	120n	1μ	150n	1μ	s
Chip Enable Precharge Time	t_P	70	–	80	–	90	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	30	–	35	–	40	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns
$\overline{RFSH}$ Hold Time	t_{RHC}	15	–	15	–	15	–	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	–	5	–	5	–	5	ns

(to be continued)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Chip Select Set-up Time	t_{CSS}	0	–	0	–	0	–	ns
Chip Select Hold Time	t_{CSH}	30	–	35	–	40	–	ns
Write Command Pulse Width	t_{WP}	30	–	35	–	40	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	ns
Data In to End of Write	t_{DW}	25	–	30	–	35	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	70	–	80	–	90	–	ns
Refresh Precharge Time	t_{FP}	40	–	40	–	40	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	180	–	210	–	250	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS} *9	8	–	8	–	8	–	μs
Refresh Reset Time for Self Refresh	t_{RFS} *9	180	–	210	–	250	–	ns
Refresh Reset Time for Automatic Refresh	t_{RFA}	0	–	0	–	0	–	ns
Refresh Period (512 cycles)	t_{REF}	–	8	–	8	–	8	ns

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions under the condition of t_T = 5ns and not 100% tested.

(2) t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5ns and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write end is defined at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

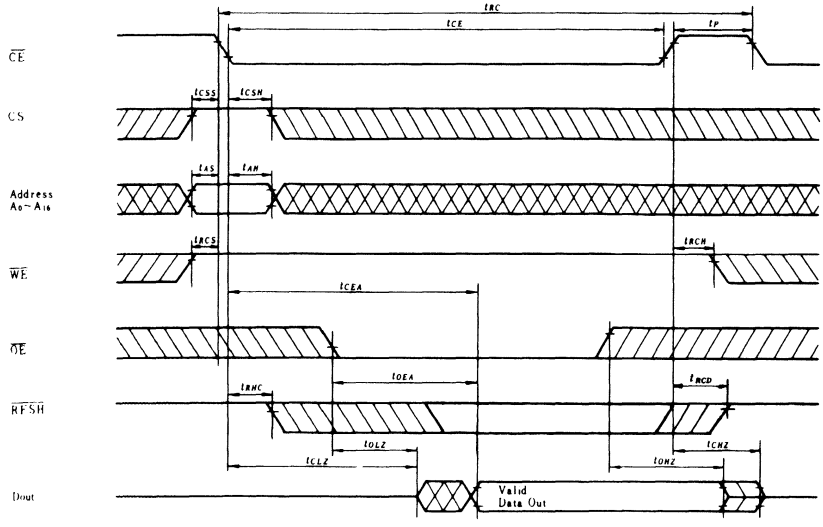
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

(8) After Self Refresh, Auto Refresh should be started within 15μs. (only for L-version)

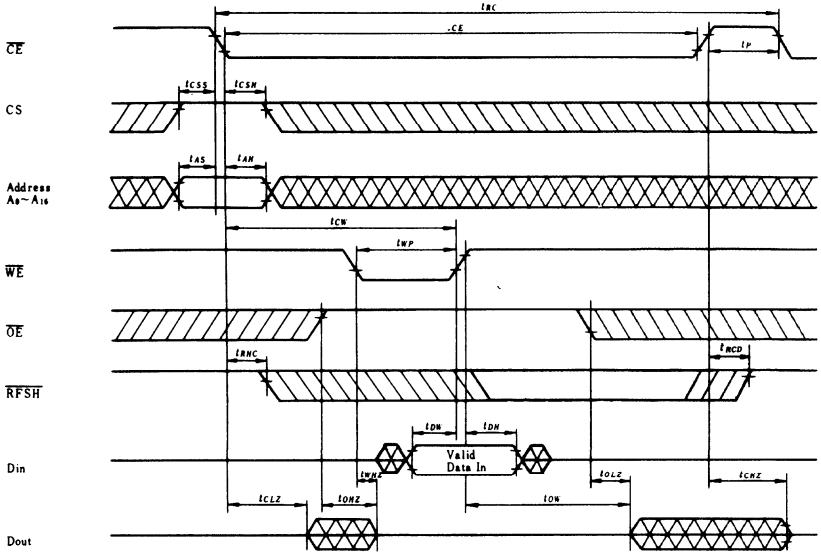
(9) This characteristics is guaranteed only for L-version.

■ TIMING WAVEFORMS

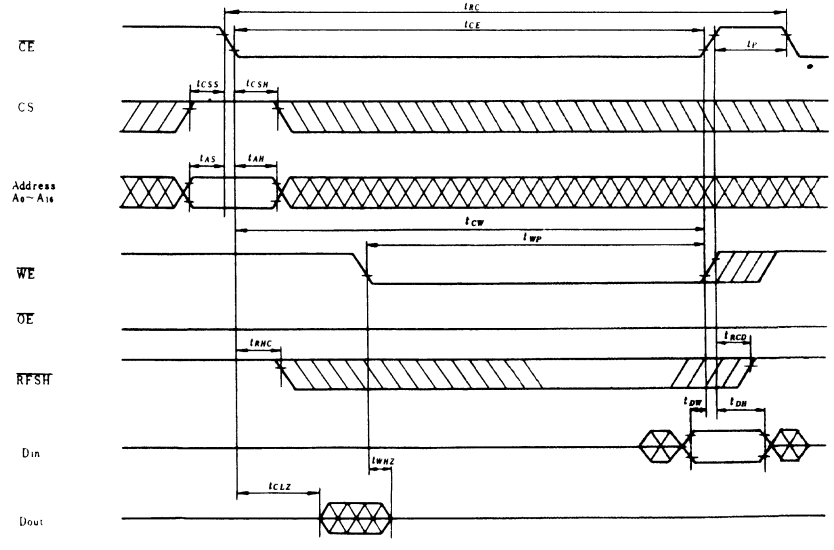
● Read Cycle



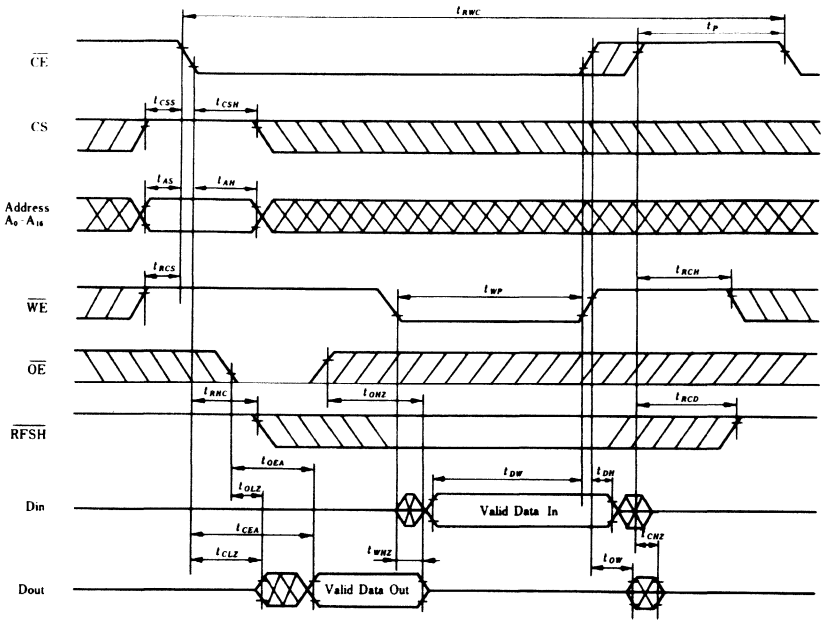
- **Write Cycle-1 ($\overline{OE}$ Clock)**



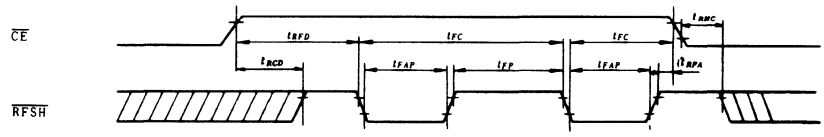
Write Cycle-2 ($\overline{OE}$ Low Fix)



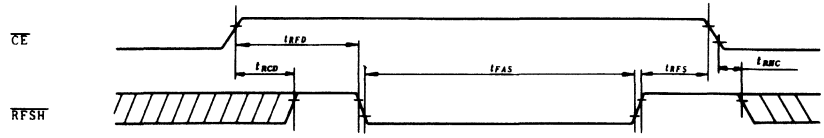
- **Read Modify Write Cycle**



- **Automatic Refresh Cycle**

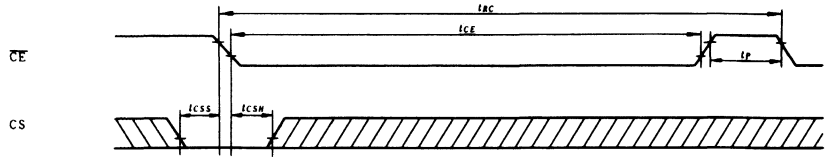


- **Self Refresh Cycle**

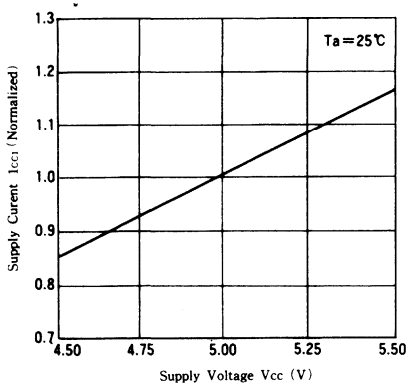


Note) Self refresh is guaranteed only for L-version.

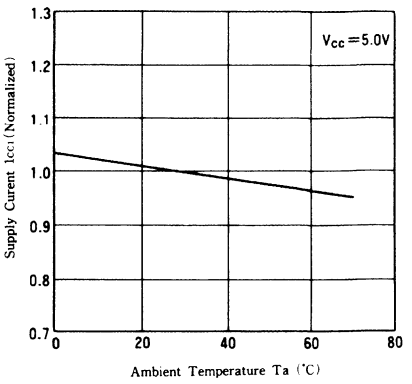
- **CS Standby Mode**



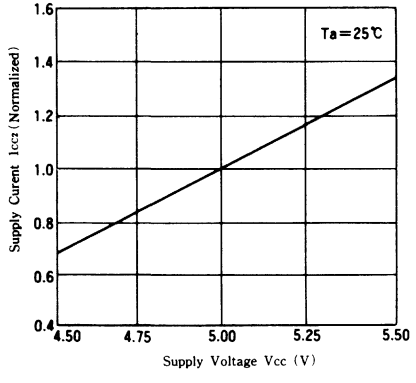
SUPPLY CURRENT VS. SUPPLY VOLTAGE(1)



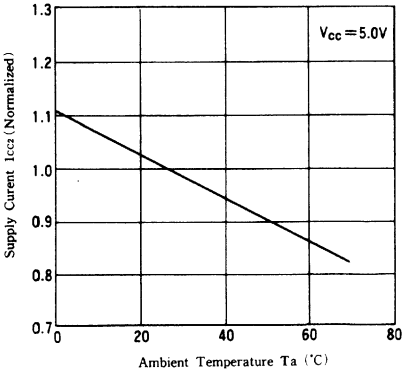
SUPPLY CURRENT VS. AMBIENT TEMPERATURE(1)



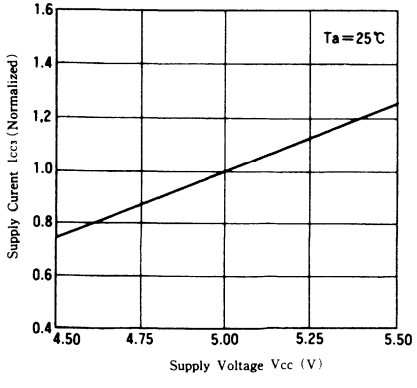
SUPPLY CURRENT VS. SUPPLY VOLTAGE(2)



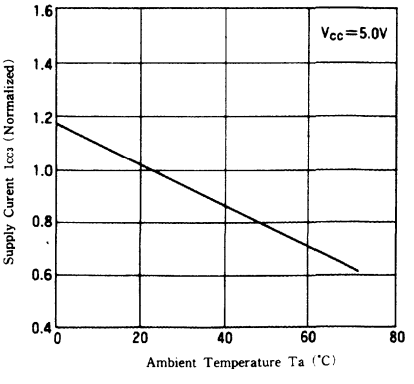
SUPPLY CURRENT VS. AMBIENT TEMPERATURE(2)



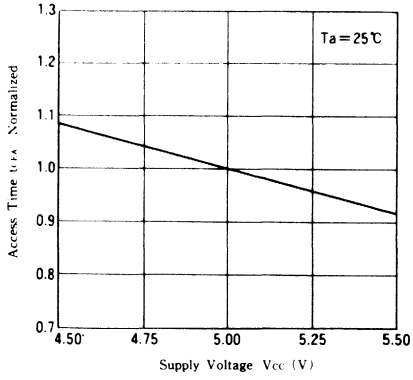
SUPPLY CURRENT VS. SUPPLY VOLTAGE(3)



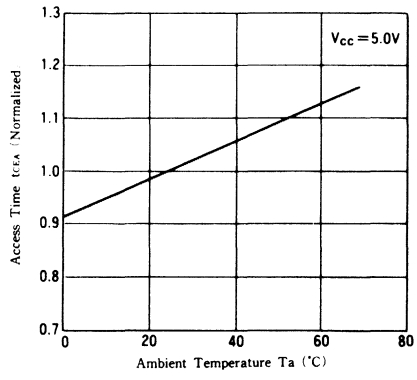
SUPPLY CURRENT VS. AMBIENT TEMPERATURE (3)



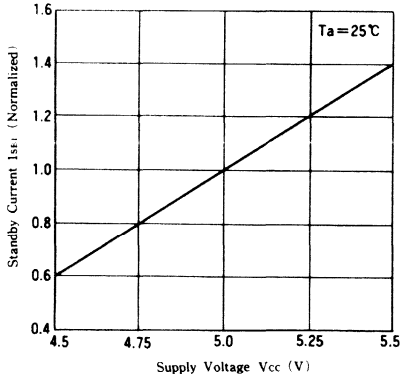
ACCESS TIME VS. SUPPLY VOLTAGE



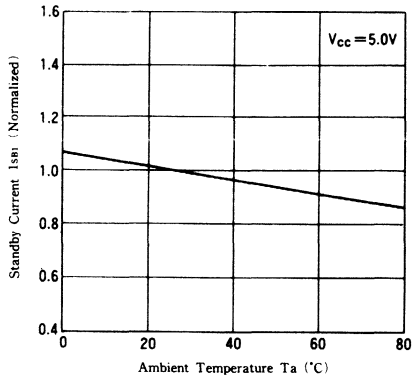
ACCESS TIME VS. AMBIENT TEMPERATURE



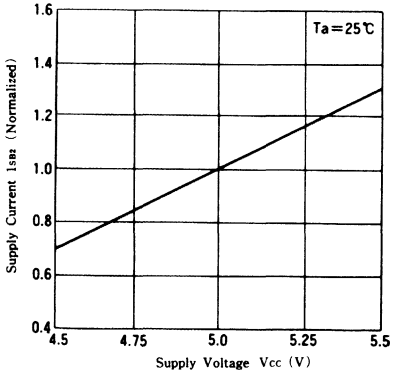
STANDBY CURRENT VS. SUPPLY VOLTAGE(1)



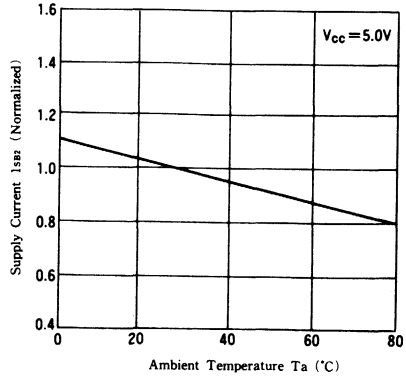
STANDBY CURRENT VS. AMBIENT TEMPERATURE (1)



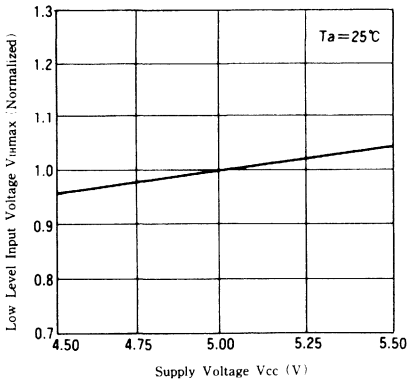
STANDBY CURRENT VS. SUPPLY VOLTAGE(2)



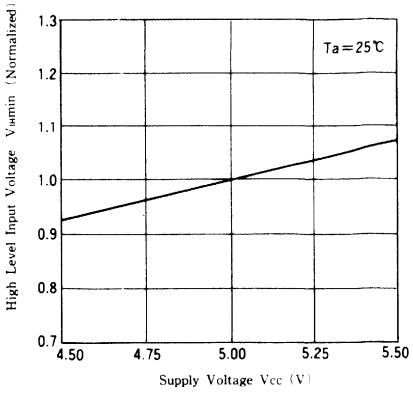
STANDBY CURRENT VS. AMBIENT TEMPERATURE(2)



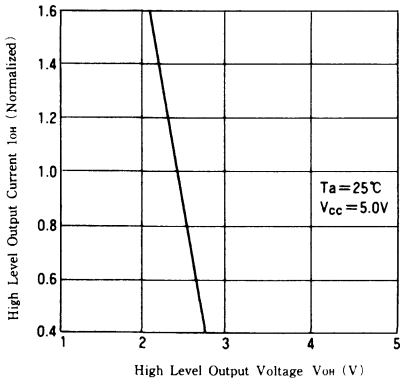
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



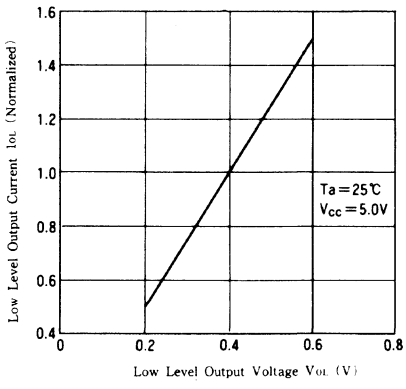
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



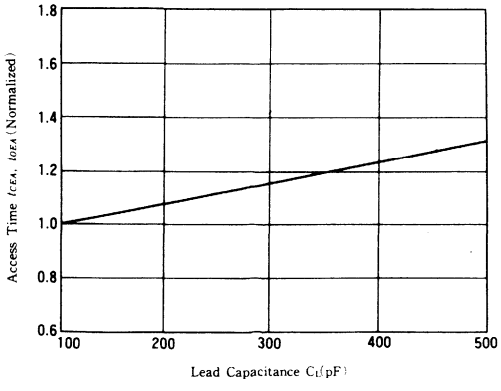
HIGH LEVEL OUTPUT CURRENT VS. OUTPUT VOLTAGE



LOW LEVEL OUTPUT CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. LOAD CAPACITANCE



HM658128A Series

131072-word x 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128A is a pseudo-static RAM organized as 131,072-word x 8-bit. HM658128A realizes low power consumption and high speed access time by employing 1.3μm CMOS process technology.

The HM658128A supports 3 refresh functions: Address Refresh, Auto Refresh and Self Refresh. Low power version dissipates only 0.5mW (type.) in Self Refresh Mode and retains the data with battery. Self Refresh Mode is guaranteed only for L-version and LL-version.

The HM658128A is pin-compatible with 1M-bit static RAM.

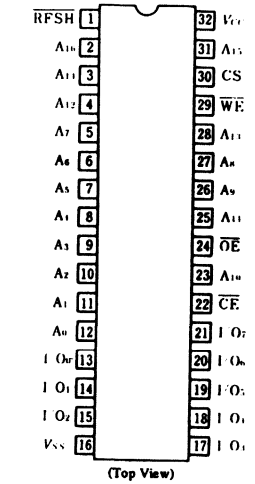
■ FEATURES

- Single 5V (±10%)
- High Speed
  - ○ Access Time
    - $\overline{CE}$ Access Time . . . 80/100/120 ns
  - ○ Cycle Time
    - Random Read/Write Cycle Time ... 130/160/190 ns
- Low Power . . . 300mW type. (Active)
  - 0.5mW (standby)
- All inputs and outputs TTL compatible
- Non Multiplexed Address
- 512 Refresh Cycles (8ms)
- Refresh Functions
  - Address Refresh
  - Automatic Refresh
  - Self Refresh (Only for L-version and LL-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658128ADP-8	80 ns	600 mil 32 pin Plastic DIP (DP-32)
HM658128ADP-10	100 ns	
HM658128ADP-12	120 ns	
HM658128ALP-8	80 ns	
HM658128ALP-10	100 ns	
HM658128ALP-12	120 ns	
HM658128ALP-8L	80 ns	
HM658128ALP-10L	100 ns	
HM658128ALP-12L	120 ns	
HM658128ADFP-8	80 ns	32 pin Plastic SOP (FP-32D)
HM658128ADFP-10	100 ns	
HM658128ADFP-12	120 ns	
HM658128ALFP-8	80 ns	
HM658128ALFP-10	100 ns	
HM658128ALFP-12	120 ns	
HM658128ALFP-8L	80 ns	
HM658128ALFP-10L	100 ns	
HM658128ALFP-12L	120 ns	

■ PIN ARRANGEMENT

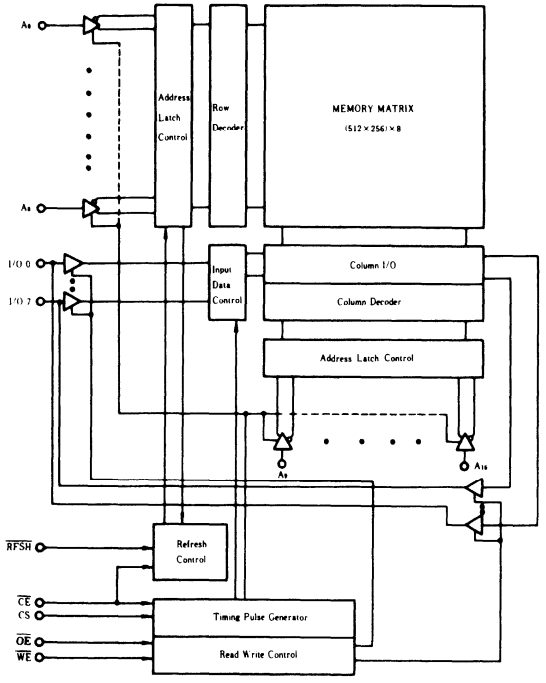


(Top View)

■ PIN DESCRIPTION

Symbol	Pin Name
A0 – A16	Address Inputs
I/O – I/O7	Data Input/Output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
CS	Chip Select
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low Z	Read
L	H	X	X	L	High Z	Write
L	H	X	H	H	High Z	–
L	L	X	X	X	High Z	CS Standby
H	X	L	X	X	High Z	Refresh*1
H	X	H	X	X	High Z	Standby

Note) *1. Self refresh is guaranteed only for L-version and LL-version.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0 t_{cyc} = min.	–	60	85	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	–	1	2	mA
Standby Power Supply Current	I_{SB2}	$\overline{CE} \geq V_{CC}$ –0.2V $\overline{RFSH} \geq V_{CC}$ –0.2V	–	100*1 70*2	200*1 100*2	µA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	–	1*1, *2	2*1, *2	mA
	I_{CC3}	$\overline{CE} \geqq V_{CC}$ –0.2V $\overline{RFSH} \leq$ 0.2V	–	100*1 70*2	200*1 100*2	µA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	–10	–	10	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	µA
Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
	V_{OH}	I_{OH} = –1mA	2.4	–	–	V

Note) *1. This characteristics is guaranteed only for L-version.
*2. This characteristics is guaranteed only for LL-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	10	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level ..... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load ..... 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM658128A-8		HM658128A-10		HM658128A-12		Unit
		min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	130	—	160	—	190	—	ns
Random Read Modify Write Cycle Time	t_{RWC}	190	—	220	—	260	—	ns
Chip Enable Access Time	t_{CEA}	—	80	—	100	—	120	ns
Output Enable Access Time	t_{OEA}	—	30	—	30	—	40	ns
Chip Disable to Output in High Z	t_{CHZ}	0	30	0	30	0	35	ns
Chip enable to Output in Low Z	t_{CLZ}	20	—	20	—	20	—	ns
Output Disable to Output in High Z	t_{OHZ}	—	25	—	25	—	30	ns
Output Enable to Output in Low Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip Enable Pulse Width	t_{CE}	80ns	10µs	100ns	10µs	120ns	10µs	
Chip Enable Precharge Time	t_P	40	—	50	—	60	—	ns
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns
Address Hold Time	t_{AH}	30	—	30	—	35	—	ns
Read Command set-up Time	t_{RCS}	0	—	0	—	0	—	ns
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns

(continued to next page)

Item	Symbol	HM658128A-8		HM658128A-10		HM658128A-12		Unit
		min.	max.	min.	max.	min.	max.	
$\overline{RFSH}$ Hold Time	t_{RHC}	15	—	15	—	15	—	ns
Chip Select Set-up Time	t_{CSS}	0	—	0	—	0	—	ns
Chip Select Hold Time	t_{CSH}	30	—	30	—	35	—	ns
Write Command Pulse Width	t_{WP}	30	—	30	—	35	—	ns
Chip Enable to End of Write	t_{CW}	80	—	100	—	120	—	ns
Data In to End of Write	t_{DW}	25	—	25	—	30	—	ns
Data In Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	ns
Write to Output in High Z	t_{WHZ}	—	25	—	25	—	30	ns
Transition time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	40	—	50	—	60	—	ns
Refresh Precharge Time	t_{FP}	40	—	40	—	40	—	ns
Refresh Command Pulse Width	t_{RP}	—	8	—	8	—	8	μs
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80ns	8μs	80ns	8μs	80ns	8μs	
Automatic Refresh Cycle Time	t_{FC}	130	—	160	—	190	—	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}*9	8	—	8	—	8	—	μs
Refresh Reset Time for Self Refresh	t_{RFS}*9	130	—	160	—	190	—	ns
Refresh Period (512 cycles)	t_{REF}	—	8	—	8	—	8	ms

Notes:
(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.
(2) t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T =5ns and not 100% tested.
(3) A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write ends at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
(4) If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
(5) In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
(6) Transition time t_T is measured between V_{IH} min and V_{IL} max.
(7) After power-up, pause more than 100μs and execute at least 8 initialization cycles.
(8) 512 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15μs after self refresh, in order to meet the refresh specification of 8ms and 512 cycles.
(9) This characteristics is guaranteed only for L-version and LL-version.

■ TIMING WAVEFORMS

Refer to the HM658128 data sheet for timing waveforms.

HM658512 Series — Preliminary

524288-Word × 8-Bit High Speed Pseudo Static RAM

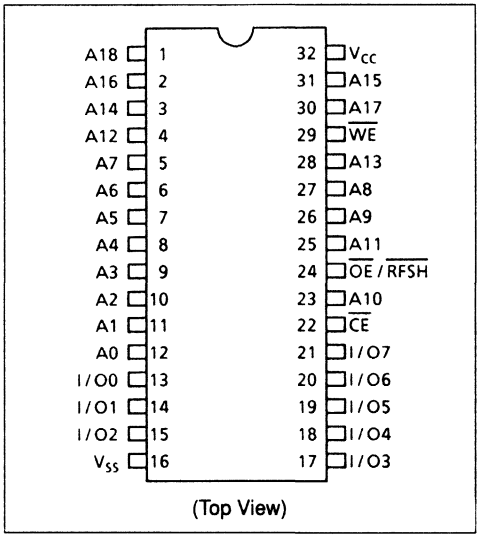
Features

- Single 5 V (±10%)
- High speed
  - Access time
    $\overline{CE}$ access time: 80/100/120 ns
  - Cycle time
    Random read/write cycle time:
    160/180/210 ns
- Low power
  - 250 mW typ active
  - 350 µW typ standby (L-version)
  - 200 µW typ standby (LL-version)
- All inputs and outputs TTL compatible
- Package
  - 32-pin dual-in-line plastic package
  - 32-pin SOP package
- Non multiplexed address
- 2048 refresh cycles (32 ms)
- Refresh functions
  - L-version: Address refresh
    LL-version Automatic refresh
    Self refresh
  - D-version: Address refresh
    Automatic refresh

Pin Description

Pin name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$/RFSH	Output enable/refresh
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Pin Arrangement



(Top View)

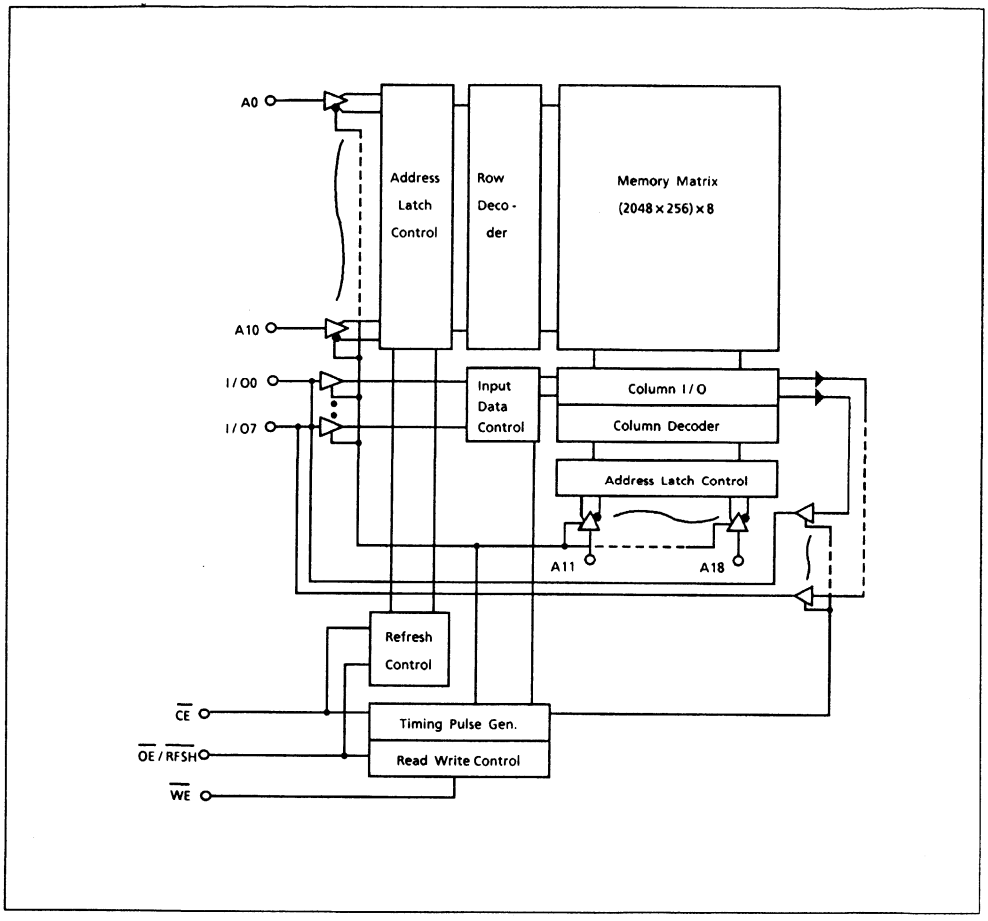
Ordering Information

Type No.	Access	Package
HM658512LP-8	80 ns	600 mil 32-pin
HM658512LP-10	100 ns	plastic DIP
HM658512LP-12	120 ns	(DP-32)
HM658512LP-8L*1	80 ns	
HM658512LP-10L*1	100 ns	
HM658512LP-12L*1	120 ns	
HM658512DP-8	80 ns	
HM658512DP-10	100 ns	
HM658512DP-12	120 ns	
HM658512LFP-8	80 ns	32-pin plastic
HM658512LFP-10	100 ns	SOP
HM658512LFP-12	120 ns	(FP-32D)
HM658512LFP-8L*1	80 ns	
HM658512LFP-10L*1	100 ns	
HM658512LFP-12L*1	120 ns	
HM658512DFP-8	80 ns	
HM658512DFP-10	100 ns	
HM658512DFP-12	120 ns	

Note: 1. LL-version (LP-8L, LP-10L, LP-12L, LFP-8L, LFP-10L, LFP-12L) will be available in the second half of 1990.

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Function Table

$\overline{CE}$	$\overline{OE}$/RFSH	$\overline{WE}$	I/O pin	Mode
L	L	H	Low-Z	Read
L	X	L	High-Z	Write
L	H	H	High-Z	—
H	L	X	High-Z	Refresh *2
H	H	X	High-Z	Standby

Notes: 1. X means don't care
2. Self refresh is guaranteed only for L-version and LL-version.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage with respect to V_{SS}	V_T	−1.0 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−1.0 *1	—	0.8	V

Note: 1. V_{IL} min = −3.0 V for pulse width 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating power supply current	I_{CC1}	—	—	75	mA	$I_{I/O}$ = 0 tcyc = min
Standby power supply current	I_{SB1}	—	1	2	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/$\overline{RFSH}$ = V_{IH}
	I_{SB2}	—	20 *1	200 *1	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V $\overline{OE}$/$\overline{RFSH}$ ≥ V_{CC} − 0.2 V
			15 *2	100 *2	µA	
Operating power supply current in self refresh mode	I_{CC2}	—	1 *1,2	2 *1,2	mA	$\overline{CE}$ = V_{IH} $\overline{OE}$/$\overline{RFSH}$ = V_{IL}
	I_{CC3}	—	70 *1	200 *1	µA	$\overline{CE}$ ≥ V_{CC} − 0.2 V $\overline{OE}$/$\overline{RFSH}$ ≤ 0.2 V
			40 *2	100 *2	µA	
Input leakage current	I_{LI}	−10	—	10	µA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}

Notes: 1. This characteristics is guaranteed only for L-version.
2. This characteristics is guaranteed only for LL-version.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output leakage current	I_{LO}	−10	—	10	µA	$\overline{OE}/\overline{RFSH}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = −1 mA

Capacitance

Item	Symbol	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	8	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%)

Test Conditions

Input pulse levels: 2.4 V, 0.4 V
Input rise and fall times: 5 ns
Timing measurement level: 2.2 V, 0.8 V
Reference level: V_{OH} = 2.0 V, V_{OL} = 0.8 V
Output load: 1 TTL and 100 pF

		HM658512-8		HM658512-10		HM658512-12			
Item	Symbol	Min	Max	Min	Max	Min	Max	Unit	Note
Random read or write cycle time	t_{RC}	160	—	180	—	210	—	ns	
Chip enable access time	t_{CEA}	—	80	—	100	—	120	ns	
Read-modify-write cycle time	t_{RWC}	—	220	—	240	—	280	ns	
Output enable access time	t_{OEA}	—	30	—	40	—	50	ns	
Chip disable to output in high-Z	t_{CHZ}	0	25	0	25	0	30	ns	1
Chip enable to output in low-Z	t_{CLZ}	20	—	20	—	20	—	ns	2

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ±10%) (cont)

Item	Symbol	HM658512-8		HM658512-10		HM658512-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
Output disable to output in high-Z	t_{OHZ}	—	25	—	25	—	30	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	0	—	0	—	ns	2
Chip enable pulse width	t_{CE}	80 ns	10 µs	100 ns	10 µs	120 ns	10 µs		
Chip enable precharge time	t_P	70	—	70	—	80	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	
Address hold time	t_{AH}	20	—	25	—	30	—	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	
Write command pulse width	t_{WP}	25	—	30	—	35	—	ns	
Chip enable to end of write	t_{CW}	80	—	100	—	120	—	ns	
Chip enable to output enable delay time	t_{OCD}	0	—	0	—	0	—	ns	
Output enable hold time	t_{OHC}	15	—	15	—	15	—	ns	
Data in to end of write	t_{DW}	20	—	25	—	30	—	ns	
Data in hold time for write	t_{DH}	0	—	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	5	—	ns	2
Write to output in high-Z	t_{WHZ}	—	20	—	25	—	30	ns	1
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	6
Refresh command delay time	t_{RFD}	70	—	70	—	80	—	ns	
Refresh precharge time	t_{FP}	40	—	40	—	40	—	ns	
Refresh command pulse width for automatic refresh	t_{FAP}	80 ns	8 µs	80 ns	8 µs	80 ns	8 µs		

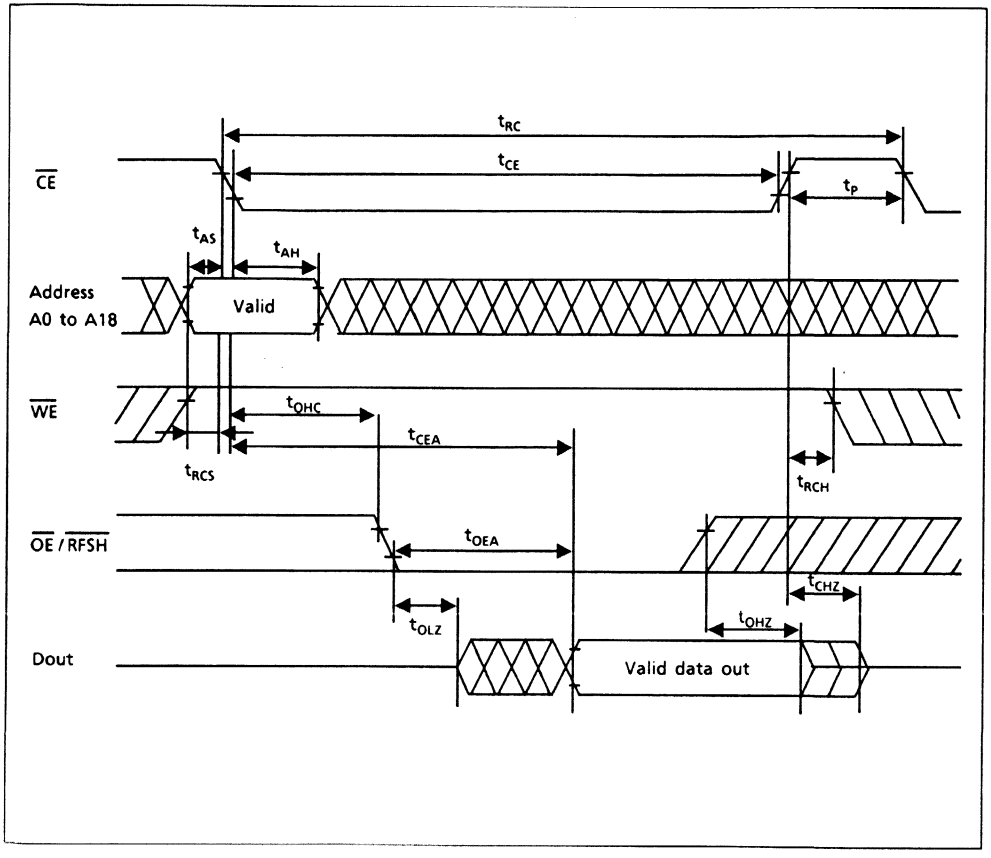
AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ±10%) (cont)

Item	Symbol	HM658512-8 Min	HM658512-8 Max	HM658512-10 Min	HM658512-10 Max	HM658512-12 Min	HM658512-12 Max	Unit	Note
Automatic refresh cycle time	t_{FC}	160	—	180	—	210	—	ns	
Refresh command pulse width for self refresh	t_{FAS}*9	8	—	8	—	8	—	µs	
Refresh reset time from self refresh	t_{RFS}*9	600	—	600	_	600	—	ns	
Refresh period	t_{REF}	—	32	—	32	—	32	ms	2048 cycle

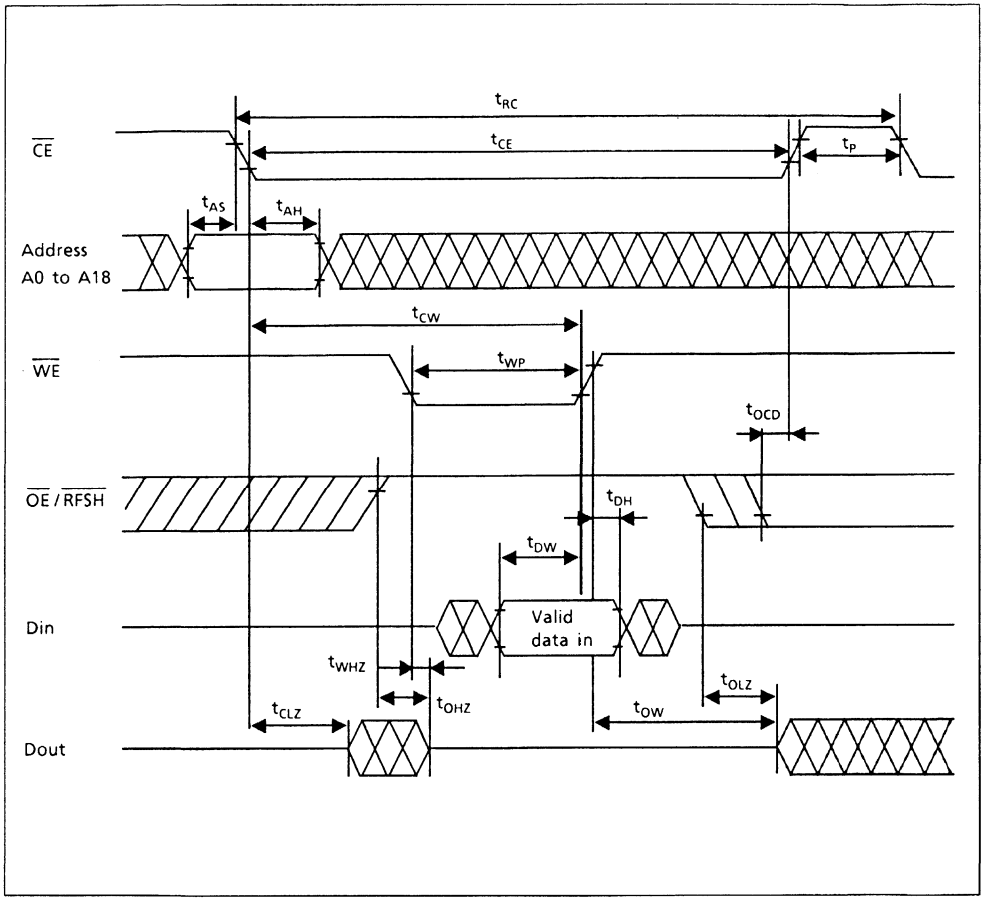
Notes:
1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit condition.
2. t_{CHZ}, t_{CLZ} t_{OHZ} t_{OLZ},t_{WHZ} and t_{OW}, are sampled under the condition of t_T = 5 ns and not 100% tested.
3. A write occurs during the overlap of low $\overline{CE}$ and low $\overline{WE}$.
4. If the $\overline{CE}$ low transition occurs simultaneously with or latter from the $\overline{WE}$ low transition, the output buffers remain in high impedance state.
5. In write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and at the end of write cycle data inputs must be floated prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
6. Transition time t_T is measured between V_{IH} min and V_{IL} max.
7. After power-up, pause for more than 100 µs and execute at least 8 initialization cycles.
8. 2048 cycles of burst refresh or the first cycle of distributed automatic refresh must be executed within 15µs after self refresh, in order to meet the refresh specification of 32 ms and 2048 cycles.
9. This characteristics is guaranteed only for L-version and LL-version.

Timing Waveforms

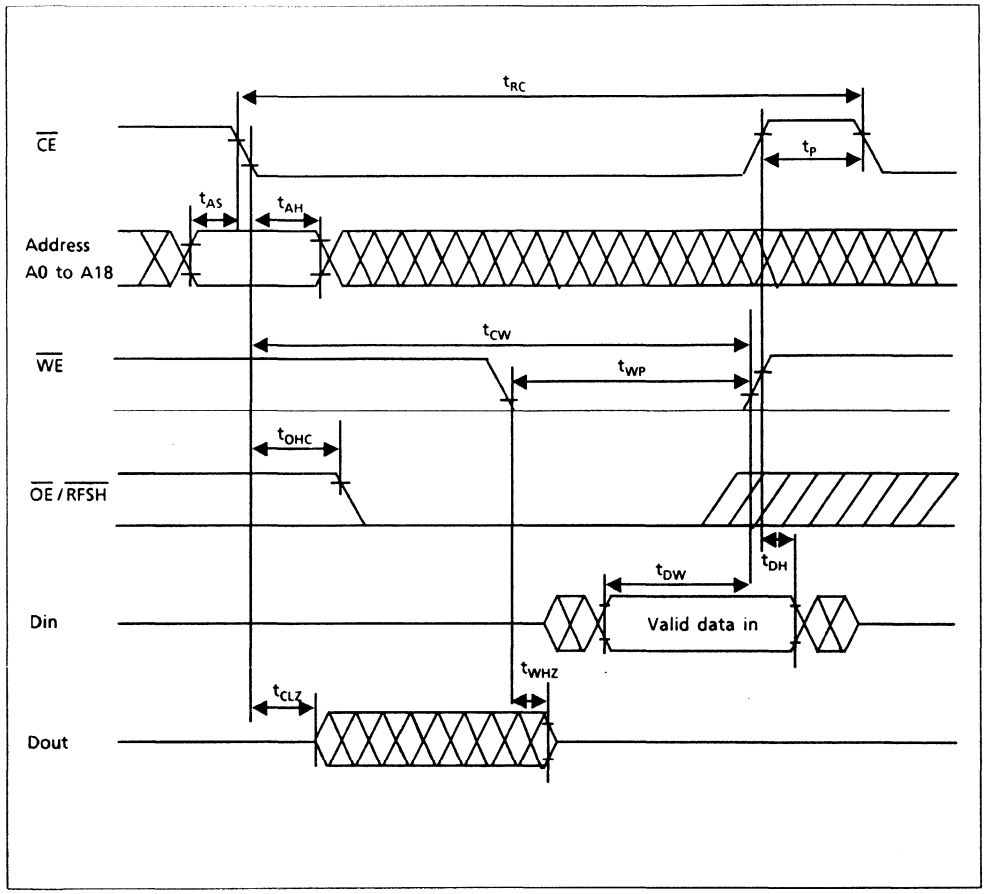
Read Cycle



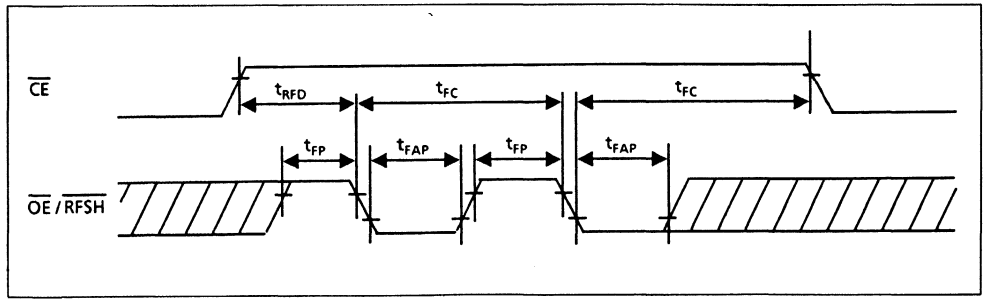
Write Cycle (1) ($\overline{OE}$ High)



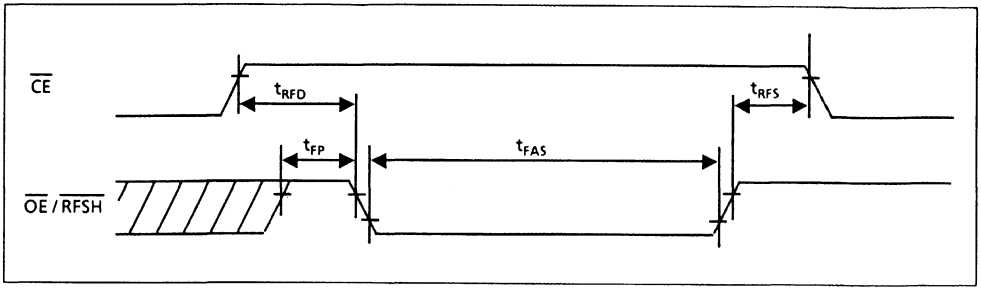
Write Cycle (2) ($\overline{OE}$ Low)



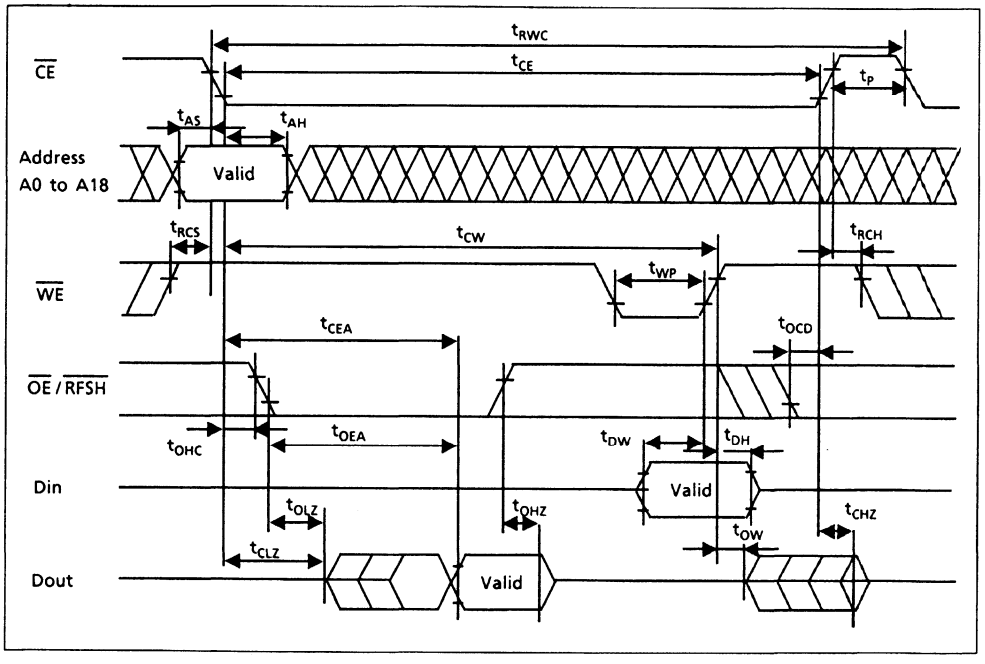
Automatic Refresh Cycle

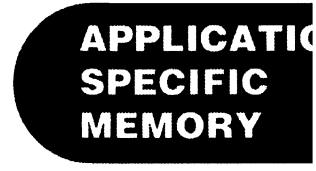


Self Refresh Cycle



Read-Modify-Write Cycle

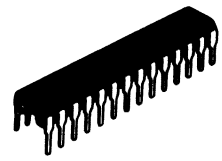



APPLICATI
SPECIFIC
MEMORY

HM63021 Series

2048-word x 8-bit Line Memory

HM63021 is a 2048-word x 8-bit static Serial Access Memory (SAM) with separate data inputs and outputs. Since it has an internal address counter, no external address signal is required and internal addresses are scanned serially. Using five different address scan modes, it is applicable to FIFO memories, double-speed conversions, 1H delay lines and 1H/2H delay lines for digital TV signals. Its minimum cycle times are 28 ns and 34 ns each corresponding to 8 fsc of PAL TV signals and NTSC TV signals. All inputs and outputs are TTL-compartiable. This device is packaged in a 300-mil dual-in-line plastic package.



(DP-28N)

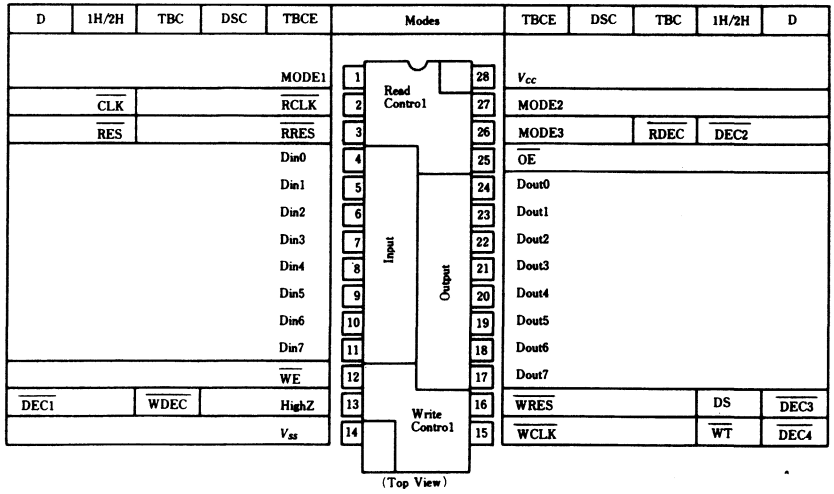
Features

- Five modes for various applications
- Corresponds to Digital TV system with 4 fsc sampling (PAL, NTSC)
- Decoder signal output pin; Fewer external circuits
- Asynchronous Read/Write operation;
  Separate address counters for Read/Write
  No Address Input required
- High Speed; Cycle Time 28/34/45 ns (min)
- Completely Static Memory; No refresh required
- 8-bit SAM with separate I/O
- Low Power; 250 mW typ. Active
- Single 5 V supply
- TTL compatible

Ordering Information

Type No.	Cycle Time	Package
HM63021P-28	28 ns	300-mil 28-pin Plastic DIP
HM63021P-34	34 ns	
HM63021P-45	45 ns	

Pin Arrangement



Pin Description

Pin No.	Pin Name	Functions
1	MODE1	Mode Input 1 (All Modes)
2	$\overline{RCLK}/\overline{CLK}$	Read Clock Input (TBCE, DSC, TBC) Clock Input (1H/2H, D)
3	$\overline{RRES}/\overline{RES}$	Read Reset Input (TBCE, DSC, TBC) Reset Input (1H/2H, D)
4-11	Din 0 – Din 7	Data Inputs (All Modes)
12	$\overline{WE}$	Write Enable Input (All Modes)
13	High Z/$\overline{WDEC}/\overline{DEC1}$	High Impedance (TBCE, DSC) Write Decode Pulse Output (TBC) Decode Pulse Output 1 (1H/2H, D)
14	V_{SS}	Ground (All Modes)
15	$\overline{WCLK}/\overline{WT}/\overline{DEC4}$	Write Clock Input (TBCE, DSC, TBC) Write Timing Input (1H/2H) Decode Pulse Output 4 (D)
16	$\overline{WRES}$/DS/$\overline{DEC3}$	Write Reset Input (TBCE, DSC, TBC) Delay Select Input (1H/2H) Decode Pulse Output 3 (D)
17-24	Dout 0 – Dout 7	Data Outputs (All Modes)
25	$\overline{OE}$	Output Enable Input (All Modes)
26	MODE3/$\overline{RDEC}/\overline{DEC2}$	Mode Input 3 (TBCE) Read Decode Pulse Output (TBC) Decode Pulse Output 2 (1H/2H, D)
27	MODE2	Mode Input 2 (All Modes)
28	V_{CC}	Power Supply (+5V) (All Modes)

Mode Table

Mode Signals			Mode	Application Example
MODE1	MODE2	MODE3		
H	H	H	Time base compression/expansion (TBCE)	Picture in Picture
H	H	L	Double speed conversion (DSC)	Non interlace
H	L	– *1	Time base correction (TBC)	Time Base Corrector
L	H	– *1	1H/2H delay (1H/2H)	Vertical filter
L	L	– *1	Delay line (D)	Delay line

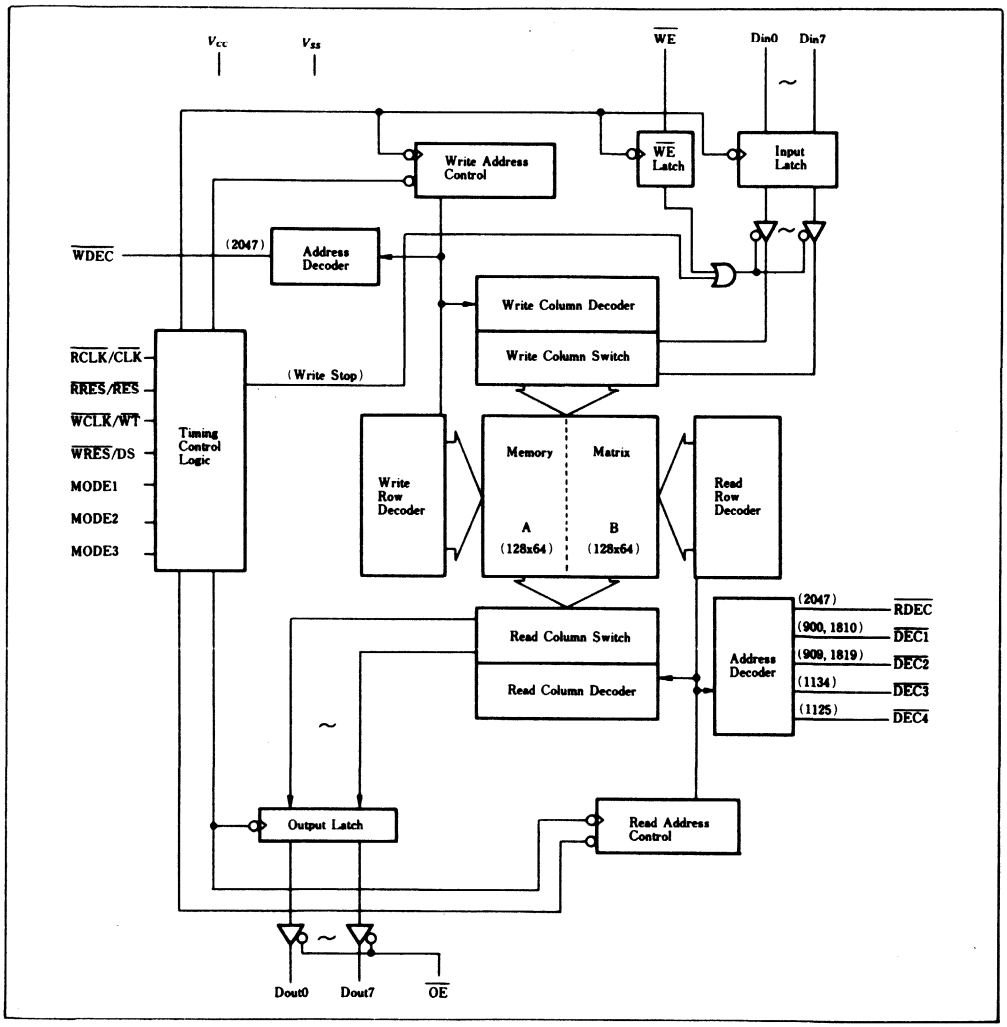
Note) *1. Decoder Output Signal ($\overline{RDEC}$, $\overline{DEC2}$)

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin relative to V_{SS}	V_T	-0.5^{*1} to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

Note) *1. −3.5V for pulse width $\leqq$ 10 ns

Block Diagram



Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.4	–	6.0	V
	V_{IL}	−0.5 *1	–	0.8	V

Note) *1. −3.0V for pulse width ≤ 10 ns.

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	min	typ*1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	10	μA	V_{CC} = 5.5 V Vin = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{OE}$ = V_{IH} V_{out} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	50	90	mA	Min. cycle, Iout*2 = 0 mA
Output Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA*3, Dout 0 to Dout 7, $\overline{DEC}$ Output pin
	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA, Dout 0 to Dout 7 pin
		2.4	–	–	V	I_{OH} = -1 mA, $\overline{DEC}$ Output pin

Notes) *1. Typical values are at V_{CC} = 5V, Ta = 25 °C and for reference only.
*2. Dout and $\overline{DEC}$
*3. I_{OL} = 6mA for 45ns version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

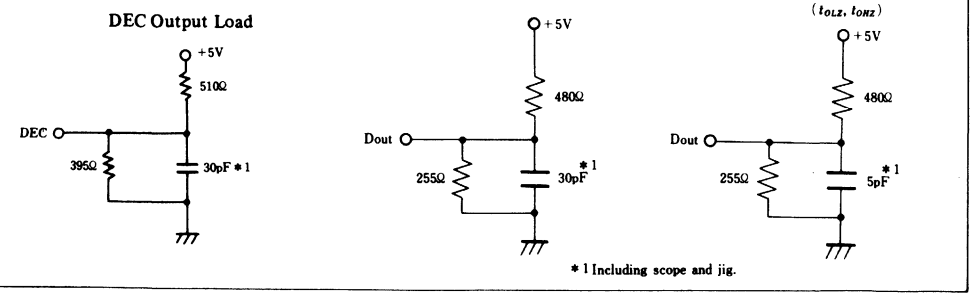
Parameter	Symbol	min	typ	max	Unit	Conditions
Input Capacitance	Cin	–	–	6	pF	Vin = 0V
Output Capacitance*2	Cout	–	–	9	pF	Vout = 0V

Notes) *1. This parameter is sampled and not 100% tested.
*2. 13, 15 – 24, 26 pin

AC Characteristics (V_{CC} = 5V ± 10%, Ta = 0 to +70°C, unless otherwise noted.)

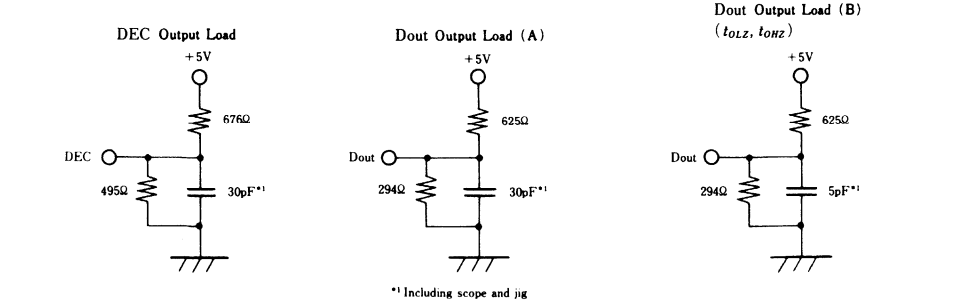
- AC Test Conditions
  Input and Output timing reference levels: 1.5V
  Input pulse levels: V_{SS} to 3V
  Input rise and fall times: 5 ns

HM63021-28/34



*1 Including scope and jig.

HM63021-45



*1 Including scope and jig

Read Cycle

Parameter		Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	28	–	34	–	45	–	ns
Read Clock Width		t_{RWL}	10	–	10	–	15	–	ns
		t_{RWH}	10	–	10	–	15	–	ns
Access Time		t_{AC}	–	20	–	25	–	30	ns
Decode Output Access Time	(fall)	t_{DA1}	–	20	–	25	–	30	ns
	(rise)	t_{DA2}	–	40	–	50	–	60	ns
Output Hold Time		t_{OH}	5	–	5	–	5	–	ns
Decode Output Hold Time	(fall)	t_{DOH1}	5	–	5	–	5	–	ns
	(rise)	t_{DOH2}	5	–	5	–	5	–	ns
Output Enable Access Time		t_{OE}	–	20	–	25	–	30	ns
Output Disable to Output in High Z		t_{OHZ}	0	15	0	20	0	25	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns

Write Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	28	–	34	–	45	–	ns
	t_{WC}(1H/2H Mode)	56	–	68	–	90	–	ns
Write Clock Width	t_{WWL}	10	–	10	–	15	–	ns
	t_{WWH}	10	–	10	–	15	–	ns
Input Data Setup Time	t_{DS}	5	–	5	–	7	–	ns
Input Data Hold Time	t_{DH}	5	–	5	–	7	–	ns
$\overline{WE}$ Setup Time	t_{WESL}	5	–	5	–	7	–	ns
	t_{WESH}	5	–	5	–	7	–	ns
$\overline{WE}$ Hold Time	t_{WEHL}	5	–	5	–	7	–	ns
	t_{WEHH}	5	–	5	–	7	–	ns
$\overline{WT}$ Setup Time	t_{WTSL}	5	–	5	–	7	–	ns
	t_{WTSH}	5	–	5	–	7	–	ns
$\overline{WT}$ Hold Time	t_{WTHL}	5	–	5	–	7	–	ns
	t_{WTHH}	5	–	5	–	7	–	ns

Reset Cycle

Parameter	Symbol	HM63021-28		HM63021-34		HM63021-45		Unit
		min	max	min	max	min	max	
Reset Setup Time	t_{RES}	8	–	9	–	10	–	ns
Reset Hold Time	t_{REH}	5	–	5	–	7	–	ns
Clock Setup Time Before Reset	t_{REPS}	8	–	9	–	10	–	ns
Clock Hold Time Before Reset	t_{REPH}	5	–	5	–	7	–	ns

Mode Description

- Time Base Compression/Expansion Mode
  This mode turns HM63021 into a 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address clock and are reset to address 0. A write-inhibit function of HM63021 stops writing automatically after the data has been written into all addresses 0 to 2047. The write-inhibit function is released by reset using $\overline{WRES}$, and the HM63021 restarts writing into address 0.
- Double-Speed Conversion Mode
  This mode turns HM63021 into a 1024-word x

8-bit x 2 memory with asynchronous input/output. It is used for generating non-interlaced TV signals. When the original signal and the interpolated signal (1 field delay) of interlaced signals are input to the HM63021, multiplexed per dot, it outputs non-interlaced signals for each line. 8 fsc should be input to $\overline{RCLK}$ and $\overline{WCLK}$. A standard H synchronizing signal and a non-interlace H synchronizing signal are input to $\overline{WRES}$ and $\overline{RRES}$ respectively. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135-1024 = 111 bits) is ignored.

- TBC Mode
  This mode turns HM63021 into 2048-word x 8-bit FIFO memory with asynchronous input/output. The HM63021 provides 2 clocks ($\overline{RCLK}$, $\overline{WCLK}$) and 2 resets ($\overline{RRES}$, $\overline{WRES}$), one each for read and write. The internal address counters increment by 1 address at each clock and are reset to address 0. The internal address counters return to address 0 after they reach address 2047. The HM63021 outputs a write decode pulse from $\overline{WDEC}$, synchronizing it with address 2047 in the write address counter, and read a decode pulse from $\overline{RDEC}$, synchronizing with address 2047 in the read address counter. Using these pulses, the memory area can be extended easily (multiple-HM63021s can be used with ease).

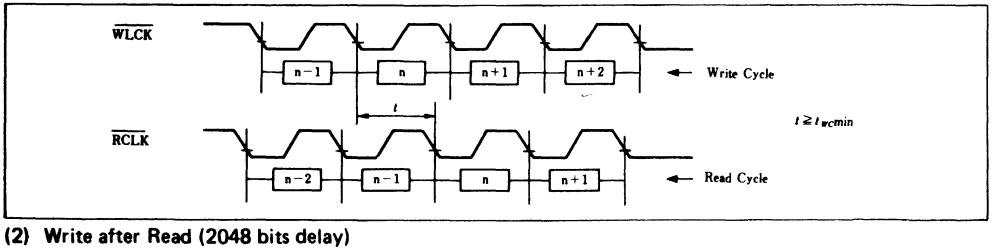
- 1H/2H Delay Mode
  This mode turns HM63021 into a 1024-word x 8-bit x 2 delay line with synchronous input/output. Delay time is defined by the reset period of $\overline{RES}$. Since the HM63021 outputs a 901 decode pulse ($\overline{DEC1}$) and a 910 decode pulse ($\overline{DEC2}$), connecting $\overline{DEC2}$ to $\overline{RES}$, for example, outputs 1H- and 2H- delayed signals alternately at a 8- fsc cycle when the original signal is input at a 4- fsc cycle. A write-inhibit function is provided in this mode, making it applicable to PAL TV, where extra data (1135-1024 = 111 bits) is ignored.

- Delay Line Mode
  This mode turns HM63021 into a 2048-word x 8-bit delay line with synchronous input/output. Delay time (3 to 2048 bits) is defined by the reset period of $\overline{RES}$. The delay is 2048 bits when $\overline{RES}$ is fixed High. Signals delayed by 910 bits to 1135 bits for example, can be easily obtained without external circuits by just connecting selected decoded pulses on $\overline{DEC1}$ – $\overline{DEC4}$ to $\overline{RES}$.

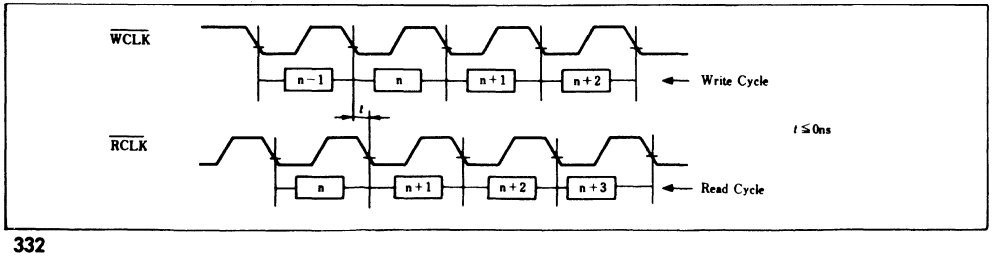
Notes on Using HM63021

- Hitachi recommends that pin 13 (high impedance) should be fixed by pulling up or down with a resistor (of several kΩ) in TBC or DSC mode.
- Hitachi recommends that the mode signal input pins and DS pin should be fixed by pulling them up or down with a resistor (of several kΩ).
- Data integrity cannot be guaranteed when mode or DS is changed during operation
- When a read address coincides with a write address in TBCE, TBC or DSC mode, the data is written correctly but it is not always read correctly.

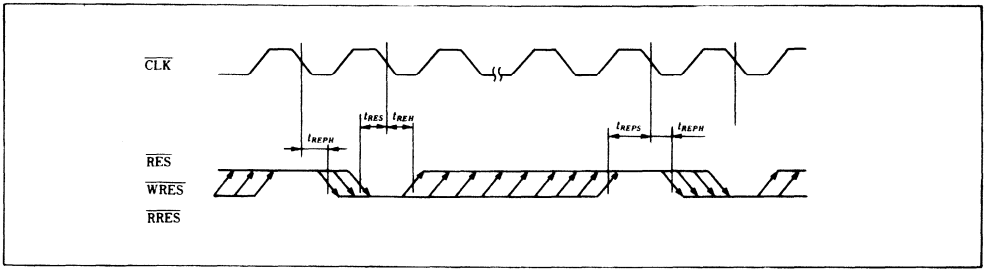
(1) Read after Write (3 bits delay)



(2) Write after Read (2048 bits delay)

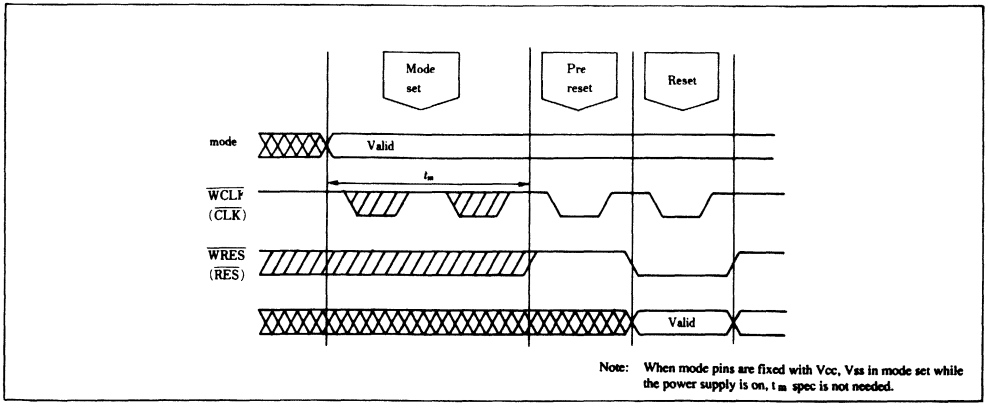


- At power on, the output of the address counter is not defined. Therefore, operations before the system is reset cannot be guaranteed, and decode signal output is not defined until after the first reset cycle.
- The decode signal is latched by a decode output latch circuit at the previous address of the internal counter address and is output synchronized with the next address. For example, $\overline{WDEC}$ in TBC mode is latched at write address 2046 and is output at write address 2047. If a write reset is performed on address 2047 at this time, the write address becomes 0 and $\overline{WDEC}$ is output.
  The same operation is performed in other modes.
- In the reset cycle, the input levels of $\overline{WRES}$, $\overline{RRES}$, $\overline{RES}$ are raised to satisfy t_{REH}, and are fixed high until t_{REPH} in the next pre-reset cycle is satisfied. The rise timings of the reset signals ($\overline{RES}$, $\overline{WRES}$, $\overline{RRES}$) are optionals provided that the t_{REPS} specification is satisfied. The timings at which $\overline{RES}$, $\overline{WRES}$, and $\overline{RRES}$ fall after pre-reset are also optional, provided that the t_{REPH} and t_{RES} specifications are satisfied.



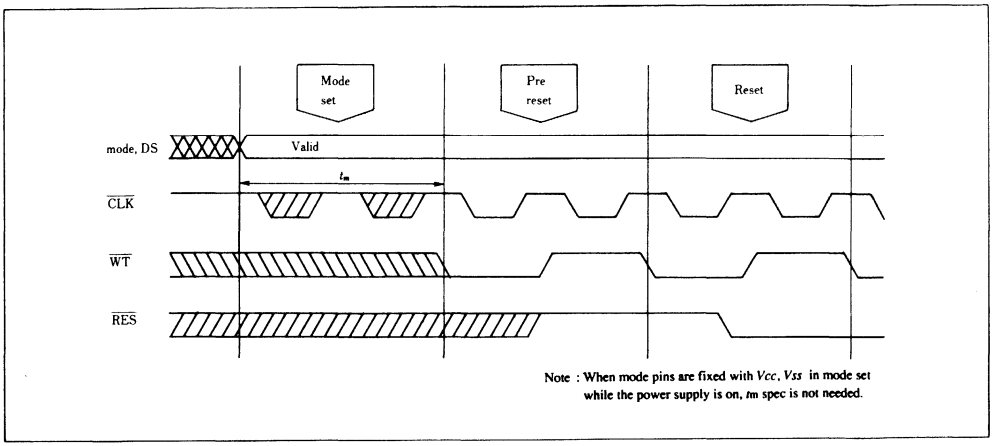
- Hitachi recommends that t_m (time between mode set and the first cycle (Pre-reset)) should be kept for 2 cycle time (56ns / 68ns / 90ns) or more while the power supply is on.

(1) TBCE, TBC, DSC and Delay Line Mode



Note: When mode pins are fixed with Vcc, Vss in mode set while the power supply is on, t_m spec is not needed.

(2) 1H / 2H Delay Mode



Decode Signal

When internal address counter reaches the specified address as shown below, decode outputs become low.

Mode	Pin No.	Pin Name	Internal Address counter	Timing of the Output Signal	Operation
TBC	13	$\overline{WDEC}$	Write 2047	After Write 2047	Completion of Writing on all bits is detected.
	26	$\overline{RDEC}$	Read 2047	Output of 2046	Completion of Reading from all bits is detected.
1H/2H	13	$\overline{DEC1}$	Read 900 (2H)	Output of 900 (1H)	By inputting this signal to pin #3, 901/1802-bit delay output is obtained.
	26	$\overline{DEC2}$	Read 909 (2H)	Output of 909 (1H)	By inputting this signal to pin #3, 910/1820-bit delay output is obtained.
Delay line	13	$\overline{DEC1}$	Read 900	Output of 899	By inputting this signal to pin #3, 901-bit delay output is obtained.
			Read 1810	Output of 1809	By inputting this signal to pin #3 after the frequency of $\overline{DEC1}$ is devided into two, 1811-bit delay output is obtained.
	26	$\overline{DEC2}$	Read 909	Output of 908	By inputting this signal to pin #3, 910-bit delay output is obtained.
			Read 1819	Output of 1818	By inputting this signal to pin #3 after the frequency of $\overline{DEC2}$ is devided into two, 1820-bit delay output is obtained.
	16	$\overline{DEC3}$	Read 1134	Output of 1133	By inputting this signal to pin #3, 1135-bit delay output is obtained.
	15	$\overline{DEC4}$	Read 1125	Output of 1124	By inputting this signal to pin #3, 1126-bit delay output is obtained.

Note) When counter is reset by Reset Signal ($\overline{RRES}$, $\overline{RES}$, $\overline{WRES}$), address becomes 0.

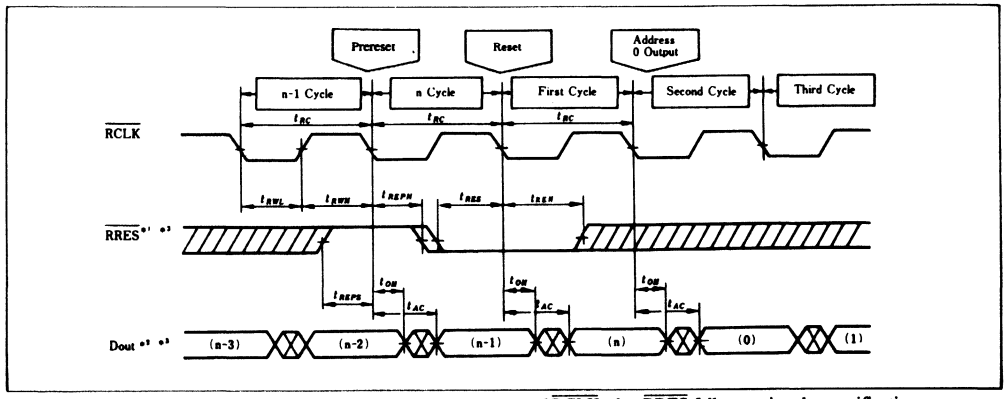
Write-inhibit Function

When internal address counter is as follows, writing is inhibited automatically for the next cycle. The write-inhibit function is cancelled by reset through $\overline{WRES}$ or $\overline{RES}$.

Mode	Write-inhibit Function (internal counter address)
TBCE	Write-inhibit after address 2047
DSC	Write-inhibit after address 1023 x 2
TBC	No function
1H/2H	Write-inhibit after address 1023
D	No function

Note) When address counter is reset by $\overline{WRES}$ or $\overline{RES}$, address becomes 0.

Read Reset Cycle (TBCE, TBC Modes)

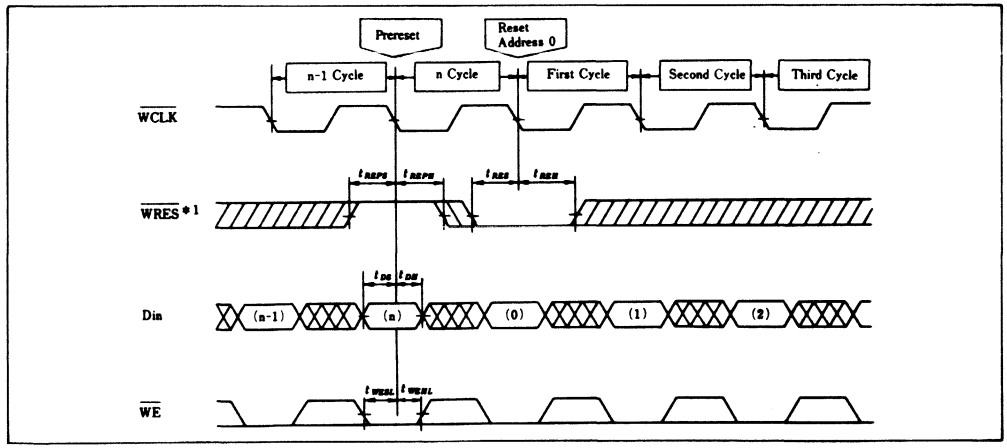


Notes) *1. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS}, and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meeet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

*2. Output is from the read address of the previous cycle.

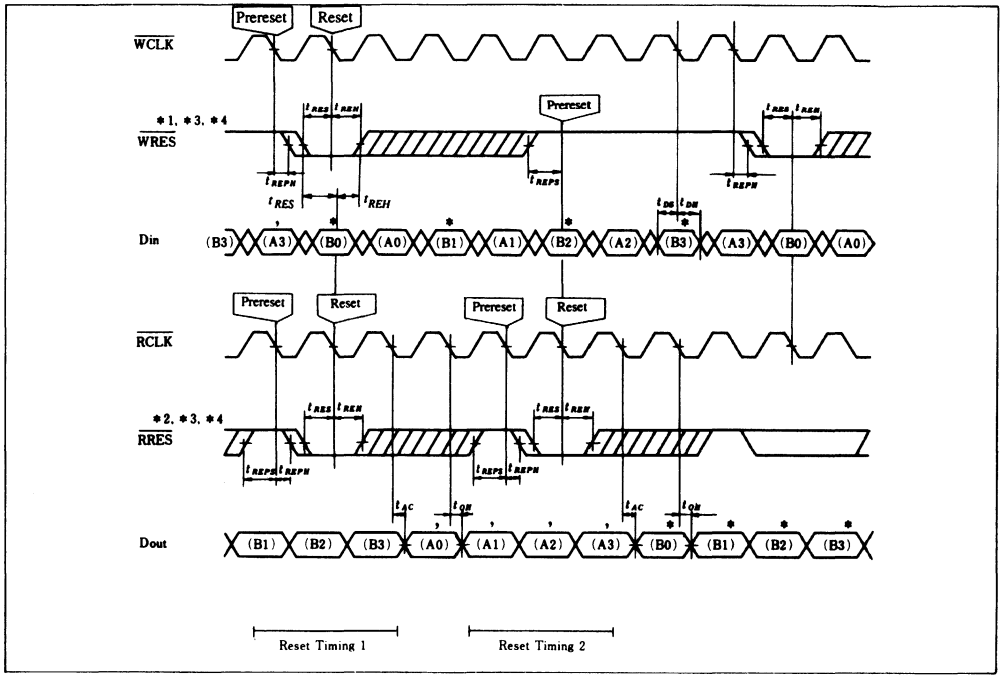
*3. When $\overline{RRES}$ is fixed high, the data at the read address counter is reset after the data of address 2047 is output, and the same operation restarts.

Write Reset Cycle (TBCE, TBC Modes)



Note) The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

Reset Cycle (DSC Mode)



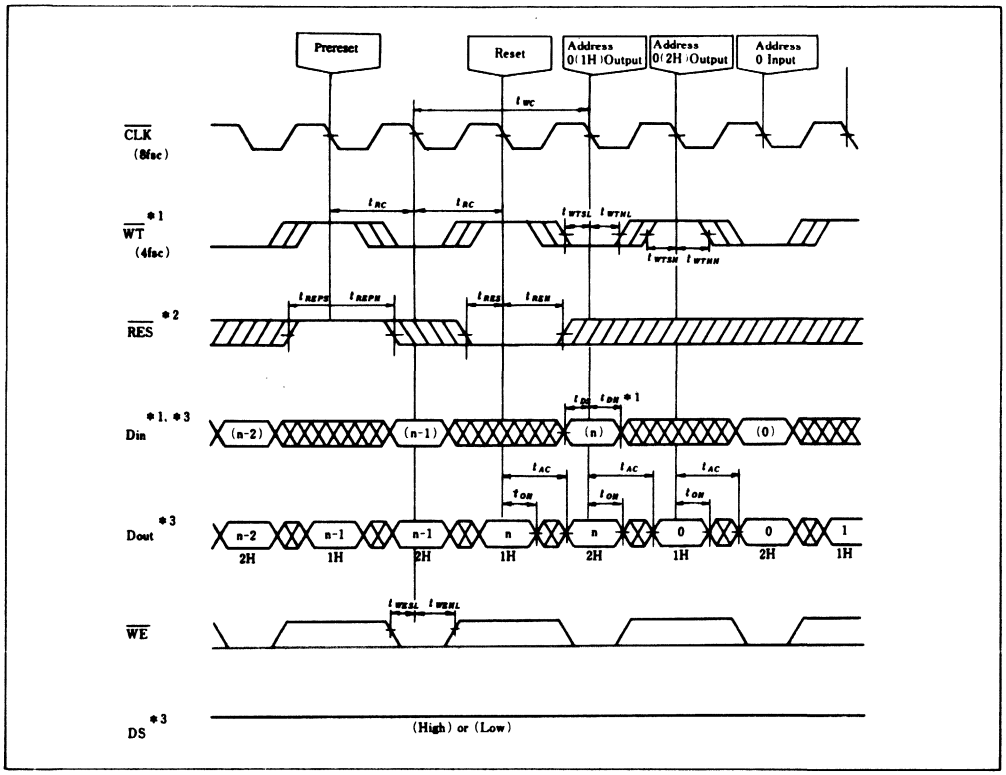
Notes) *1. The write address counter is reset at the first falling edge of $\overline{WCLK}$ after $\overline{WRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and is not reset at the next falling edge of $\overline{WCLK}$ even if $\overline{WRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH} cannot meet the specifications, the reset operation is not guaranteed.

*2. The read address counter is reset at the first falling edge of $\overline{RCLK}$ after $\overline{RRES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{RCLK}$ even if $\overline{RRES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS} and t_{REPH} cannot meet the specifications, reset operation is not guaranteed.

*3. When t_{REPH}, t_{RES}, t_{REH}, ($\overline{WRES}$ to $\overline{WCLK}$), t_{RES}, t_{REH}, ($\overline{WRES}$ to $\overline{RCLK}$) or t_{REPS}, t_{REPH}, t_{RES}, t_{REH} ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the output of video signal A is not guaranteed, (Reset Timing I).

*4. When t_{REPS}, ($\overline{WRES}$ to $\overline{RCLK}$), or t_{RES}, t_{REH}, t_{REPS}, t_{REPH}, ($\overline{PRES}$ to $\overline{RCLK}$) cannot meet the specifications, the interpolation signal B is not guaranteed. (Reset Timing II).

Reset Cycle (1H/2H Mode)

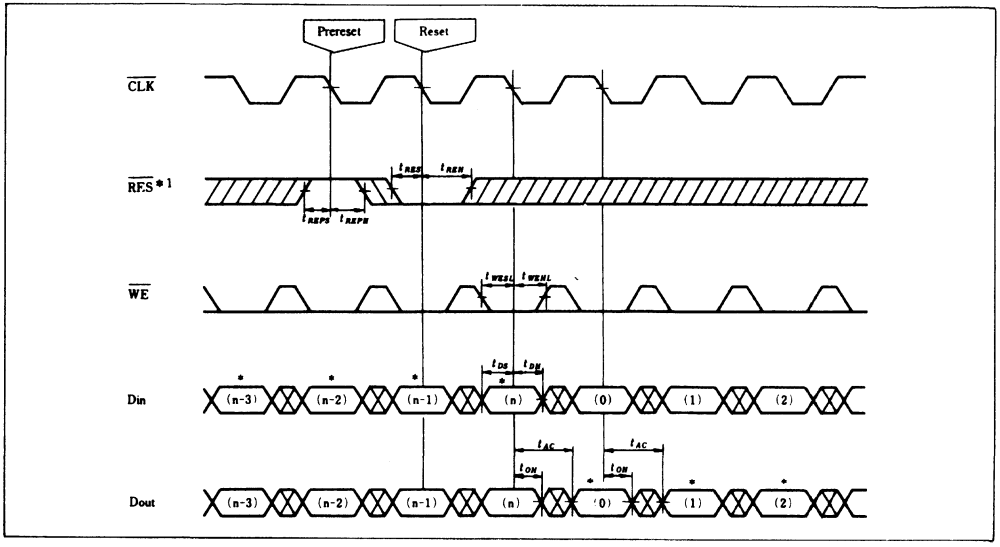


Notes) *1. $\overline{WT}$ is the input during half cycle of $\overline{CLK}$, meeting the specifications of t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH}. Data is written when $\overline{WT}$ is low. Reset is possible when $\overline{WT}$ is high.

*2. Read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH}, cannot meet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

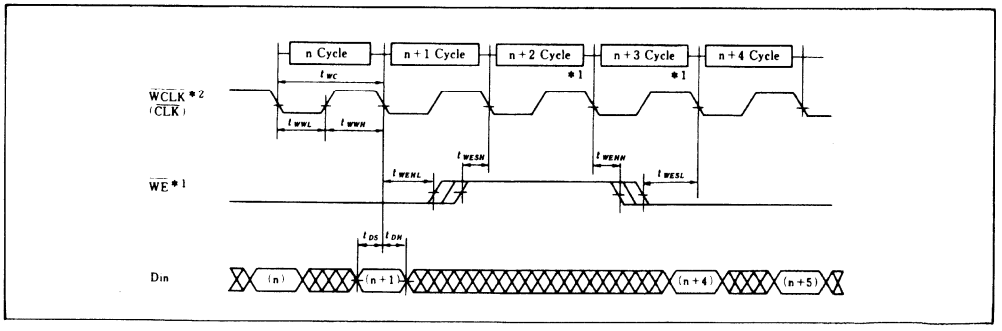
*3. When DS is fixed high, 1H output data is delayed by n bits and 2H output data is delayed by 2n bits where 2n is the reset cycle of $\overline{RES}$.
When DS is fixed low, 1H output data is delayed by n-5 bits and 2H output data is delayed by 2n-5 bits.

Reset Cycle (D Mode)



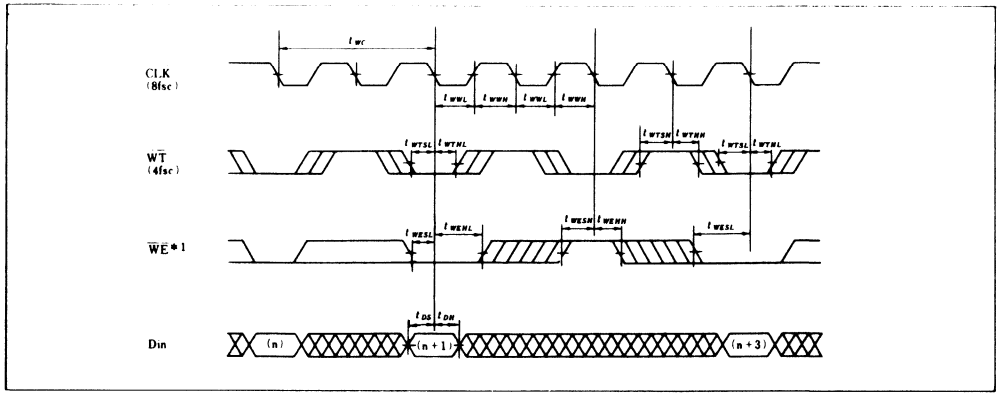
Note) *1. The read address counter is reset at the first falling edge of $\overline{CLK}$ after $\overline{RES}$ falls, meeting the specifications of t_{REPS} and t_{REPH}, and it is not reset at the next falling edge of $\overline{CLK}$ even if $\overline{RES}$ is kept low.
When t_{RES}, t_{REH}, t_{REPS}, and t_{REPH}, cannot meet the specifications, the reset operation is not guaranteed.
In reset operation, both prereset and reset are required.

Write Enable (TBCE, DSC, TBC, D Modes)



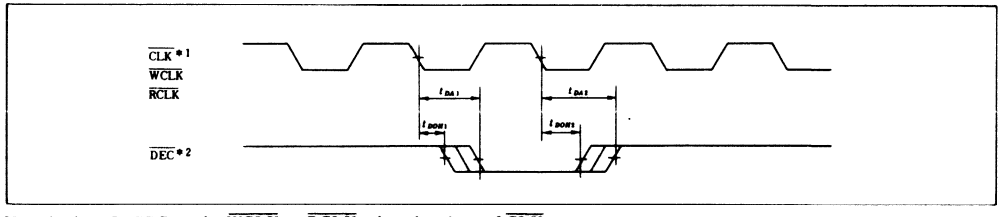
Notes) *1. When t_{WEHL}, t_{WESH}, t_{WEHH}, and t_{WESL} cannot meet this specifications, the write enable operation is not guaranteed.
*2. In the delay line mode, $\overline{CLK}$ takes the place of $\overline{WCLK}$.

Write Enable (1H/2H Mode)



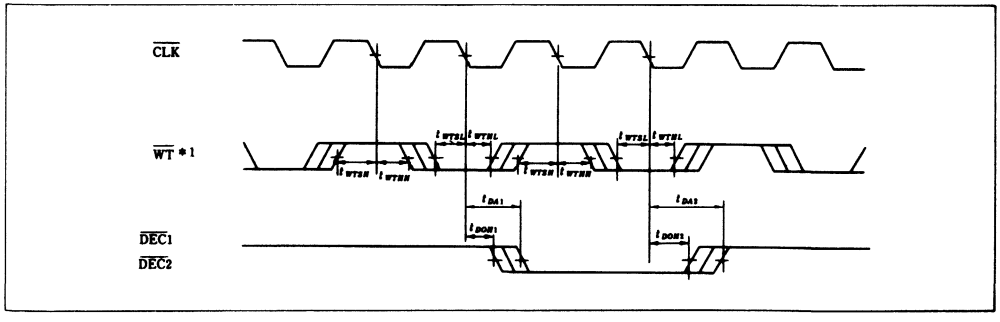
Note) *1. When t_{WTSL}, t_{WTHL}, t_{WEHL}, and t_{WEHH} cannot meet the specifications, the write enable operation is not guaranteed.

Decode Output (TBC, D Modes)



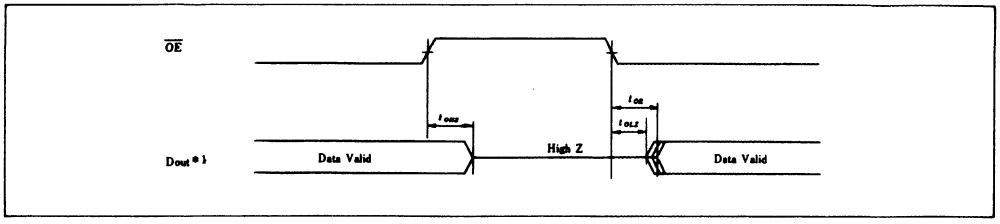
Notes) *1. In TBC mode, $\overline{WCLK}$ or $\overline{RCLK}$ takes the place of $\overline{CLK}$.
*2. $\overline{DEC}$ is $\overline{WDEC}$ or $\overline{RDEC}$ in TBC, $\overline{DEC1}$, $\overline{DEC2}$, $\overline{DEC3}$ or $\overline{DEC4}$ in D mode.

Decode Output (1H/2H Mode)



Note) *1. When t_{WTSL}, t_{WTHL}, t_{WTSH}, and t_{WTHH} cannot meet the specifications, the decode output operation is not guaranteed.

Output Enable (All Modes)



Note) *1. Transition of t_{OHZ} and t_{WLZ} is measured ±200 mV from steady state voltage with Output Load B. This parameter is sampled and not 100% tested.

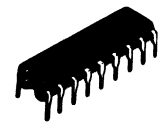
HM53051 Series

262144-word x 4-bit Frame Memory

HM53051P is a 262,144-word x 4-bit frame memory, using the most advanced 1.3μm CMOS processes. It performs serial access by an internal address generator.

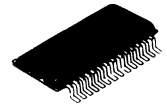
It offers a high-speed cycle time of 34ns, 45ns or 60ns (min). As input data and output data can be written or read in any cycle, synchronized with a system clock, and the delay between data read/write operations is freely settable. Y/C separation and frozen pictures can be realized easily in 8fsc NTSC digital TV or VCR systems. Also, it enables random access in 32-word x 4-bit data block. With this function, picture in picture or a multiplexed picture can be displayed with ease.

HM53051P Series



(DP-18C)

HM53051FP Series



(FP-28DA)

Features

- 262,144-word x 4-bit serial access memory
- Organized with dual ports
  - Serial input x 4-bit
  - Serial output x 4-bit
- High Speed
  - Read/Write Cycle Time: 34ns/45ns/60ns (min)
  - Access Time: 30ns/35ns/40ns (max)
- Semi-synchronous Read/Write Cycle
- Low Power
  - Active : HM53051-34 225 mW(typ)
  - HM53051-45/60 200 mW(typ)
- Random Access in 32-word x 4-bit blocks
- External Refresh Control is unnecessary

Ordering Information

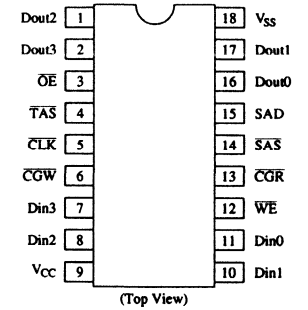
Type No.	Access Time	Package
HM53051P-34 HM53051P-45 HM53051P-60	34ns 45ns 60ns	300-mil 18-pin Plastic DIP
HM53051FP-34 HM53051FP-45 HM53051FP-60	34ns 45ns 60ns	28-pin Plastic SOP

Pin Description

Pin Name	Function
Din	Data Input
Dout	Data Output
$\overline{OE}$	Output Enable
$\overline{TAS}$	Transfer Address Strobe
$\overline{CLK}$	System Clock
$\overline{CGW}$	Clock Gate (Write)
$\overline{CGR}$	Clock Gate (Read)
SAD	Serial Address
$\overline{SAS}$	Serial Address Strobe
$\overline{WE}$	Write Enable

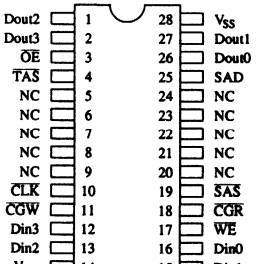
Pin Arrangement

HM53051P Series



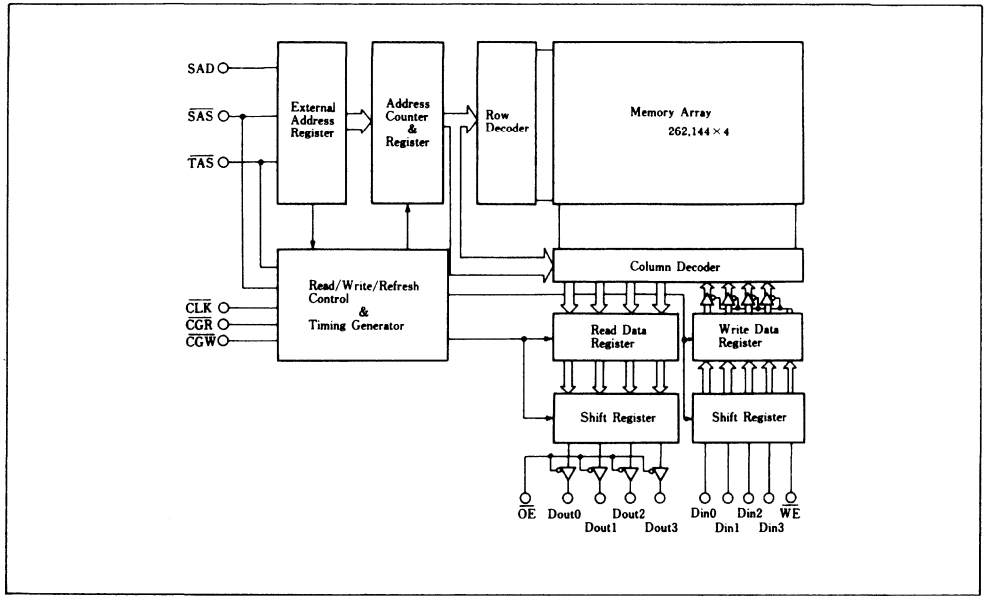
(Top View)

HM53051FP Series



(Top View)

Block Diagram



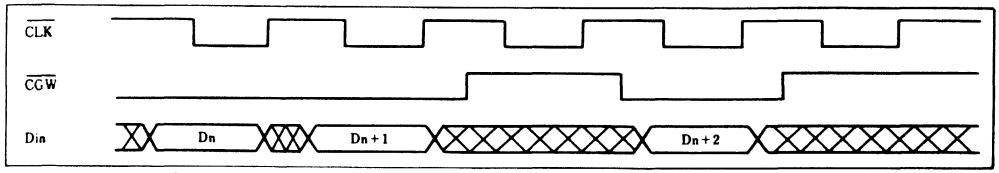
Functional Description

Serial access memory with I/O separated

Read cycle and write cycle of HM53051 can be operated independently synchronized with a system clock. It realizes time compression or expansion for picture in picture in digital TV, for example.

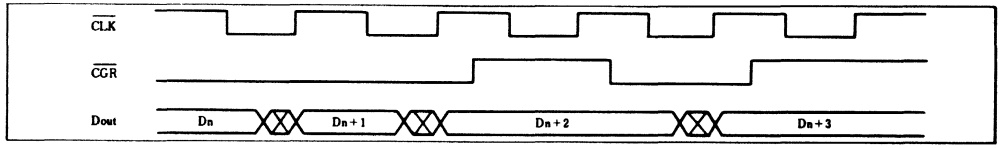
- **Write cycle by $\overline{CGW}$**

Write data are taken in at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGW}$ is low. If $\overline{CGW}$ is high, HM53051 does not enter write cycle (cycle time is defined by system clock cycle time). Time is compressed easily with $\overline{CGW}$.



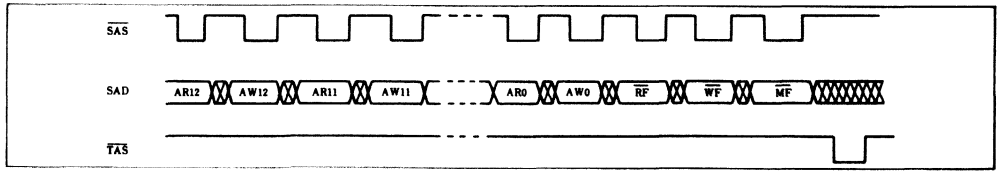
- **Read Cycle by $\overline{CGR}$**

Read data is output at the falling edge of the system clock $\overline{CLK}$ when $\overline{CGR}$ is low. If $\overline{CGR}$ is high, HM53051 does not enter read cycle (cycle time is defined by system clock time). Time is expanded is realized easily with $\overline{CGR}$.



Random Access

The HM53051 is also capable of random access by serial address input, SAD. Random access by the unit of 32-word x 4-bit is performed, when $\overline{TAS}$ is low after read address (AR0 – AR12), write address (AW0 – AW12) and mode setting flags, $\overline{RF}$ (Read Flag), $\overline{WF}$ (Write Flag) and $\overline{MF}$ (Mode Flag) are read into by $\overline{SAD}$ with synchronous $\overline{SAS}$. In order to output data continuously, the address specified by $\overline{SAD}$ increments automatically.



Mode Programming

Operation mode in HM53051 is programmed by the combination of SAD 5-bit.

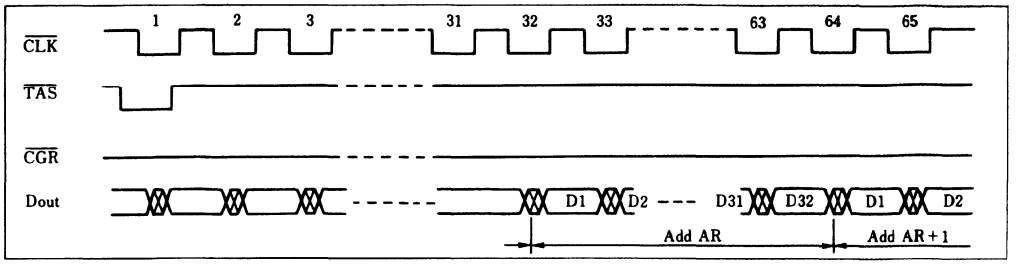
$\overline{MF}$	$\overline{WF}$	$\overline{RF}$	AW0	AR0	Mode
0	0	0	x	x	Write/read address asynchronous transfer
0	0	1	x	x	Write address asynchronous transfer
0	1	0	x	x	Read address asynchronous transfer
0	1	1	x	x	–
1	0	0	x	x	Write/read address synchronous transfer
1	0	1	x	x	Write address synchronous transfer
1	1	0	x	x	Read address synchronous transfer
1	1	1	1	1	System reset
1	1	1	0	0	
1	1	1	0	1	Inhibit
1	1	1	1	0	

Note) x means Don't care.

Read/Write Address Asynchronous Transfer Mode

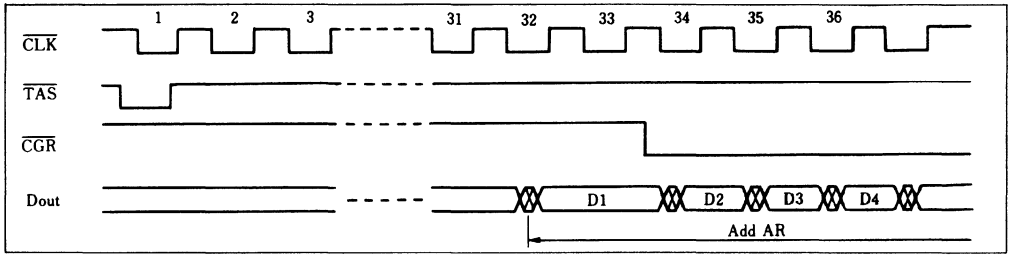
- **Read address asynchronous transfer mode**

(1) Read address asynchronous transfer mode (1) ($\overline{CGR}$: Low)



Note) The data block at read address AR, specified by SAD, is output starting from the 32-nd system clock after the of $\overline{TAS}$.

(2) Read address asynchronous transfer mode (2) ($\overline{CGR}$: High)

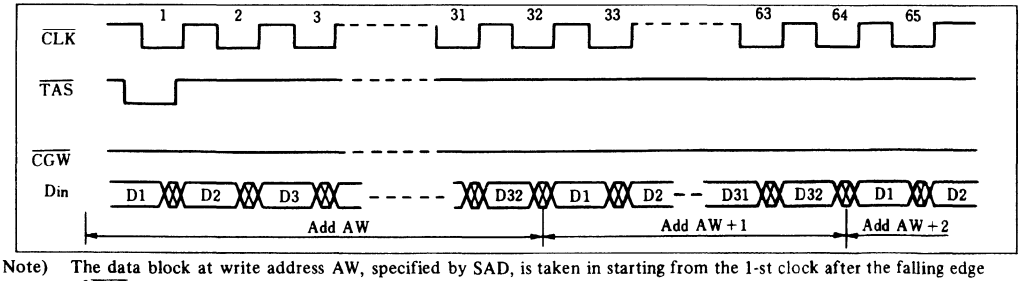


Notes) *1. The data block at read address AR, specified by SAD, is output starting from the 32-nd system clock after the falling of $\overline{TAS}$.

*2. If $\overline{CGR}$ is turned to low after 33-rd clock from the falling edge of $\overline{TAS}$, the data at read address AR (D2, D3, D4 . . .) is output with synchronous $\overline{CLK}$ while $\overline{CGR}$ is low.

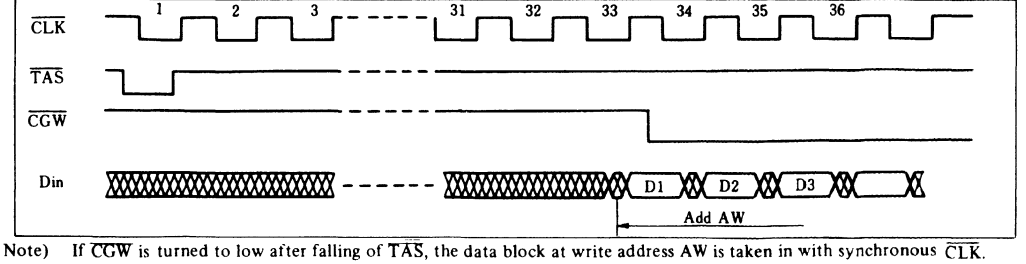
- **Write address asynchronous transfer mode**

(1) Write address asynchronous transfer mode (1) ($\overline{CGW}$: Low)



Note) The data block at write address AW, specified by SAD, is taken in starting from the 1-st clock after the falling edge of $\overline{TAS}$.

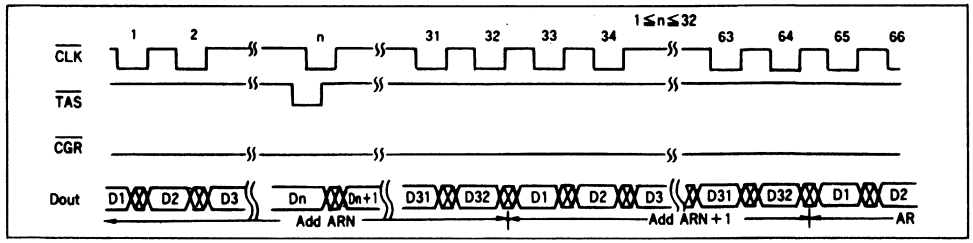
(2) Write address asynchronous transfer mode (2) ($\overline{CGW}$; High)



Note) If $\overline{CGW}$ is turned to low after falling of $\overline{TAS}$, the data block at write address AW is taken in with synchronous $\overline{CLK}$.

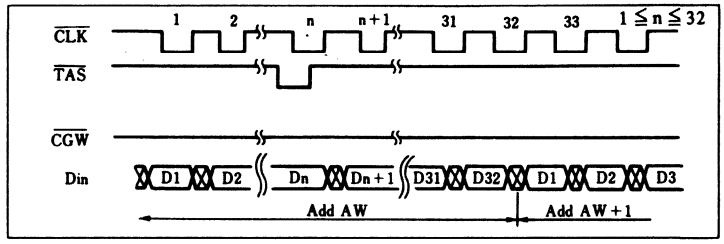
Read/Write Address Synchronous Transfer Mode

- Read address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block at read address AR, specified by SAD, is output after the data block at the present read address ARN, and the next address ARN+1 is put out.

- Write address synchronous transfer mode



Note) When $\overline{TAS}$ turns to low, the data block being written is taken into write address AW.

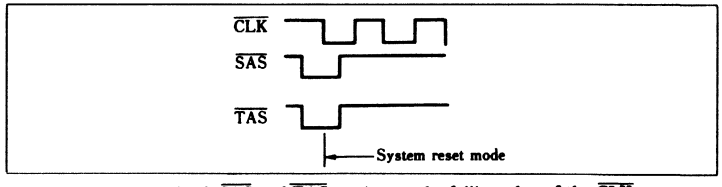
System Reset Mode

System reset mode is the same as read/write address asynchronous transfer mode except that read/write address are reset to 0.

- System reset by SAD

Note) System reset mode starts when $\overline{MF}$, $\overline{WF}$, $\overline{RF}$, AW0, and AR0 are all high.

- System reset by $\overline{SAS}$ and $\overline{TAS}$



Note) System reset mode starts when both $\overline{SAS}$ and $\overline{TAS}$ are low at the falling edge of the $\overline{CLK}$.

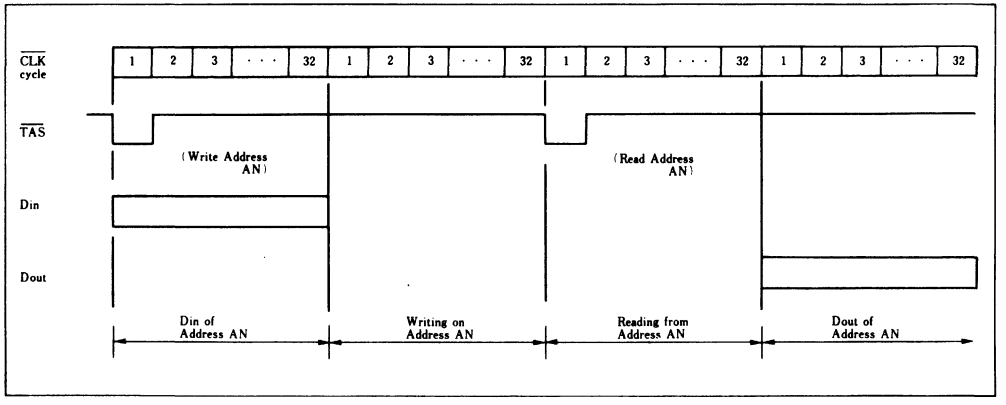
- 1 field delay

Note) Field-delayed data is output, when $\overline{CGR}$ and $\overline{CGW}$ turn to high before the system reset at the beginning of every field, and turn to low simultaneously after the 33rd clock from the system reset.

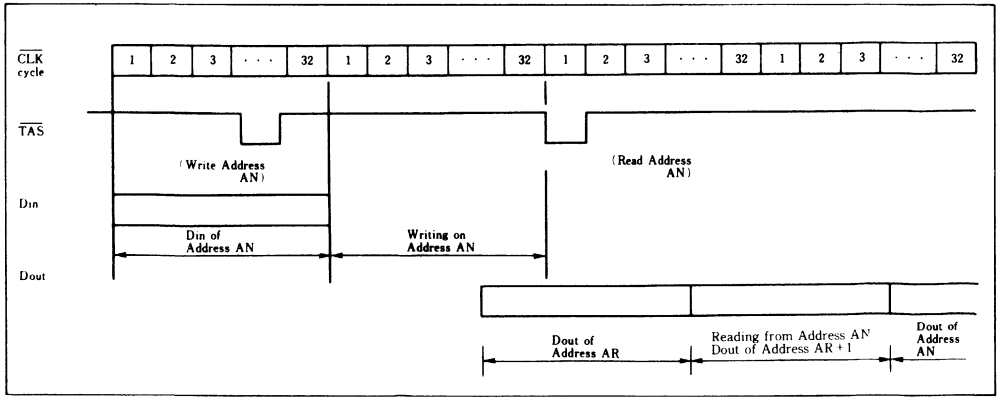
Notes on Using HM53051

- Input/output data of 32 words is not written or read in read/write address asynchronous transfer mode or during system reset. The data is written or read out in blocks of 32-word x 4-bit. Input data of less than 32 words is not written in write address asynchronous transfer mode or during system reset. When asynchronous read address transfer mode or system reset mode is activated, output from the current data block will continue. When output data from the current data block is finished, the next data block is not read out if it has less than 32 words.
- Input data is not read out immediately. The data (32 word x 4-bit) is written into the memory array in the next 32 cycles after it is taken in. The data can be read out only after writing to the memory array is completed. If read address transfer mode is programmed after the 33 word clock from on input data block, new data can be read out. If this mode is programmed before the 33 word clock, new data or old data is output.

(1) Read/write address asynchronous transfer mode



(2) Read/write address synchronous transfer mode

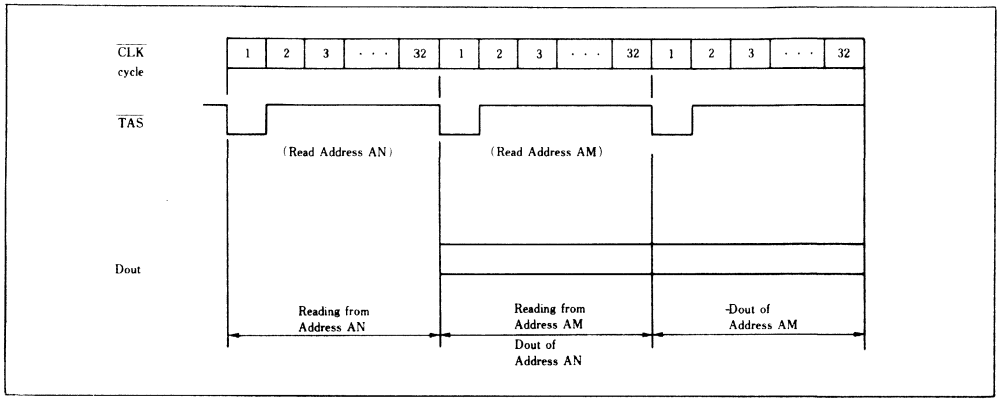


- **Mode programming**

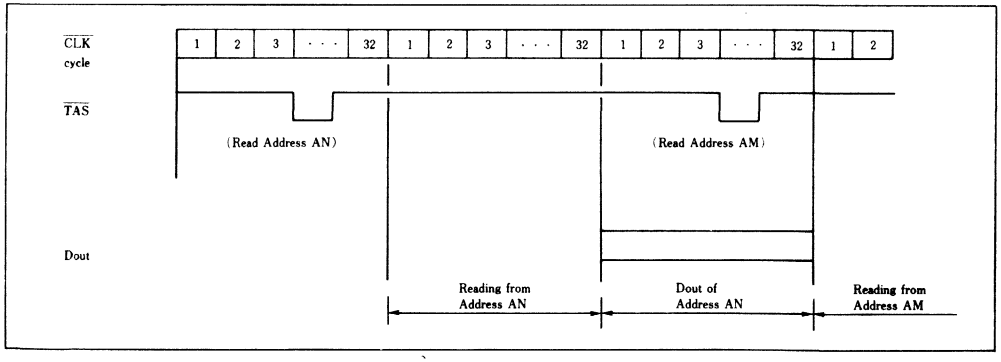
  Do not reprogram read address transfer mode before a read operation of the previous read address transfer mode or system reset mode is completed. If it is reprogrammed during a read operation, address becomes invalid, and the device may malfunction.

  Do not reprogram write address transfer mode or system reset mode before a write operation of the previous write address transfer mode or system reset mode is completed. If it is reprogrammed during a write operation, address become invalid, and the device may malfunction.

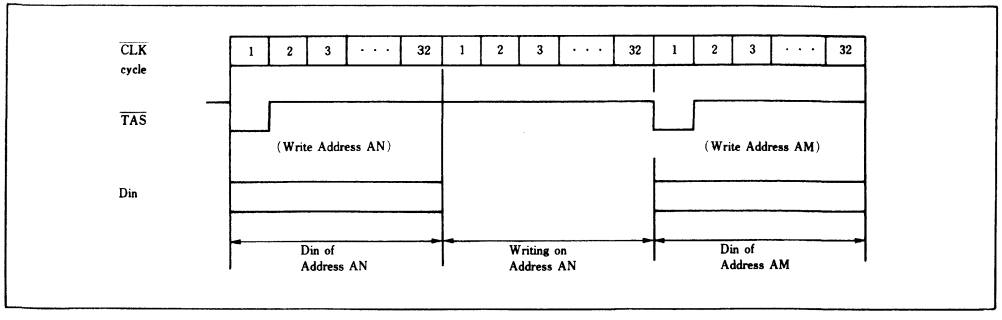
(1) Read address asynchronous transfer mode



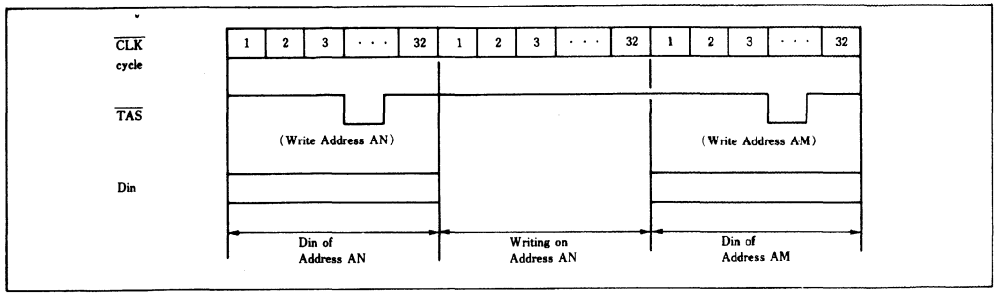
(2) Read address synchronous transfer mode



(3) Write address asynchronous transfer mode



(4) Write address synchronous transfer mode



- Addresses must be set by read and write address asynchronous transfer or system reset 100μs after power on. Before an address can be set, 32 $\overline{CLK}$ initialization cycles or more are required.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature (under bias)	Tbias	−10 to +85	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.7	—	6.5	V
($\overline{CLK}$, $\overline{SAS}$)	V_{IL}	−0.5*1	—	0.8	V
Input Voltage	V_{IH}	2.4	—	6.5	V
(All pins except $\overline{CLK}$ and $\overline{SAS}$)	V_{IL}	−0.5*1	—	0.8	V

Note) *1. −3.0V for pulse width ≦ 10ns.

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	HM53051-34			HM53051-45/60			Unit
			min	typ	max	min	typ	max	
Operating Power Supply Current	I_{CC}	Min. cycle Iout=0 mA	—	45	60	—	40	60	mA
Input Leakage Current	I_{LI}	VCC=5.5V Vin=Vss to Vcc	−10	—	10	−10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$=VIH Vout=Vss to Vcc	−10	—	10	−10	—	10	μA
Output Voltage	V_{OL}	I_{OL}=4.2mA	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH}=−2 mA	2.4	—	—	2.4	—	—	V

Capacitance (Ta = 25°C, f = 1.0 MHz)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	Cin	Vin = 0 V	–	–	5	pF
Output Capacitance	Cout	Vout = 0 V	–	–	7	pF

Note) This parameter is sampled and not 100% tested.

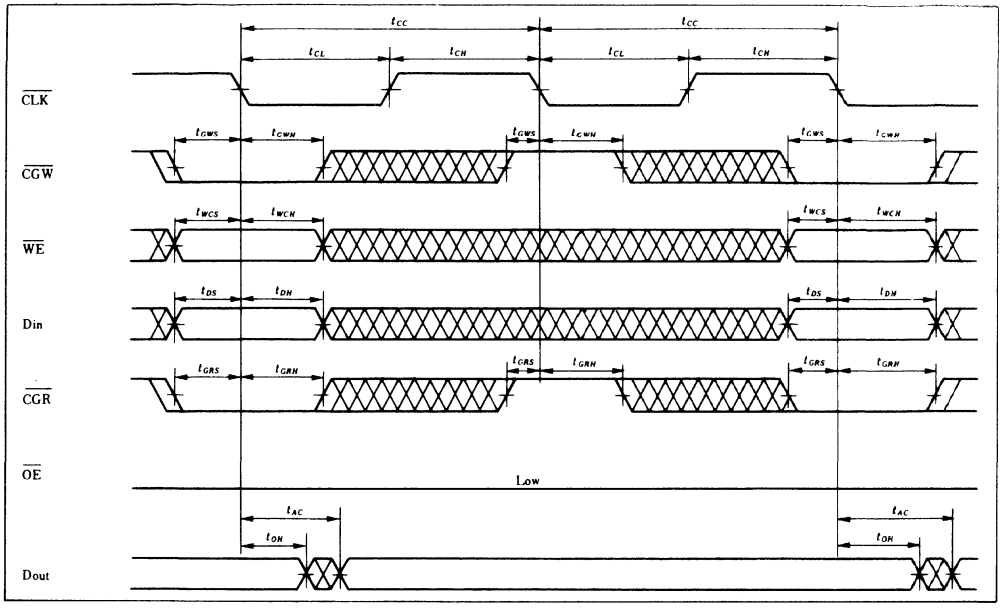
AC Characteristics (V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

AC Test Conditions

- Input and output timing reference levels: 1.5 V
- Input pulse levels: V_{SS} to 3 V
- Input rise and fall times: 5 ns
- Output Load: 2 TTL + 50 pF
  (Including scope and jig)

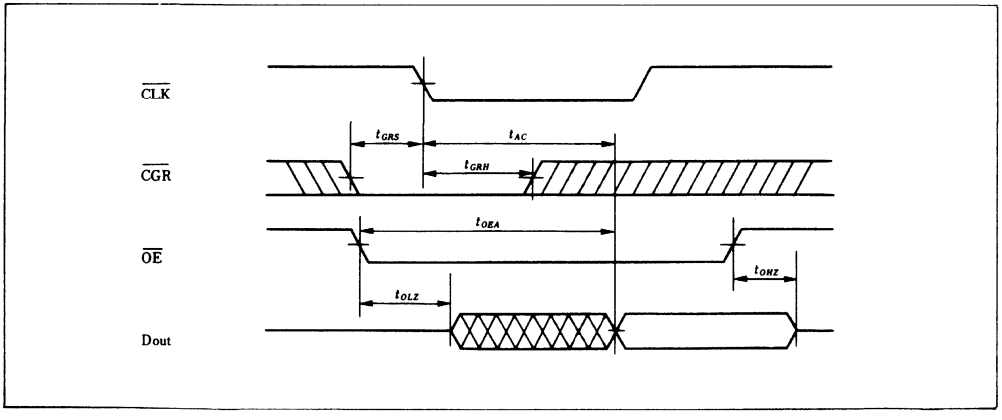
Parameter	Symbol	HM53051-34		HM53051-45		HM53051-60		Unit
		min	max	min	max	min	max	
System Clock Cycle Time	t_{CC}	34	300	45	300	60	300	ns
$\overline{CLK}$ Pulse Width	t_{CL}	15	—	15	—	15	—	ns
	t_{CH}	15	—	15	—	15	—	ns
Access Time from $\overline{CLK}$	t_{AC}	—	30	—	35	—	40	ns
Output Hold Time	t_{OH}	5	—	5	—	8	—	ns
Output Enable Access Time	t_{OEA}	—	25	—	25	—	30	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	5	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	20	0	20	0	20	ns
$\overline{CGR}$ Setup Time	t_{GRS}	15	—	15	—	15	—	ns
$\overline{CGR}$ Hold Time	t_{GRH}	5	—	5	—	5	—	ns
$\overline{CGW}$ Setup Time	t_{GWS}	15	—	15	—	15	—	ns
$\overline{CGW}$ Hold Time	t_{GWH}	5	—	5	—	5	—	ns
Write Command Setup Time	t_{WCS}	15	—	15	—	15	—	ns
Write Command Hold Time	t_{WCH}	5	—	5	—	5	—	ns
Data Input Setup Time	t_{DS}	15	—	15	—	15	—	ns
Data Input Hold Time	t_{DH}	5	—	5	—	5	—	ns
$\overline{SAS}$ Cycle Time	t_{SC}	34	—	45	—	60	—	ns
$\overline{SAS}$ Pulse Width	t_{SL}	15	—	15	—	15	—	ns
	t_{SH}	15	—	15	—	15	—	ns
Serial Address Setup Time	t_{SAS}	15	—	15	—	15	—	ns
Serial Address Hold Time	t_{SAH}	5	—	5	—	5	—	ns
$\overline{SAS}$ Setup Time during Mode Programming	t_{SSH}	15	—	15	—	15	—	ns
$\overline{SAS}$ Hold Time during Mode Programming	t_{SHH}	5	—	5	—	5	—	ns
$\overline{TAS}$ Setup Time	t_{TS}	15	—	15	—	15	—	ns
$\overline{TAS}$ Hold Time	t_{TH}	5	—	5	—	5	—	ns
$\overline{SAS}$ Setup Time during System Reset by $\overline{SAS/TAS}$	t_{SSL}	15	—	15	—	15	—	ns
$\overline{SAS}$ Hold Time during System Reset by $\overline{SAS/TAS}$	t_{SHL}	5	—	5	—	5	—	ns

Read/Write Cycle



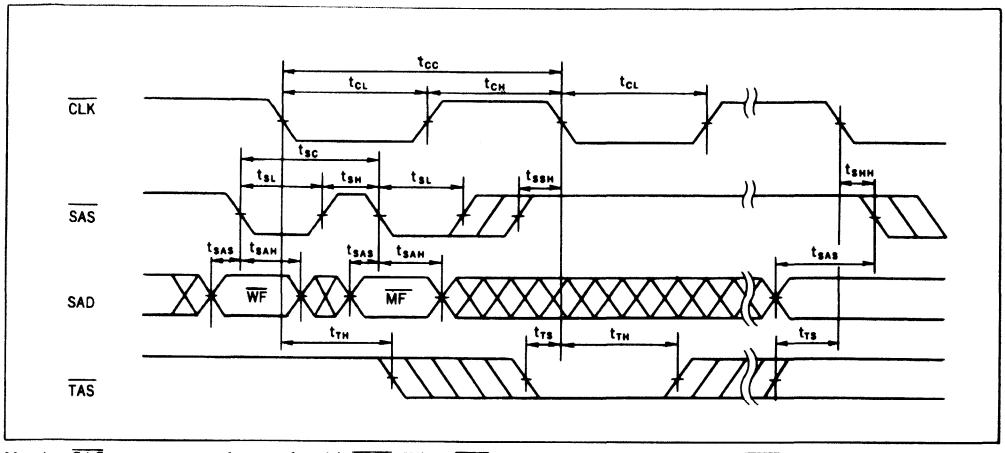
Notes) *1. Write Cycle starts when $\overline{CGW}$ is low and $\overline{WE}$ is low. Data are not written when $\overline{WE}$ is high. Time-compression mode is realized by controlling $\overline{CGW}$.
*2. Read cycle starts when $\overline{CGR}$ is low. Time-expansion mode is realized by controlling $\overline{CGR}$.

Read Cycle ($\overline{OE}$ control)



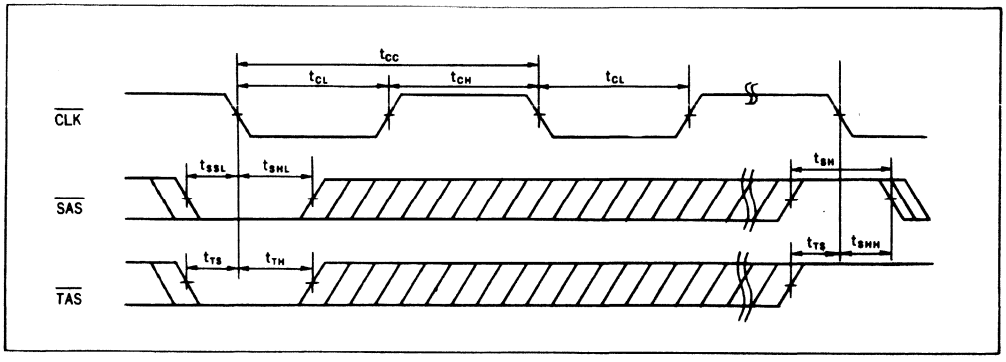
Notes) *1. t_{OHZ} is defined by the time at which the output achieves the open circuit condition.
*2. t_{OLZ} and t_{OHZ} are sampled and not 100% tested.

Mode Selection



Note) $\overline{SAS}$ operates asynchronously with $\overline{CLK}$. When $\overline{TAS}$ is low at the falling edge of the $\overline{CLK}$, the address transfer cycle starts. $\overline{SAS}$ should be high during the address transfer cycle.

$\overline{SAS}$, $\overline{TAS}$ Reset Mode



Note) The mode which was selected by SAD before $\overline{SAS}$ and $\overline{TAS}$ reset, if $\overline{SAS}$ and $\overline{TAS}$ are reset, should be changed because SAD is newly taken into by SAS. The mode should be reselected by SAD after $\overline{SAS}$ and $\overline{TAS}$ reset.

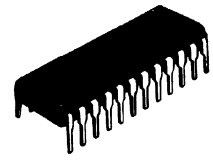
HM53461 Series

65,536-word x 4-bit Multiport CMOS Video RAM

The HM53461 is a 262, 144-bit multiport memory equipped with a 64k-word x 4-bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

Utilizing the Hitachi 2μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

HM53461P Series



(DP-24A)

HM53461ZP Series

(ZP-24)

HM53461JP Series

(CP-24D)

■ FEATURES

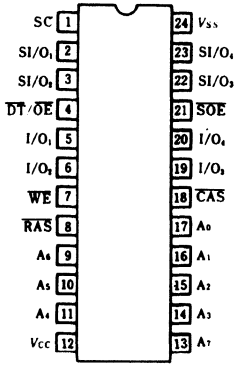
- Multiport organization
  (RAM; 64k-word x 4-bit and SAM; 256 word x 4-bit)
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V (±10%)
- Low power Active RAM; 380mW max.
  SAM; 220mW max.
  Standby 40mW max.
- Access Time RAM; 100ns/120ns/150ns
  SAM; 40ns/40ns/60ns
- Cycle Time Random read or write cycle time (RAM)
  190ns/220ns/260ns
  Serial read or write cycle time (SAM)
  40ns/40ns/60ns
- TTL compatible
- 256 refresh cycles 4ms
- Refresh function $\overline{RAS}$ – only refresh
  $\overline{CAS}$ – before – $\overline{RAS}$ refresh
  Hidden refresh
- Data transfer operation (RAM⇄SAM)
- Fast serial access operation asynchronized with RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM53461P-10 HM53461P-12 HM53461P-15	100ns 120ns 150ns	400 mil 24-pin Plastic DIP
HM53461ZP-10 HM53461ZP-12 HM53461ZP-15	100ns 120ns 150ns	24 pin Plastic ZIP
HM53461JP-10 HM53461JP-12 HM53461JP-15	100ns 120ns 150ns	24 pin Plastic SOJ

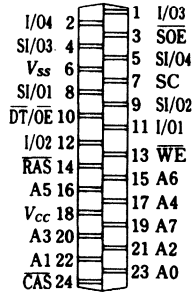
■ PIN ARRANGEMENT

● HM53461P Series
HM53461JP Series



(Top View)

● HM53461ZP Series

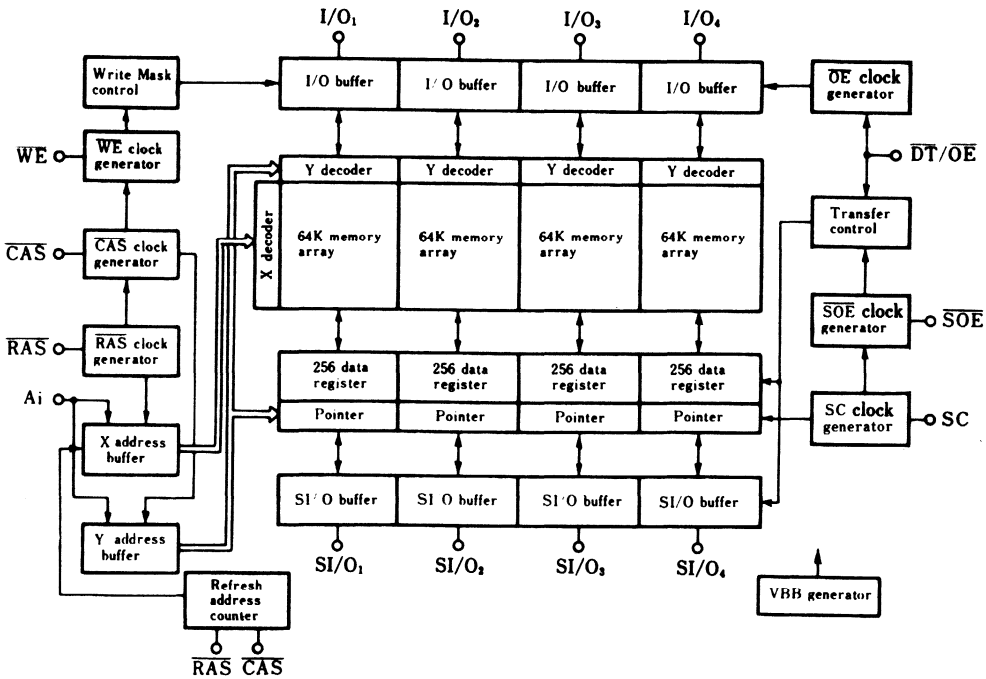


(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A0 – A7	Address Inputs
I/O1 – I/O4	RAM Port Data Input/Output
SI/O1 – SI/O4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Power supply voltage relative to V_{SS} . . . . . -0.5V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	-0.5*2	–	0.8	V

Notes: 1. All voltages referenced to V_{SS}.
2. -3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)

RAM PORT	Symbol	SAM PORT		HM53461 -10	HM53461 -12	HM53461 -15	Unit
		Standby	Active				
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	O	X	70	60	50	mA
	I_{CC7}	X	O	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	O	X	7	7	7	mA
	I_{CC8}	X	O	40	40	30	mA
$\overline{RAS}$ only refresh current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min.	I_{CC3}	O	X	60	50	40	mA
	I_{CC9}	X	O	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	I_{CC4}	O	X	50	40	35	mA
	I_{CC10}	X	O	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	O	X	60	50	40	mA
	I_{CC11}	X	O	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	O	X	75	65	55	mA
	I_{CC12}	X	O	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{LI}	-10	10	μA
Output leakage	I_{LO}	-10	10	μA
Output high voltage I_{OH}=-2mA	V_{OH}	2.4	–	V
Output low voltage I_{OL}=4.2mA	V_{OL}	–	0.4	V

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	CI1	–	5	pF
Clocks	CI2	–	5	pF
I/O, SI/O	$C_{I/O}$	–	7	pF

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)[1), 10), 11)]

Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	–	300	–	355	–	ns	
Page Mode Cycle Time	t_{PC}	70	–	85	–	105	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	25	–	30	–	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	8
$\overline{CAS}$ Setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	25	–	30	–	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	–	15	–	20	–	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	–	0	–	0	–	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	–	40	–	45	–	ns	
Serial Clock Cycle Time	t_{SCC}	40	–	40	–	60	–	ns	
Access Time from SC	t_{SCA}	–	40	–	40	–	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	–	25	–	30	–	40	ns	10
SC Pulse Width	t_{SC}	10	–	10	–	10	–	ns	

(to be continued)

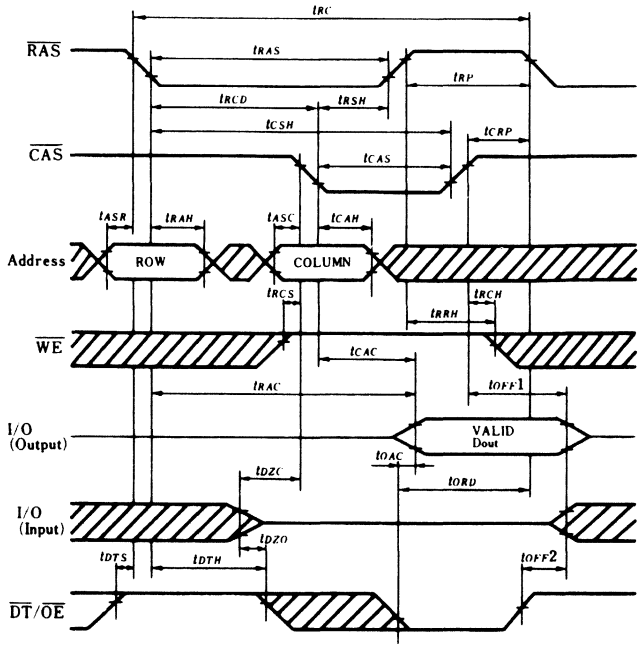
Parameter	Symbol	HM53461-10		HM53461-12		HM53461-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
SC Precharge Width	t_{SCP}	10	–	10	–	10	–	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	–	10	–	10	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	–	25	–	25	–	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	–	0	–	0	–	ns	
Serial Data-in Hold Time	t_{SIH}	15	–	20	–	25	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	–	0	–	0	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time(Read Transfer Cycle)	t_{RDH}	80	–	90	–	110	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	–	15	–	20	–	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	–	30	–	45	–	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	–	5	–	10	–	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	–	25	–	30	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	–	10	–	10	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	–	0	–	0	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	–	15	–	20	–	ms	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	–	0	–	0	–	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	–	15	–	20	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
$\overline{SC}$ to $\overline{RAS}$ Setup Time	t_{SRS}	30	–	40	–	45	–	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	–	30	–	35	–	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	–	60	–	75	–	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	–	15	–	20	–	ns	
Serial Write Enable Setup Time	t_{SWS}	0	–	0	–	0	–	ns	
Serial Write Enable Hold Time	t_{SWH}	35	–	35	–	55	–	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	–	0	–	0	–	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	–	35	–	55	–	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	–	10	–	10	–	ns	

Notes)

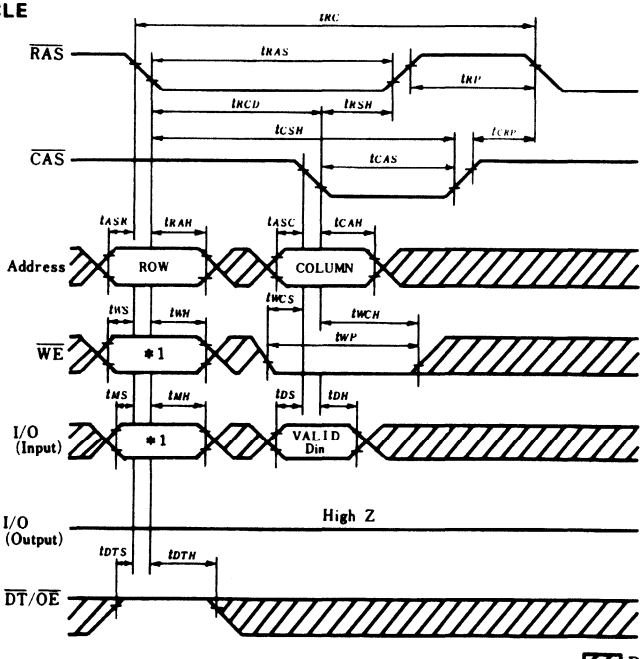
1. AC measurements assume t_T=5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$(max).
5. t_{OFF}(max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD}(max) limit insures that t_{RAC} (max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50pF.
11. An initial pause of 100μs is required after power-up. Then execute at least 8 initialization cycles.
12. After a read transfer cycle, the first SAM is needed to be read out before $\overline{CAS}$ falling edge in the succeeding read transfer cycle. When SAM is not read out after a read transfer cycle or when SAM read out is not used as valid data, the restriction mentioned above is not required.

■ WAVE FORMS

• READ CYCLE

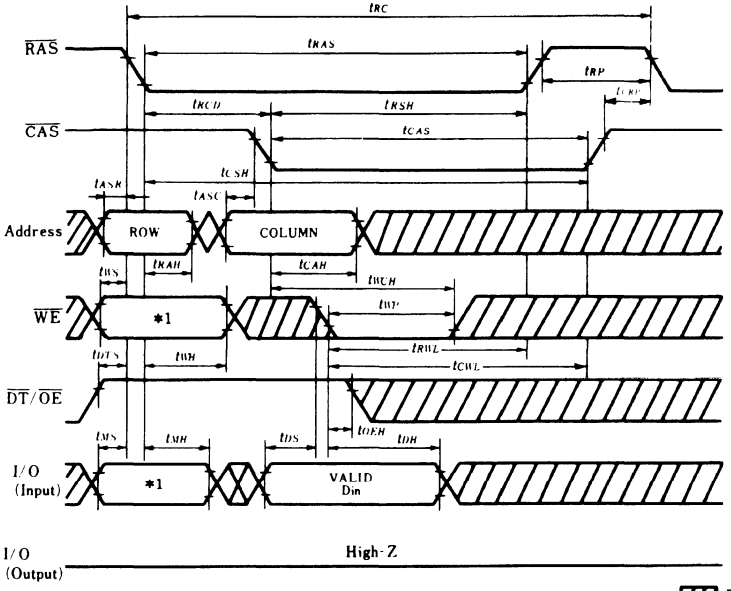


• EARLY WRITE CYCLE



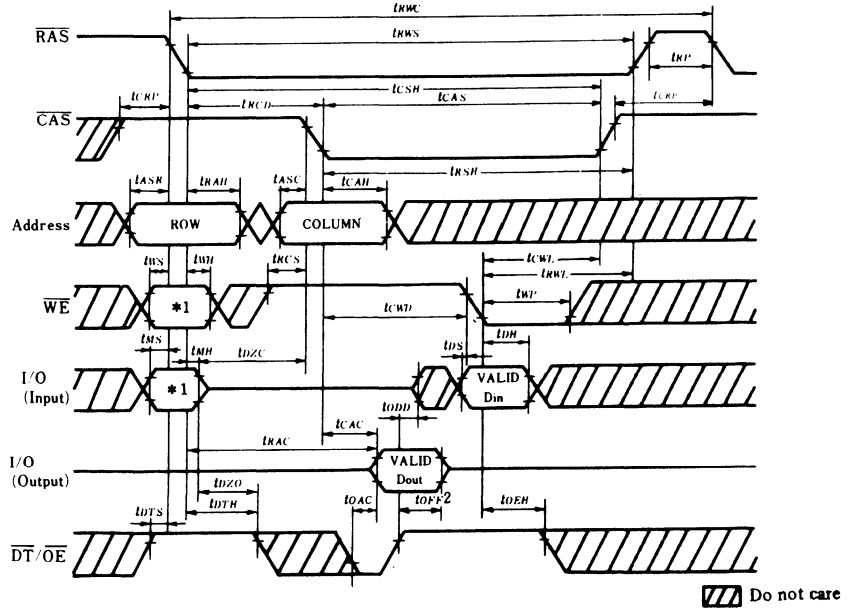
Note) *1. When $\overline{WE}$ is "H" level, the all data on the I/O can be written into the cell.
When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

• DELAYED WRITE CYCLE



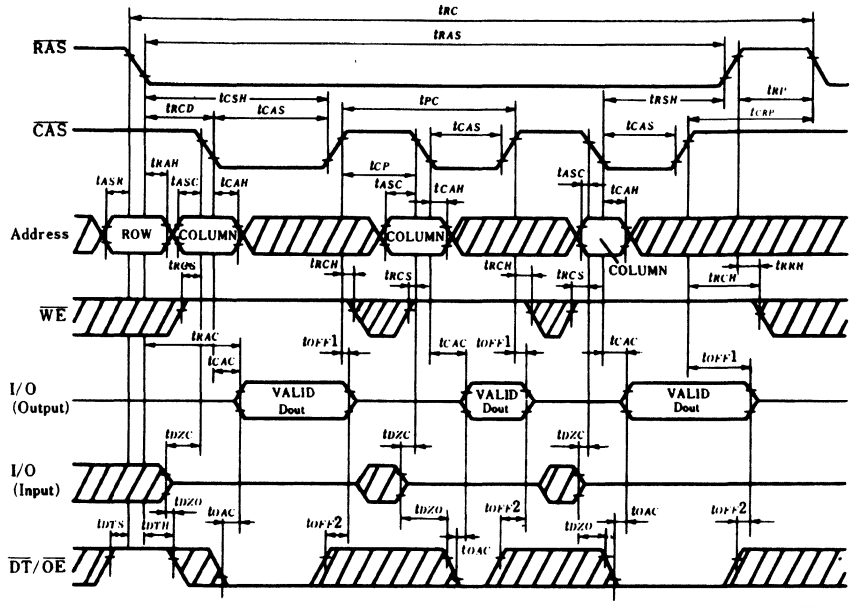
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written exept for when I/O="H" at the falling edge of $\overline{RAS}$.

• READ MODIFY WRITE CYCLE

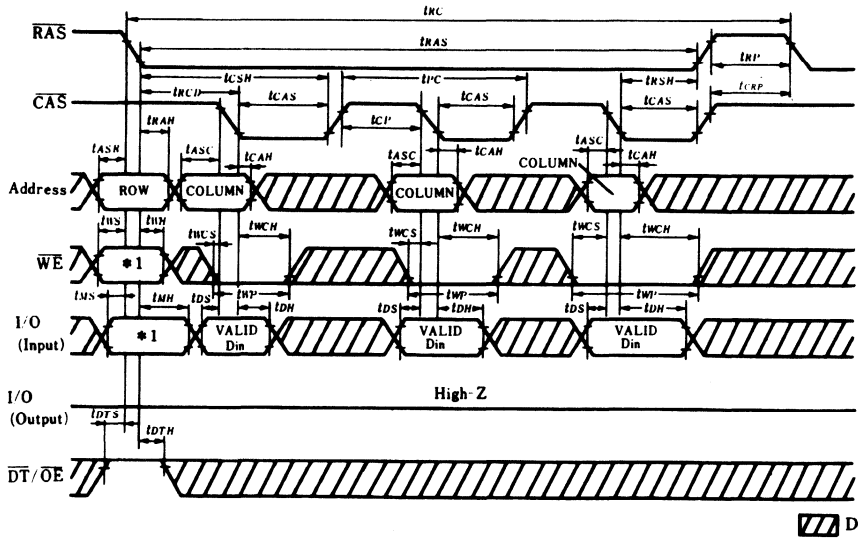


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE READ CYCLE

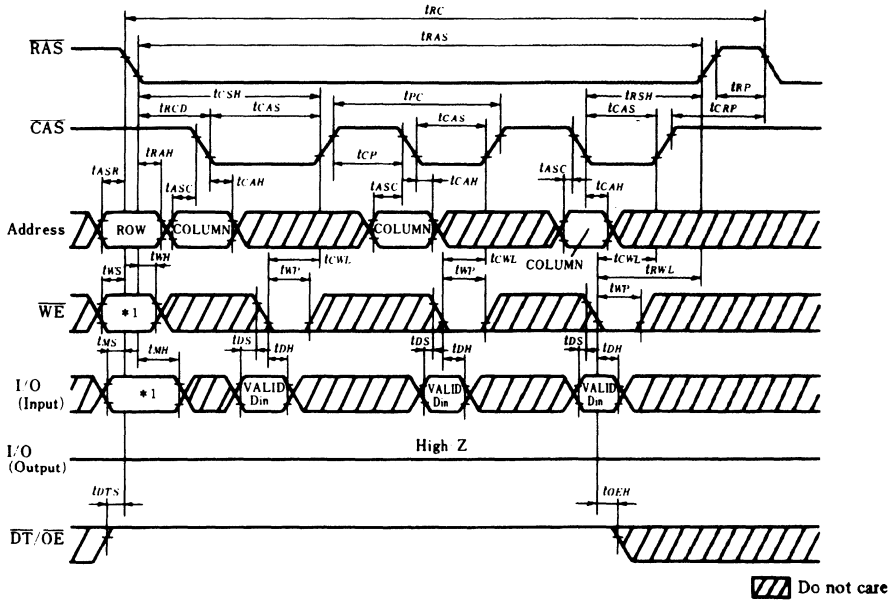


• PAGE MODE WRITE CYCLE (Early Write)



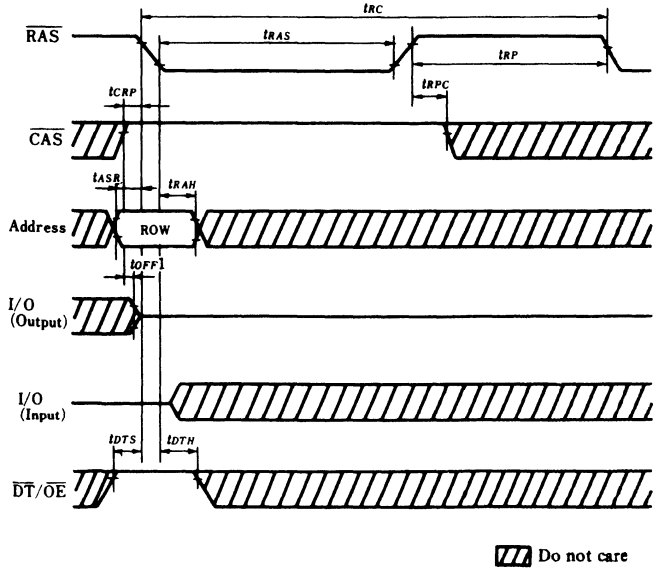
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

• PAGE MODE WRITE CYCLE (Delayed Write)

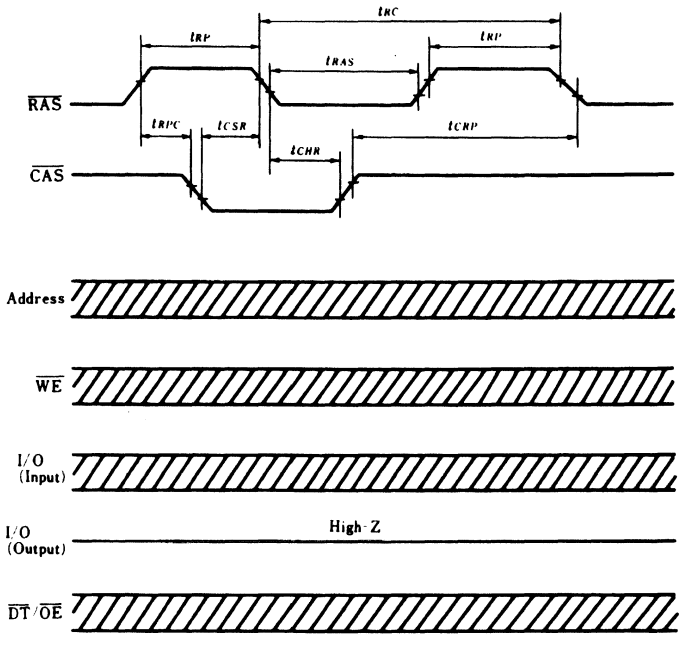


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of $\overline{RAS}$.

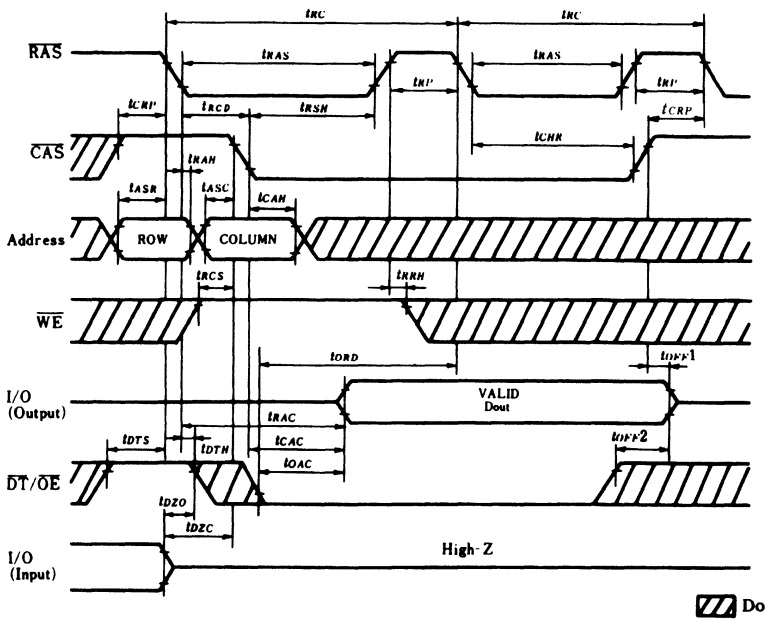
• $\overline{RAS}$-ONLY REFRESH CYCLE



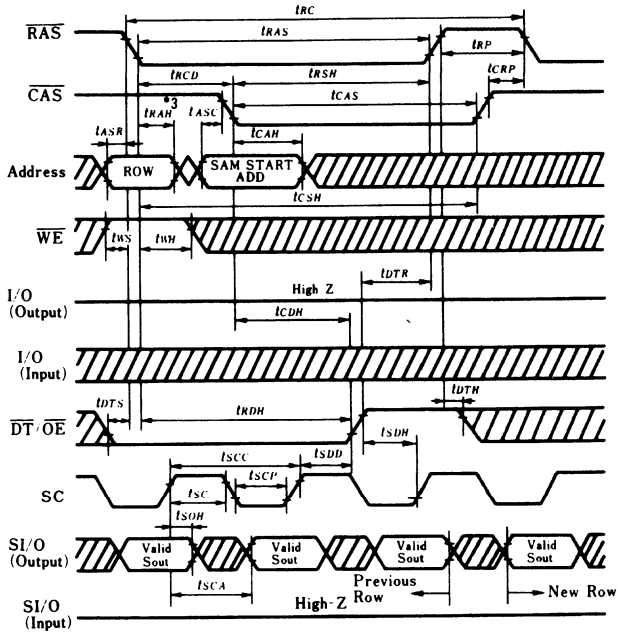
• $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH



• HIDDEN REFRESH CYCLE



• READ TRANSFER CYCLE (1)*1,*2



Note

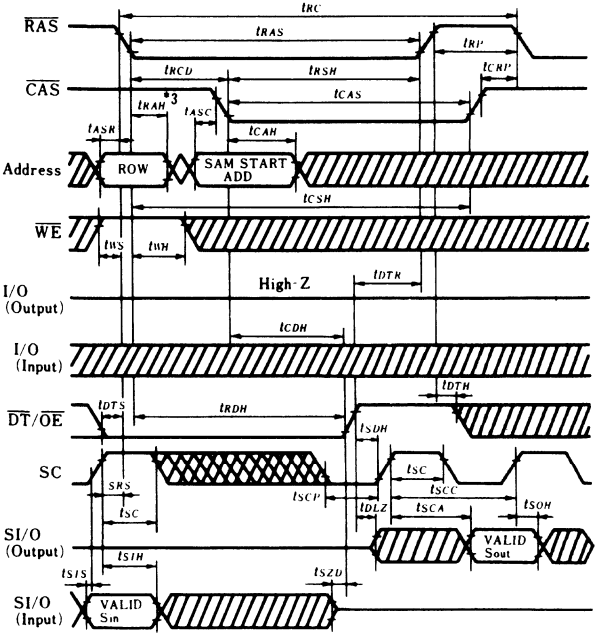
*1) In the case that the previous data transfer cycle was read transfer.

*2) Assume that $\overline{SOE}$ is "L" level.

*3) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

Do not care

• READ TRANSFER CYCLE (2)*1,*2



Do not care

Inhibit rising transient

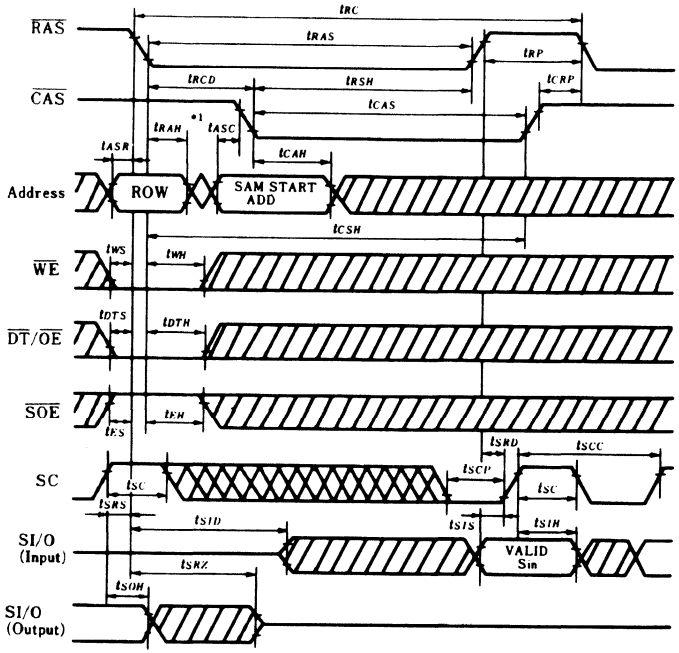
Note)

*1) In the case that the previous data transfer cycle was write transfer or pseudo transfer.

*2) Assume that $\overline{SOE}$ is "L" level,

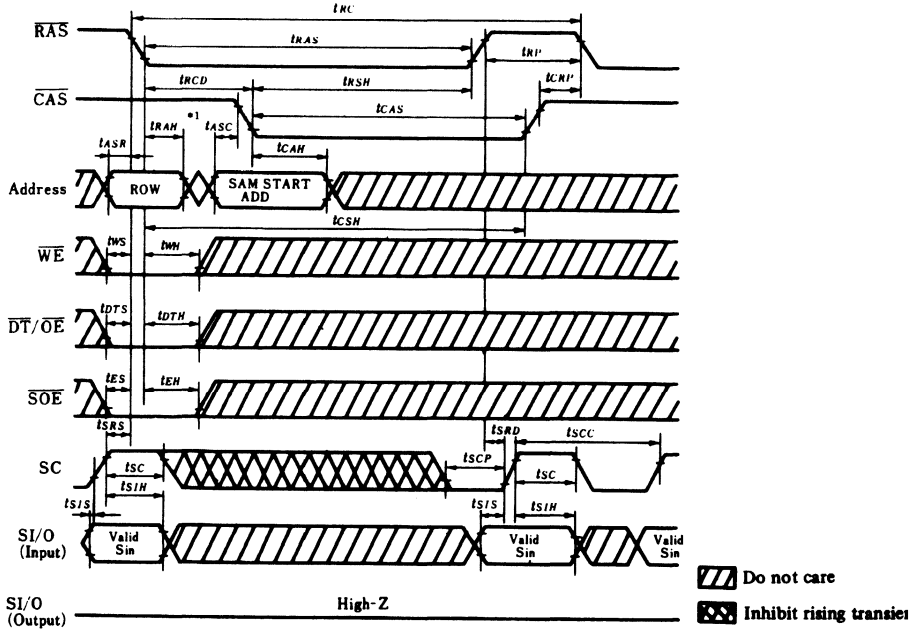
*3) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• PSEUDO TRANSFER CYCLE



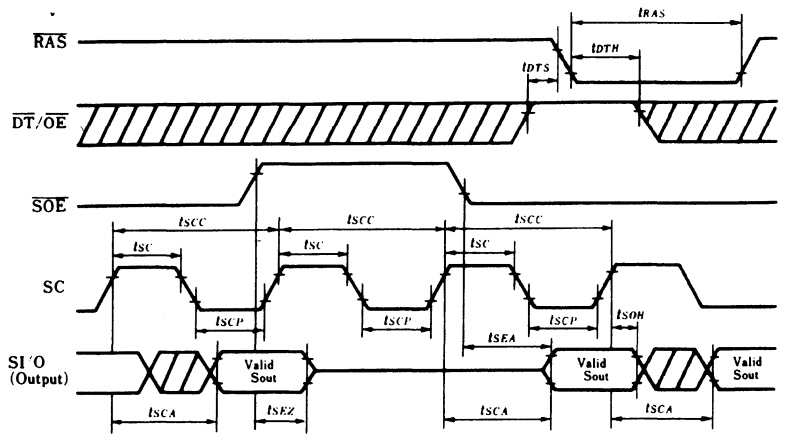
Note) *1. $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• WRITE TRANSFER CYCLE



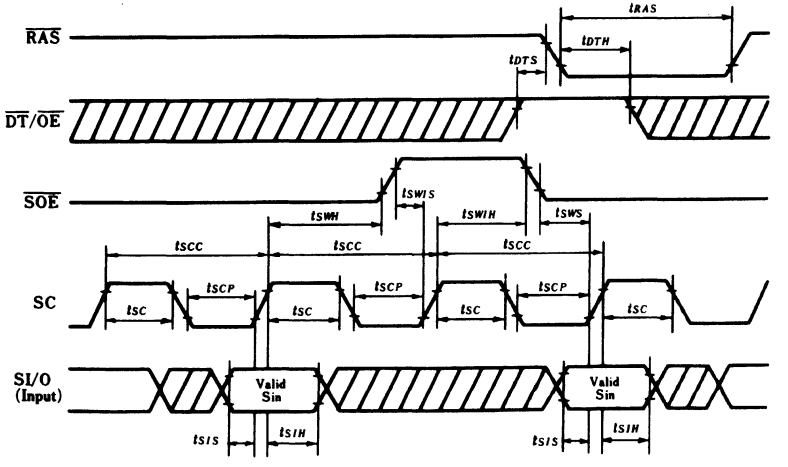
Note) *1. $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

• SERIAL READ CYCLE



▨ Do not care

• SERIAL WRITE CYCLE



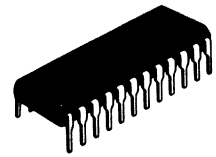
▨ Do not care

HM53462 Series

65,536-word x 4 bits Multiport CMOS Video RAM (with Logic operation mode)

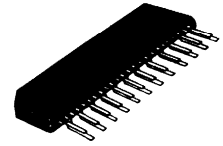
The HM53462 is a 262, 144 bit multiport memory equipped with a 64k-word x 4 bit Dynamic RAM port and a 256-word x 4-bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024-bit data register through a 256-word x 4-bit serial read or write access control. In the read transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. RAM port has another new function, logic operation capability. By this function logic operation between memory data and input data can be done in one cycle. Utilizing the Hitachi 2μm CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible.

HM53462P Series



(DP-24A)

HM53462ZP Series



(ZP-24)

HM53462JP Series

(CP-24D)

■ FEATURES

- Multiport organization
  (RAM; 64k-word x 4 bit and SAM; 256-word x 4 bit)
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V (±10%)
- Low powr Active RAM; 380 mW max.
  SAM; 220 mW max.
  Standby 40 mW max.
- Access Time RAM; 100ns/120ns/150ns
  SAM; 40ns/40ns/60ns
- Cycle Time Random read or write cycle time (RAM)
  190ns/220ns/260ns
  Serial read or write cycle time (SAM)
  40ns/40ns/60ns
- TTL compatible
- 256 refresh cycles . . 4ms
- Refresh function $\overline{RAS}$ – only refresh
  $\overline{CAS}$ – before – $\overline{RAS}$ refresh
  Hidden refresh
- Bidirectional data transfer operation (RAM ⇄ SAM)
- Fast serial access operation asynchronized with RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability
- Logic operation capability between Din and Dout
- SAM organization can be changed to 1024 x 1

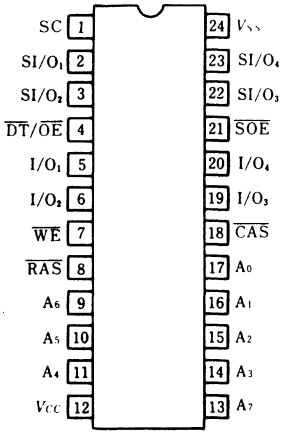
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM53462P-10 HM53462P-12 HM53462P-15	100ns 120ns 150ns	400 mil 24-pin Plastic DIP
HM53462ZP-10 HM53462ZP-12 HM53462ZP-15	100ns 120ns 150ns	24 pin Plastic ZIP
HM53462JP-10 HM53462JP-12 HM53462JP-15	100ns 120ns 150ns	24 pin Plastic SOJ

■ PIN ARRANGEMENT

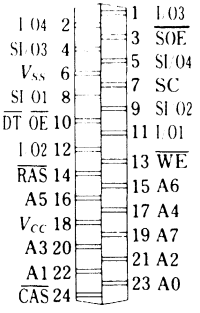
● HM53462P Series

HM53462JP Series



(Top View)

● HM53462ZP Series

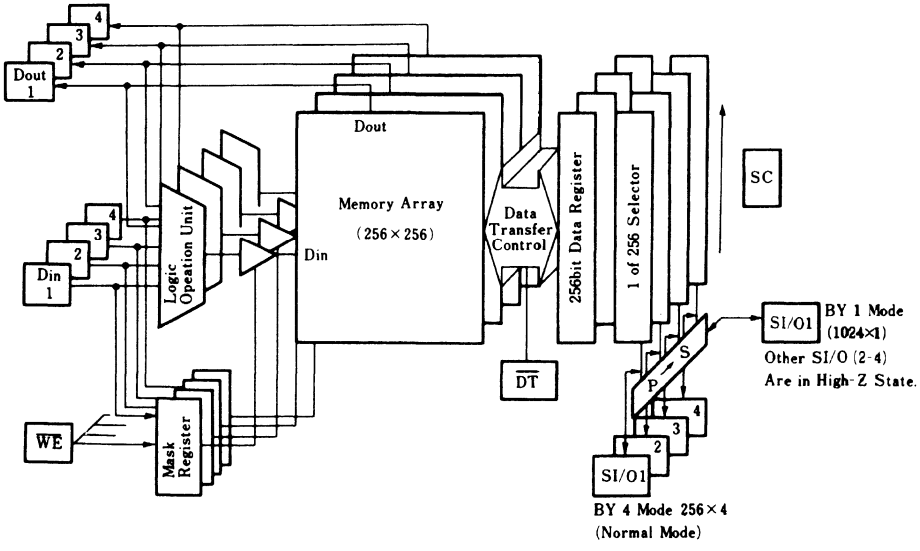


(Bottom View)

■ PIN DESCRIPTION

Pin Name	Function
A0 – A7	Address Inputs
I/O1 – I/O4	RAM Port Data Input/Output
SI/O1 – SI/O4	SAM Port Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
SC	Serial Clock
$\overline{WE}$	Write Enable
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{SOE}$	SAM Port Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Power supply voltage relative to V_{SS} . . . . . -0.5V to +7V
Operating temperature, T_a (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	CI_1	–	5	pF
Clocks	CI_2	–	5	pF
I/O, SI/O	$C_{I/O}$	–	7	pF

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	–	6.5	V
Input Low voltage	V_{IL}	-0.5*2	–	0.8	V

Notes) 1. All voltages referenced to V_{SS}.
2. -3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

RAM PORT	Symbol	SAM PORT Standby	SAM PORT Active	HM53462 -10	HM53462 -12	HM53462 -15	Unit
Operating current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC1}	O	X	70	60	50	mA
	I_{CC7}	X	O	110	100	80	mA
Standby current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	I_{CC2}	O	X	7	7	7	mA
	I_{CC8}	X	O	40	40	30	mA
$\overline{RAS}$ only refresh current $\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling t_{RC} = min.	I_{CC3}	O	X	60	50	40	mA
	I_{CC9}	X	O	100	90	70	mA
Page mode current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.	I_{CC4}	O	X	50	40	35	mA
	I_{CC10}	X	O	90	80	65	mA
CBR refresh current $\overline{RAS}$ cycling t_{RC} = min.	I_{CC5}	O	X	60	50	40	mA
	I_{CC11}	X	O	100	90	70	mA
Data transfer current $\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min.	I_{CC6}	O	X	75	65	55	mA
	I_{CC12}	X	O	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{LI}	-10	10	μA
Output leakage	I_{LO}	-10	10	μA
Output high voltage I_{OH} = -2 mA	V_{OH}	2.4	–	V
Output low voltage I_{OL} = 4.2 mA	V_{OL}	–	0.4	V

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)[1), 10), 11)]

Parameter	Symbol	HM53462 -10		HM53462 -12		HM53462 -15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
Read-Modify-Write Cycle Time	t_{RWC}	260	–	300	–	355	–	ns	
Page Mode Cycle Time	t_{PC}	70	–	85	–	105	–	ns	
Access Time from $\overline{RAS}$	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	25	–	30	–	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
$\overline{RAS}$ Pulse Width (Read-Modify-Write Cycle)	t_{RWS}	170	10000	200	10000	245	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	85	–	100	–	125	–	ns	8
$\overline{CAS}$ Setup Time ($\overline{CAS}$ – before – $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ – before – $\overline{RAS}$ refresh)	t_{CHR}	20	–	25	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	25	–	30	–	40	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	25	–	30	–	40	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	10	–	15	–	20	–	ns	
Data-in to $\overline{CAS}$ Delay Time	t_{DZC}	0	–	0	–	0	–	ns	
Data-in to $\overline{OE}$ Delay Time	t_{DZO}	0	–	0	–	0	–	ns	
$\overline{OE}$ to $\overline{RAS}$ Delay Time	t_{ORD}	35	–	40	–	45	–	ns	

(to be continued)

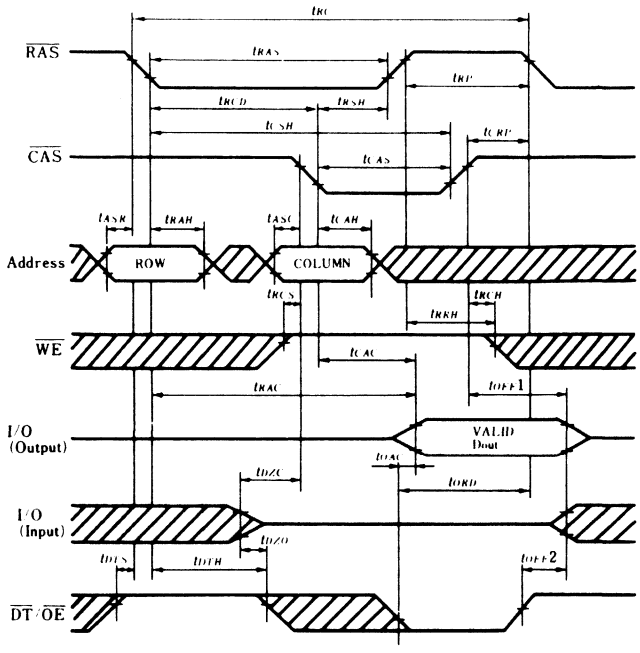
Parameter	Symbol	HM53462 -10		HM53462 -12		HM53462 -15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Serial Clock Cycle Time	t_{SCC}	40	–	40	–	60	–	ns	
Access Time from SC	t_{SCA}	–	40	–	40	–	60	ns	10
Access Time from $\overline{SOE}$	t_{SEA}	–	25	–	30	–	40	ns	10
SC Pulse Width	t_{SC}	10	–	10	–	10	–	ns	
SC Precharge Width	t_{SCP}	10	–	10	–	10	–	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	–	10	–	10	–	ns	
Serial Output Buffer Turn-off Delay from $\overline{SOE}$	t_{SEZ}	–	25	–	25	–	30	ns	
Serial Data-in Setup Time	t_{SIS}	0	–	0	–	0	–	ns	
Serial Data-in Hold Time	t_{SIH}	15	–	20	–	25	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Setup Time	t_{DTS}	0	–	0	–	0	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time (Read Transfer Cycle)	t_{RDH}	80	–	90	–	110	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Hold Time	t_{DTH}	15	–	15	–	20	–	ns	
$\overline{DT}$ to $\overline{CAS}$ Hold Time	t_{CDH}	20	–	30	–	45	–	ns	
Last SC to $\overline{DT}$ Delay Time	t_{SDD}	5	–	5	–	10	–	ns	
First SC to $\overline{DT}$ Hold Time	t_{SDH}	25	–	25	–	30	–	ns	
$\overline{DT}$ to $\overline{RAS}$ Delay Time	t_{DTR}	10	–	10	–	10	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Setup Time	t_{WS}	0	–	0	–	0	–	ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time	t_{WH}	15	–	15	–	20	–	ns	
I/O to $\overline{RAS}$ Setup Time	t_{MS}	0	–	0	–	0	–	ns	
I/O to $\overline{RAS}$ Hold Time	t_{MH}	15	–	15	–	20	–	ns	
Serial Output Buffer Turn off Delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	75	ns	
SC to $\overline{RAS}$ Setup Time	t_{SRS}	30	–	40	–	45	–	ns	
$\overline{RAS}$ to SC Delay Time	t_{SRD}	25	–	30	–	35	–	ns	
Serial Data Input Delay Time from $\overline{RAS}$	t_{SID}	50	–	60	–	75	–	ns	
Serial Data Input to $\overline{DT}$ Delay Time	t_{SZD}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Setup Time	t_{ES}	0	–	0	–	0	–	ns	
$\overline{SOE}$ to $\overline{RAS}$ Hold Time	t_{EH}	15	–	15	–	20	–	ns	
Serial Write Enable Setup Time	t_{SWS}	0	–	0	–	0	–	ns	
Serial Write Enable Hold Time	t_{SWH}	35	–	35	–	55	–	ns	
Serial Write Disable Setup Time	t_{SWIS}	0	–	0	–	0	–	ns	
Serial Write Disable Hold Time	t_{SWIH}	35	–	35	–	55	–	ns	
$\overline{DT}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	–	10	–	10	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycle and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50 pF.
11. After power-up, pause for more than 100μs and execute at least 8 initialization cycles. Then execute at least one logic reset cycle including write mask reset (on the falling edge of $\overline{RAS}$, $\overline{WE}$ = "Low" and I/O1 – I/O = "High"), and execute one or more transport cycle for initiation of SAM port.
12. After a read transfer cycle, the first SAM is needed to be read out before $\overline{CAS}$ falling edge in the succeeding read transfer cycle. When SAM is not read out after a read transfer cycle or when SAM read out is not used as valid data, the restriction mentioned above is not required.

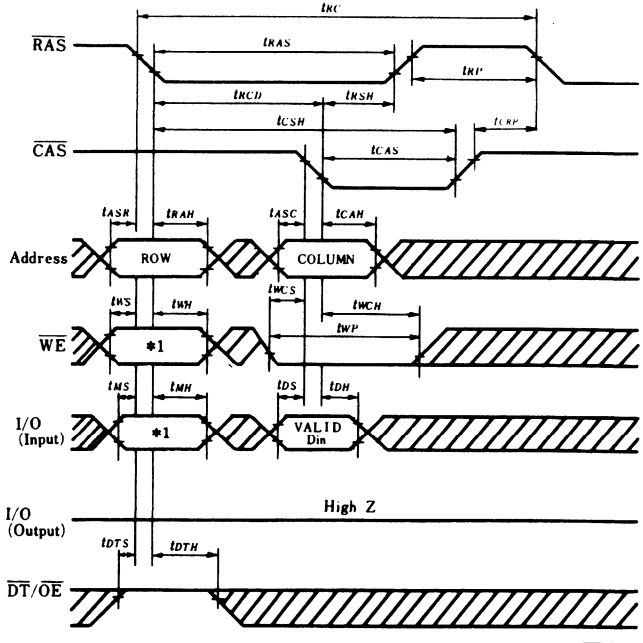
■ WAVE FORMS

• READ CYCLE



Do not care

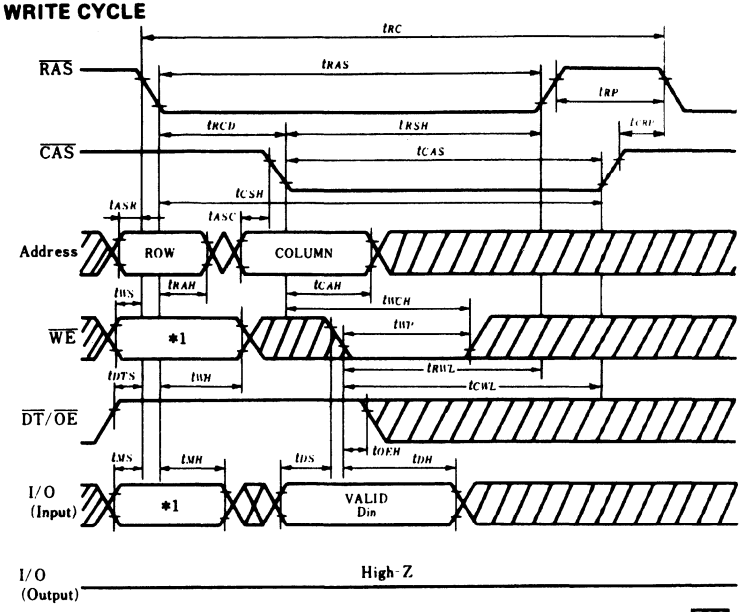
• EARLY WRITE CYCLE



Do not care

Note) *1. When $\overline{WE}$ is "H" level, the all data on the I/O can be written into the cell. When $\overline{WE}$ is "L" level, the data on the I/O are not written except for when I/O is "H" level at the falling edge of $\overline{RAS}$.

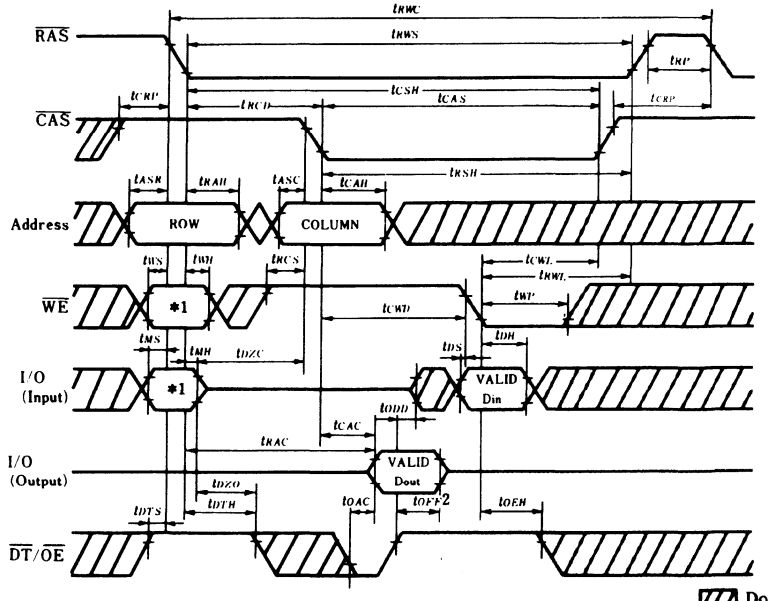
- **DELAYED WRITE CYCLE**



▨ Do not care

Note) *1. When WE is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When WE is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.

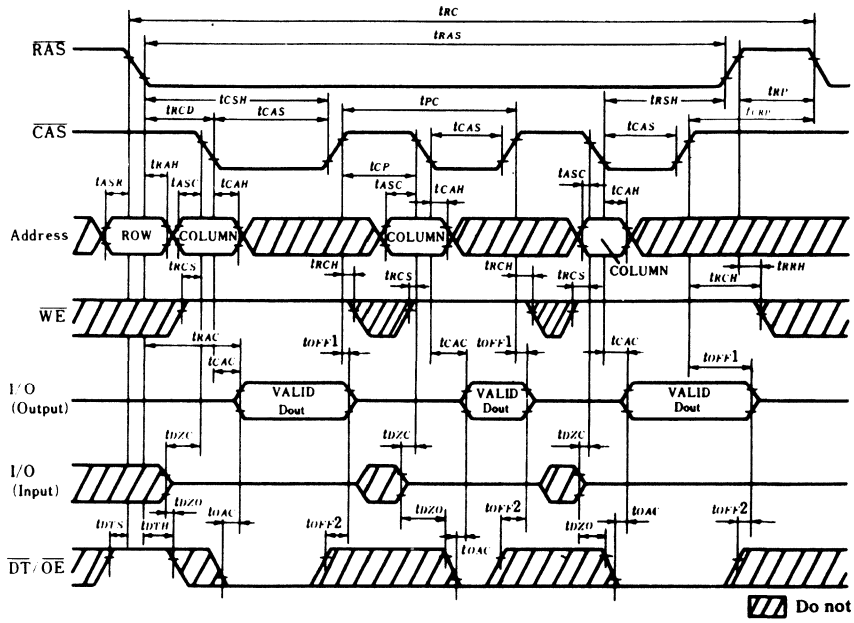
- **READ MODIFY WRITE CYCLE**



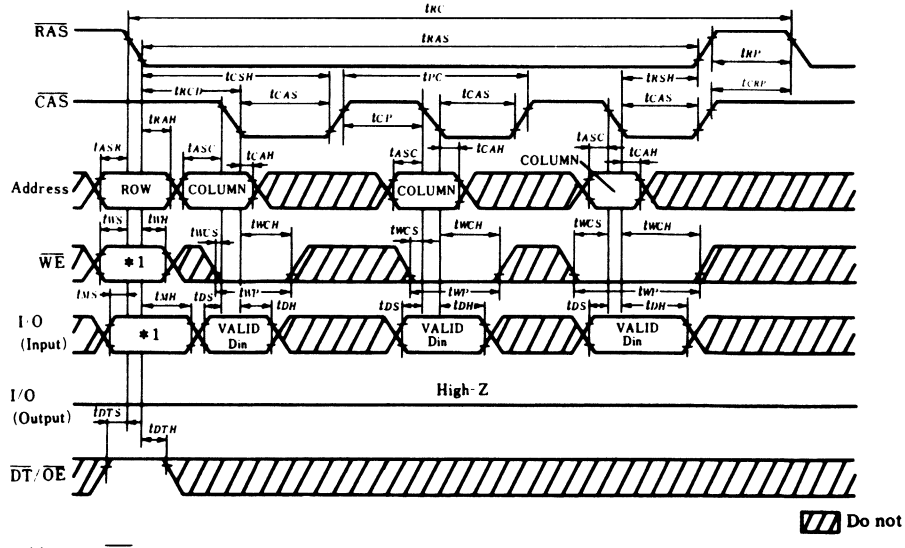
▨ Do not care

Note) *1. When WE is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When WE is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.

- **PAGE MODE READ CYCLE**

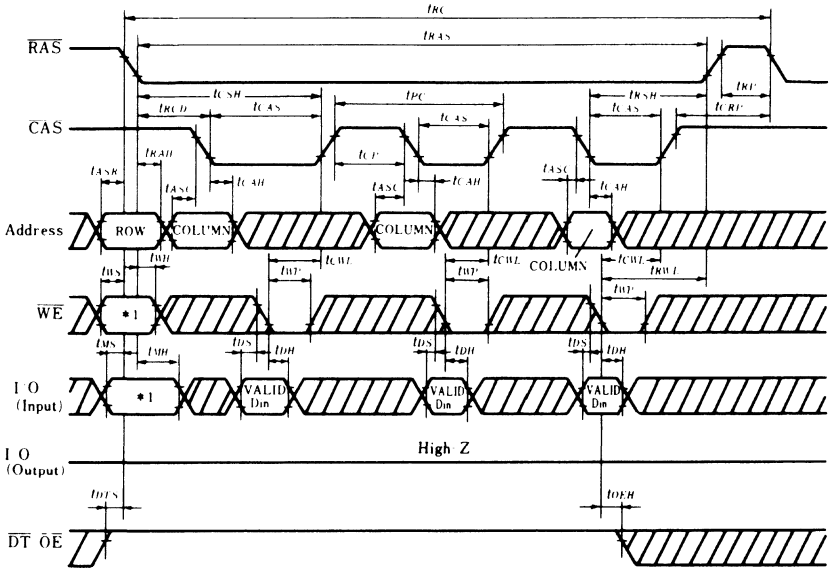


- **PAGE MODE WRITE CYCLE (Early Write)**



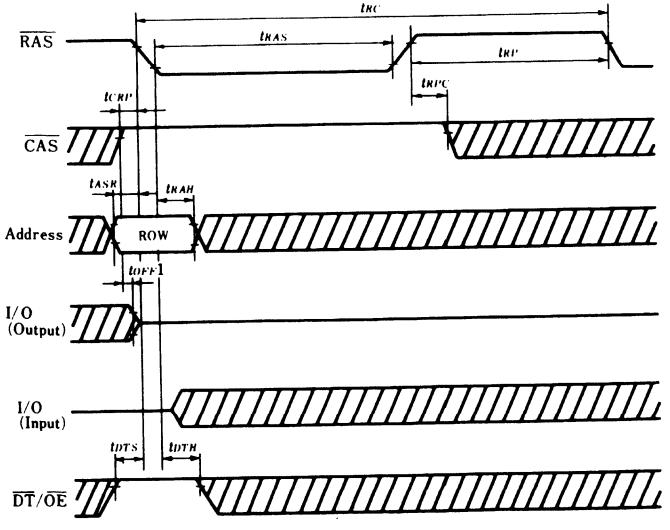
Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1–I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

- **PAGE MODE WRITE CYCLE (Delayed Write)**

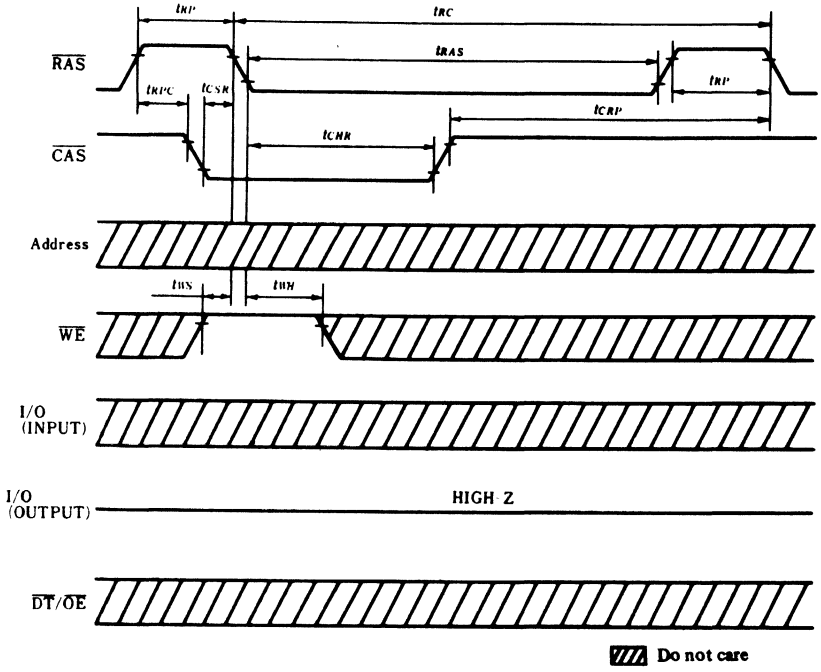


Note) *1. When $\overline{WE}$ is "H" level, all the data on I/O1-I/O4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

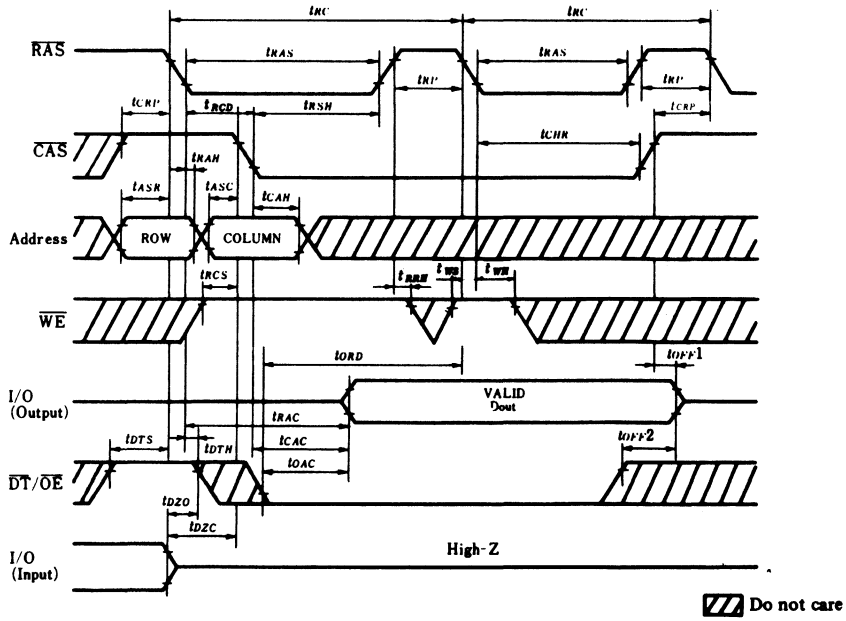
- **$\overline{RAS}$-ONLY REFRESH CYCLE**



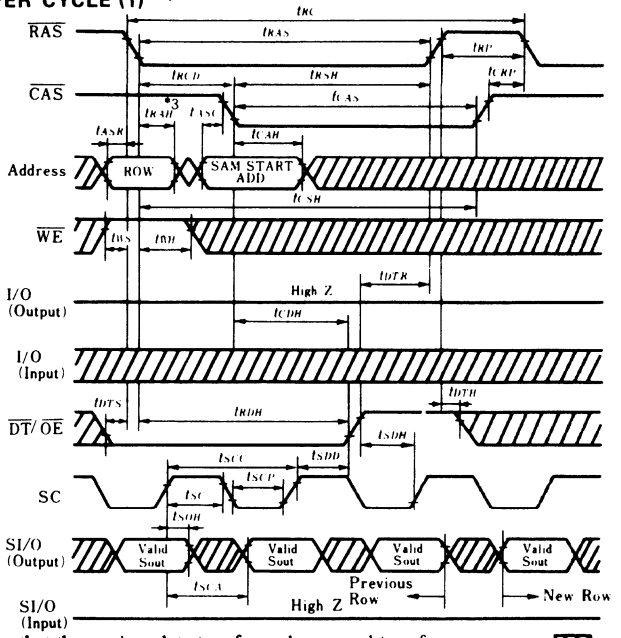
• $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



• HIDDEN REFRESH CYCLE



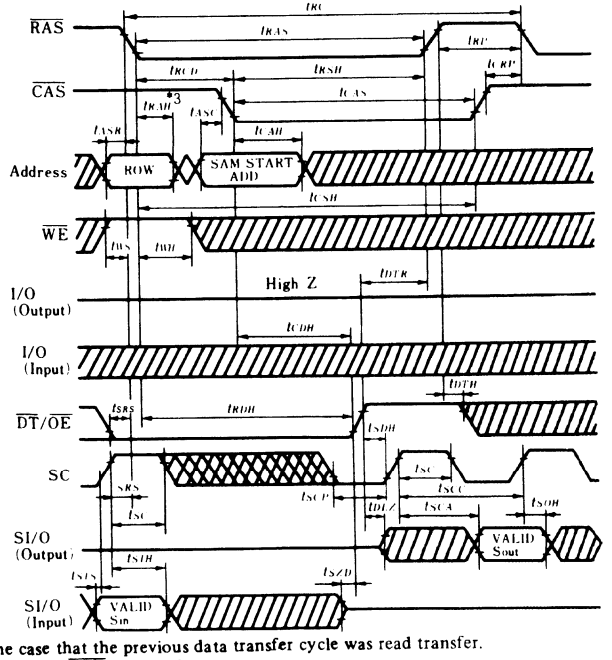
• READ TRANSFER CYCLE (1)*1,*2



NOTE *1) In the case that the previous data transfer cycle was read transfer.
*2) Assume that $\overline{SOE}$ is "Low".
*3) $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

Do not care

• READ TRANSFER CYCLE (2)*1,*2

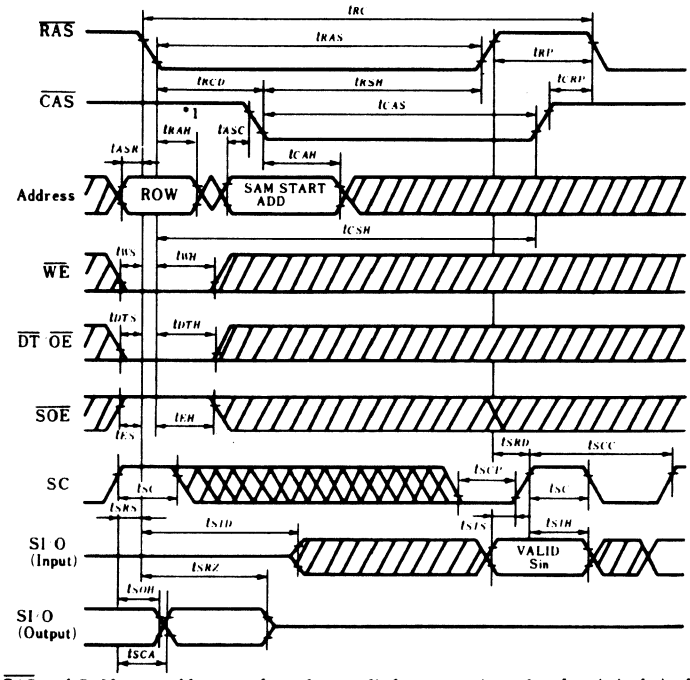


Do not care

Inhibit rising transient

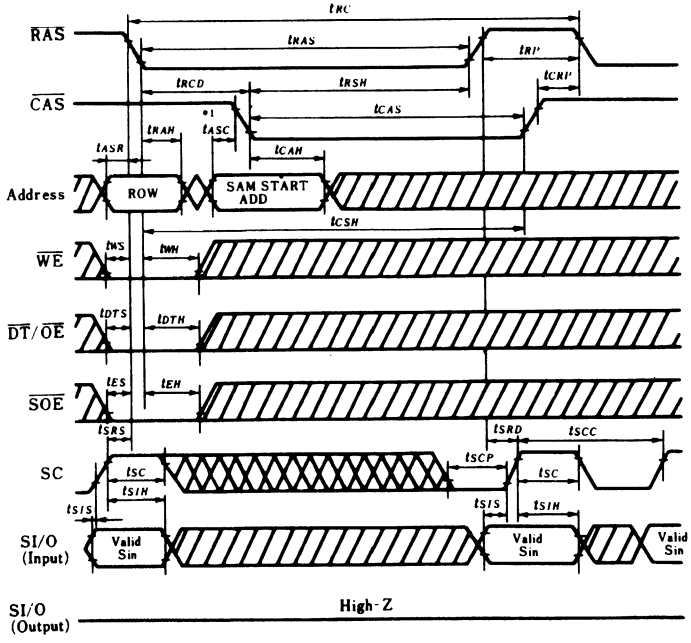
NOTE *1) In the case that the previous data transfer cycle was read transfer.
*2) Assume that $\overline{SOE}$ is "Low"
*3) $\overline{CAS}$ and SAM start Address need not be supplied every cycle, only when it is desired to change to a new $\overline{SAM}$ start Address.

• PSEUDO TRANSFER CYCLE



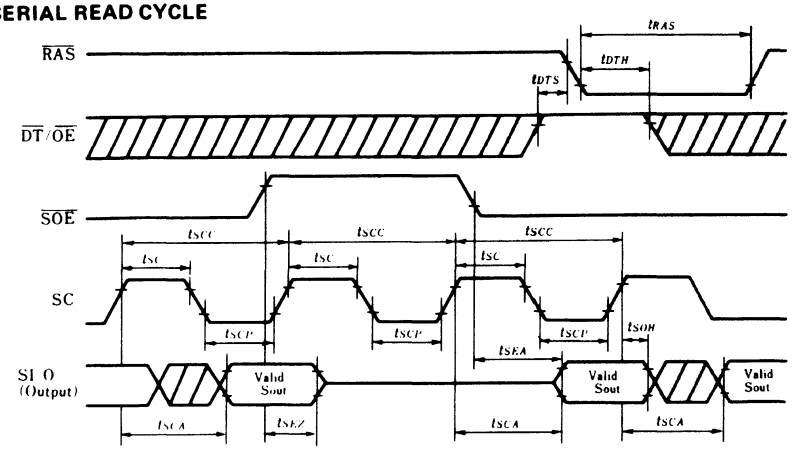
*1) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• WRITE TRANSFER CYCLE

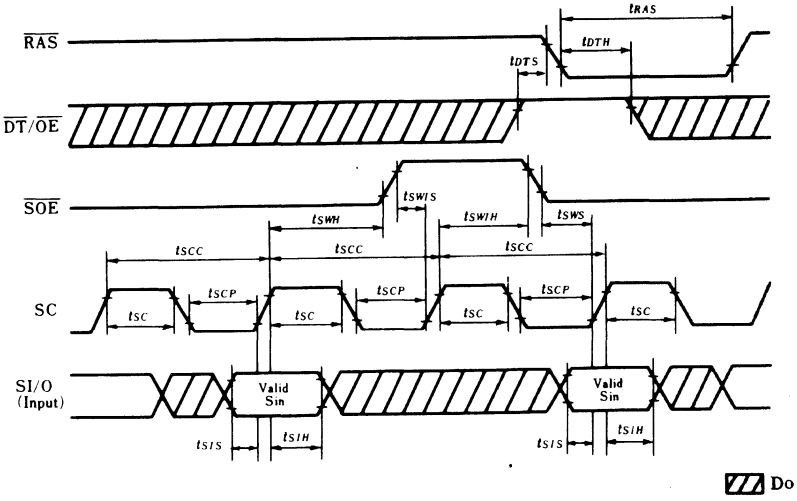


*1) $\overline{CAS}$ and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

• SERIAL READ CYCLE



• SERIAL WRITE CYCLE



■ ELECTRICAL AC CHARACTERISTICS (Logic operation mode)

Parameter	Symbol	HM53462-10		HM53462-12		HM53462-15		Unit
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{FRC}	230	–	265	–	310	–	ns
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	165	10000	200	10000	ns
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	80	10000	95	10000	105	10000	ns
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	–	165	–	200	–	ns
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	80	–	95	–	105	–	ns
Page mode cycle time (Write cycle)	t_{FPC}	100	–	120	–	135	–	ns
$\overline{CAS}$ hold time (Logic operation set/reset cycle)	t_{FCHR}	90	–	100	–	120	–	ns
$\overline{CAS}$ hold time from $\overline{RAS}$ precharge (x4 → x1 set cycle)	t_{PSCH}	10	–	10	–	10	–	ns

■ **LOGIC CODE** (FC0 – 3 are AX0 – AX3 in Logic Operation Set Cycle)

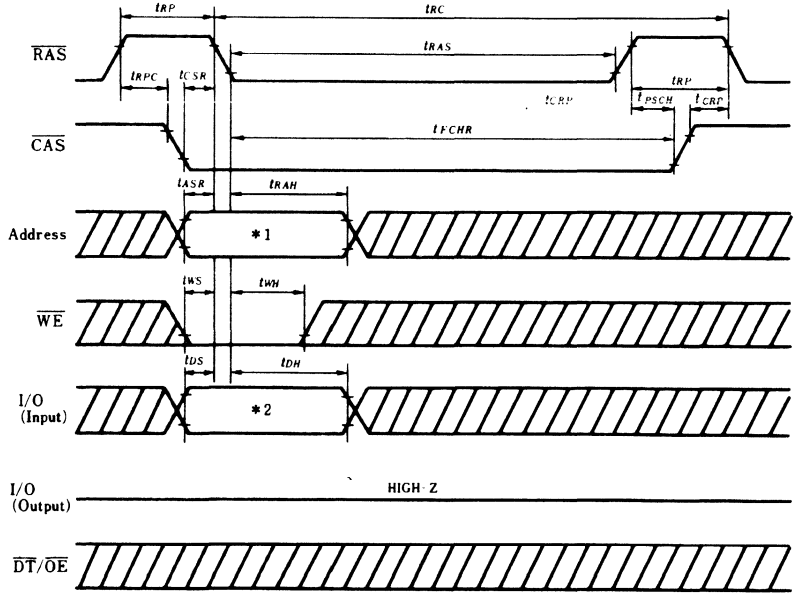
FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	Di · Mi
0	0	1	0	AND2	$\overline{Di}$ · Mi
0	0	1	1	X4 → X1	–
0	1	0	0	AND3	Di · $\overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di}$ · Mi + Di · $\overline{Mi}$
0	1	1	1	OR1	Di + Mi
1	0	0	0	NOR	$\overline{Di}$ · $\overline{Mi}$
1	0	0	1	ENOR	Di · Mi + $\overline{Di}$ · $\overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di}$ + Mi
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	Di + $\overline{Mi}$
1	1	1	0	NAND	$\overline{Di}$ + $\overline{Mi}$
1	1	1	1	1	ONE

→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

Di : External Data-in
Mi : The data of the memory cell

● **LOGIC OPERATION SET/RESET CYCLE** (With $\overline{CAS}$ before $\overline{RAS}$ refresh)

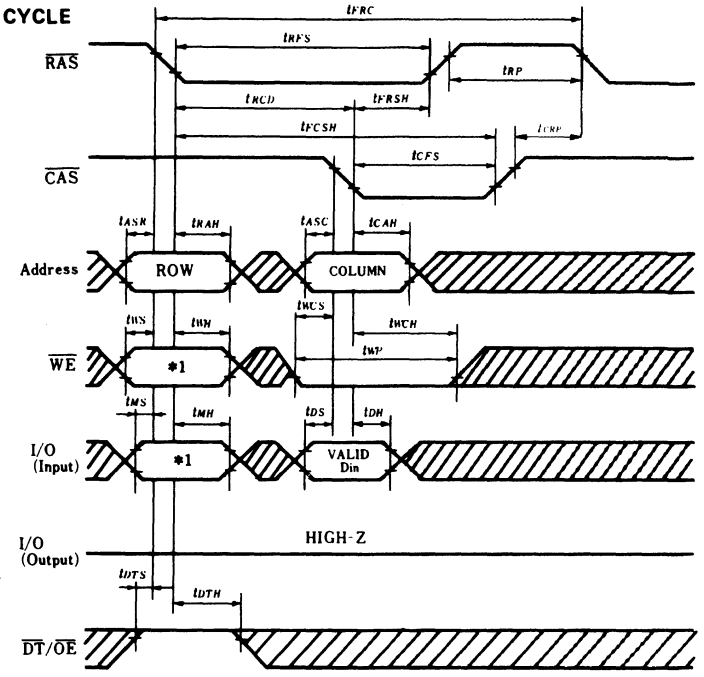


▨ Do not care

*1) Logic code A0-A3 (A4-A7: don't care)
*2) Write mask data

■ LOGIC OPERATION MODE

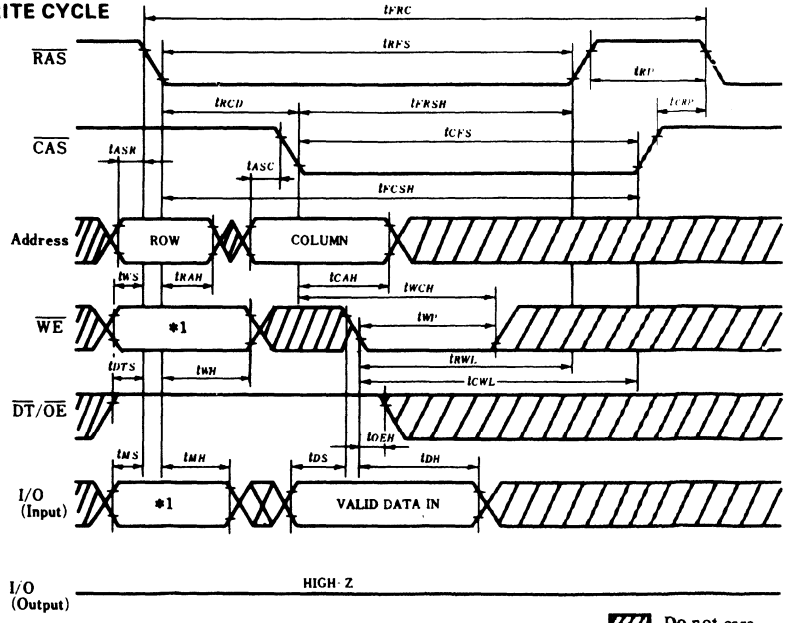
• EARLY WRITE CYCLE



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

▨ Do not care

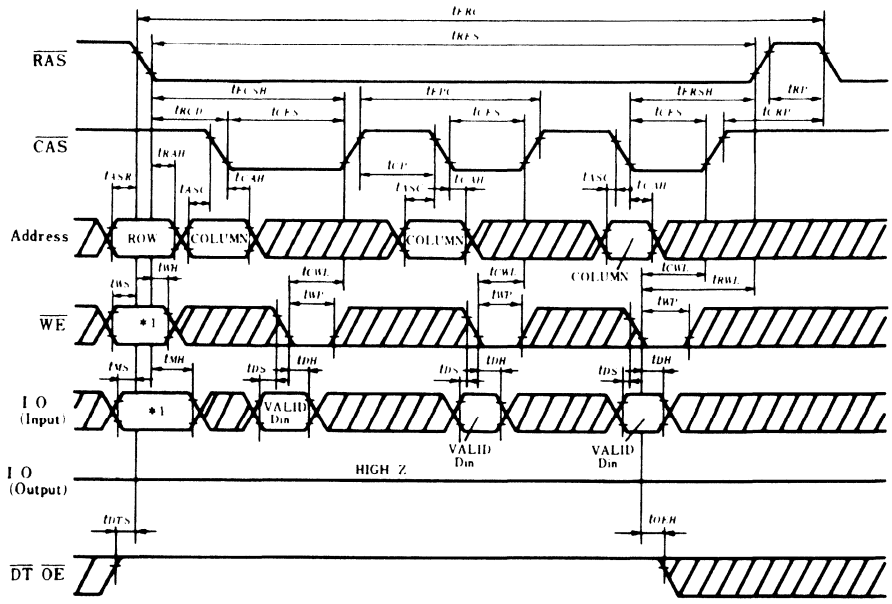
• DELAYED WRITE CYCLE



NOTE 1) When $\overline{WE}$ is "H" level, all the data on I/01-4 can be written into the memory cell.
When $\overline{WE}$ is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of $\overline{RAS}$.

▨ Do not care

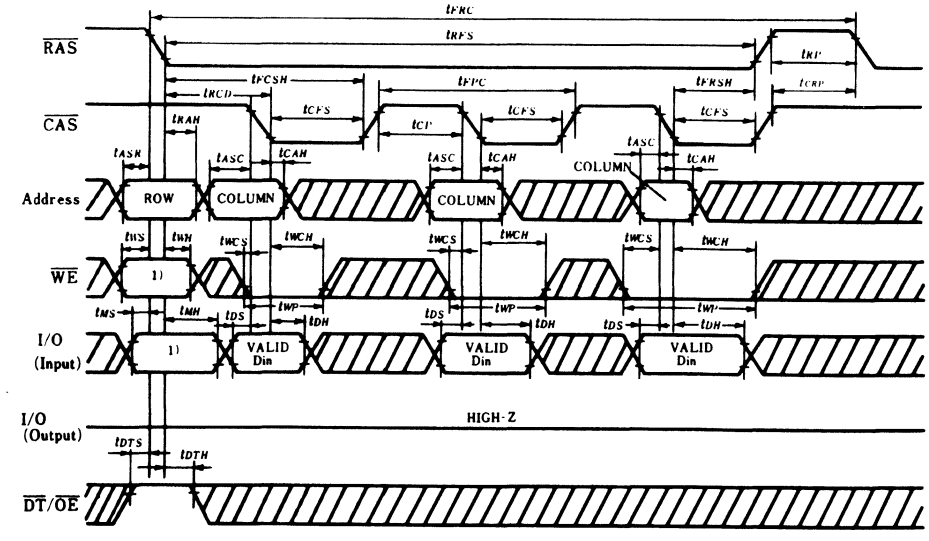
- **PAGE MODE WRITE CYCLE** (Delayed Write)



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

Do not care

- **PAGE MODE WRITE CYCLE** (Early Write)



Note) *1. When $\overline{WE}$ is 'high', the all data on the I/O can be written into the cell.
When $\overline{WE}$ is 'low', the data on the I/O are not written except for when I/O is 'high' at the falling edge of $\overline{RAS}$.

Do not care

■ DESCRIPTION

1. LOGIC OPERATION MODE

HM53462 has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between Din and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{CAS}$ and $\overline{WE}$ low when $\overline{RAS}$ falls (Fig. 1). The logic code and the bits to be masked are determined respectively by Ax0-3 state and I/01-4 state at the falling edge of $\overline{RAS}$. Furthermore, in this cycle $\overline{CAS}$ – before – $\overline{RAS}$ refresh operation is executed, too. In the case of executing the conventional $\overline{CAS}$ – before – $\overline{RAS}$ refresh operation, $\overline{WE}$ must be high when $\overline{RAS}$ falls.

2.1. Logic code

The logic code is shown in Table 1. When power is turned on, at least one logic reset cycle including write mask reset is required to initialize logic code. If the logic code is (Ax3, Ax2, Ax1, Ax0) = (0, 0, 1, 1), the SAM organization is changed converter (Fig. 2). In the case that the SAM organization is changed to 1,024 x 1, one data transfer cycle is needed to initialie the SAM selector.

Once the SAM organization is changed to 1024 x 1, this code is maintained unless power is turned off.

2.2. Write mask

HM53462 has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{WE}$ low at the falling edge of $\overline{RAS}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

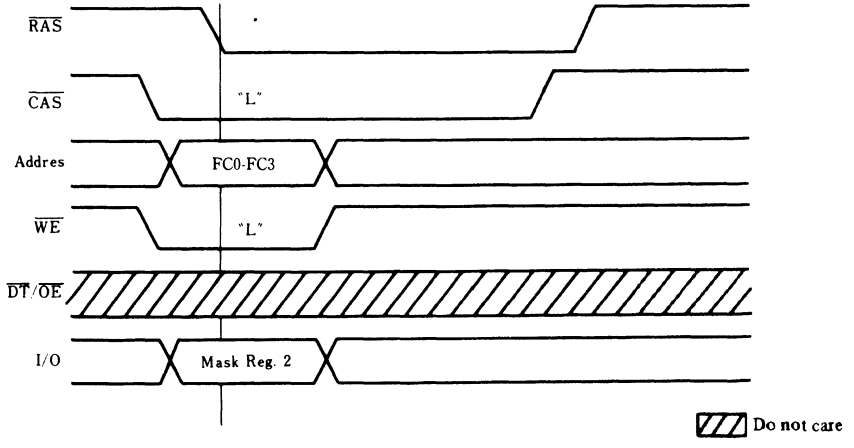


Fig. 1 LOGIC OPERATION SET/RESET CYCLE

Table 1. LOGIC CODE (FC0 – FC3 are AX0 – AX3 in Logic Operation Set Cycle)

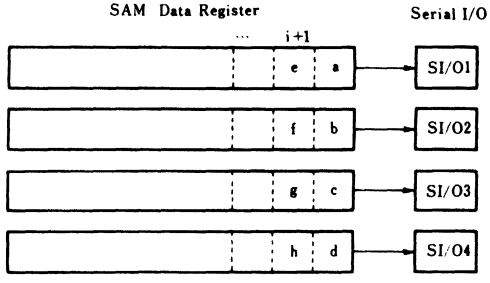
FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$Di \cdot Mi$
0	0	1	0	AND2	$\overline{Di} \cdot Mi$
0	0	1	1	X4 →X1	–
0	1	0	0	AND3	$Di \cdot \overline{Mi}$
0	1	0	1	THROUGH	Di
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$
0	1	1	1	OR1	$Di + Mi$
1	0	0	0	NOR	$\overline{Di} \cdot \overline{Mi}$
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$
1	0	1	0	INV1	$\overline{Di}$
1	0	1	1	OR2	$\overline{Di} + Mi$
1	1	0	0	INV2	$\overline{Mi}$
1	1	0	1	OR3	$Di + \overline{Mi}$
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$
1	1	1	1	1	ONE

→ SAM organization changes to 1024 x 1

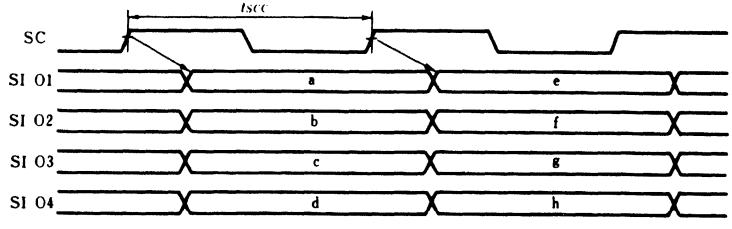
→ Logic operation mode reset

Di : External Data-in
Mi : The data of the memory cell

Fig. 2 THE SHIFT WAY OF SAM DATA



1) By 4 mode (SAM organization: 256 x 4)



2) By 1 mode (SAM organization: 1024 x 1)

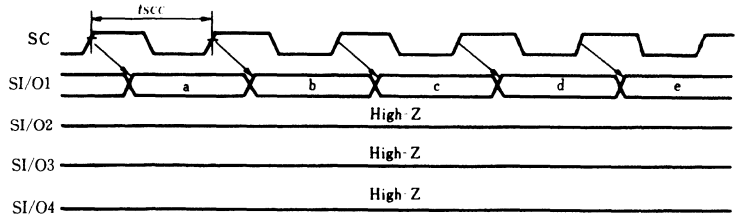


Fig. 3 EXAMPLE OF LOGIC OPERATION MODE

	Logic operation set/reset cycle	Write cycle	Write cycle	Write cycle	Write cycle
$\overline{RAS}$					
$\overline{CAS}$	"L"	"H"	"H"	"H"	"H"
$\overline{WE}$	"L"	"H"	"L"	"H"	"H"
I/O1		"0" Write	Masked	"1" Write	"0" Write
I/O2		Masked	"1" Write	Masked	Masked
I/O3		Masked	"0" Write	Masked	Masked
I/O4		"1" Write	Masked	"0" Write	"1" Write
Logic	—	AND1	THROUGH	AND1	AND1
	Mask reg.2 is set I O2,3 :Masked Assume that the logic is set to "AND1".		Mask reg.1 is set, and valid only in this cycle. I O1,4:Masked		

HM534251 Series

262144-Word × 4-Bit Multiport CMOS Video RAM

The HM534251 is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function. It is suitable for a graphic processing buffer memory.

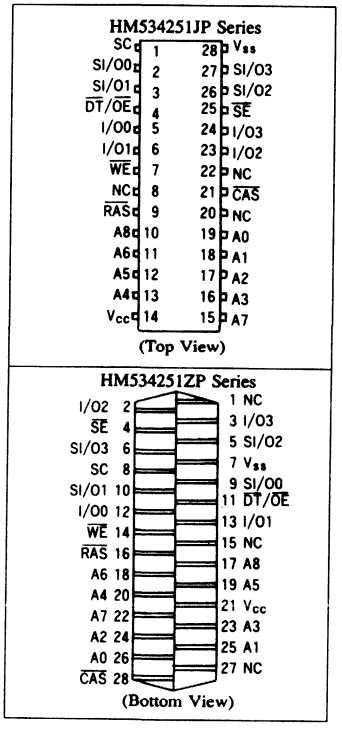
Feautues

- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 256-kword x 4-bit and SAM: 512-word x 4-bit
- Access time RAM: 100 ns/100 ns/120 ns/150 ns max
  SAM: 30 ns/35 ns/40 ns/50 ns max
- Cycle time RAM: 190 ns/190 ns/220 ns/260 ns min
  SAM: 30 ns/40 ns/40 ns/60 ns min
- Low power
  - Active RAM: 385 mW max
    SAM: 358 mW max
  - Standby 40 mW max
- High-speed page mode capability
- Mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{RAS}$-only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM534251JP-10	100 ns	400-mil
HM534251JP-11	100 ns	28-pin
HM534251JP-12	120 ns	Plastic SOJ (CP-28D)
HM534251JP-15	150 ns	
HM534251ZP-10	100 ns	400-mil
HM534251ZP-11	100 ns	28-pin
HM534251ZP-12	120 ns	Plastic ZIP (ZP-28)
HM534251ZP-15	150 ns	

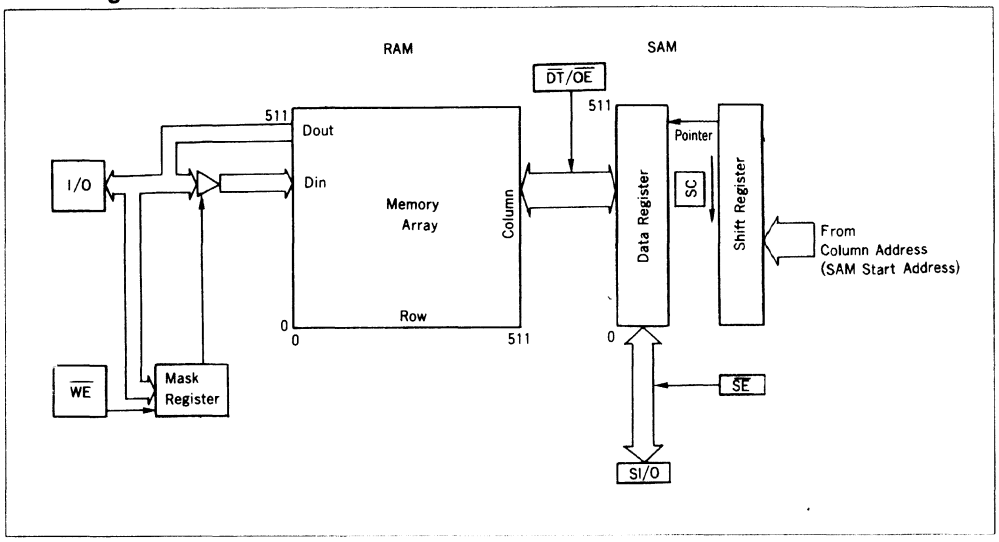
Pin Arrangement



Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O0–I/O3	RAM port data inputs/ outputs
SI/O0–SI/O3	SAM port data inputs/ outputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{DT/OE}$	Data transfer/Output enable
SC	Serial clock
$\overline{SE}$	SAM port enable
Vcc	Power supply
Vss	Ground
NC	No connection

Block Diagram



Pin Function

$\overline{RAS}$ (input pin): $\overline{RAS}$ is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of $\overline{RAS}$. The input level of those signals determine the operation cycle of the HM534251.

Table 1. Operation Cycles of the HM534251

Input level at the falling edge of $\overline{RAS}$				Operation Cycle
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WE}$	$\overline{SE}$	
H	H	H	×	RAM read/write
H	H	L	×	Mask write
H	L	H	×	Read transfer
H	L	L	H	Pseudo transfer
H	L	L	L	Write transfer
L	×	×	×	CBR refresh

Note: ×; Don't care.

$\overline{CAS}$ (input pin): Column address is put into chip at the falling edge of $\overline{CAS}$. $\overline{CAS}$ controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of $\overline{RAS}$. Column address is determined by A0–A8 level at the falling edge of $\overline{CAS}$. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

$\overline{WE}$ (input pin): $\overline{WE}$ pin has two functions at the falling edge of $\overline{RAS}$ and after. When $\overline{WE}$ is low at the falling edge of $\overline{RAS}$, the HM534251 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. ($\overline{WE}$ level at the falling edge of $\overline{RAS}$ is don't care in read cycle.) When $\overline{WE}$ is high at the falling edge of $\overline{RAS}$, a normal write cycle is executed. After that, $\overline{WE}$ switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by $\overline{WE}$ level at the falling edge of $\overline{RAS}$. When $\overline{WE}$ is low, data is transferred from SAM to RAM (data is written into RAM), and when $\overline{WE}$ is high, data

is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O3 (input/output pins): I/O pins function as mask data at the falling edge of RAS (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data is output from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534251

Operation of RAM Port

RAM Read Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data is output through I/O pin. At the falling edge of $\overline{RAS}$, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle (Early Write, Delayed Write, Read-Modify-Write)

($\overline{DT}/\overline{OE}$ high, CAS high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle
  ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore, address access time

(t_{AA}), $\overline{RAS}$ to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Transfer Operation

The HM534251 provides the read transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
   (a) Read transfer cycle: RAM → SAM
   (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
   Read transfer cycle: SI/O output
   Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by setting $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512x4 bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can execute SAM access serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH}(min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see figure 1).

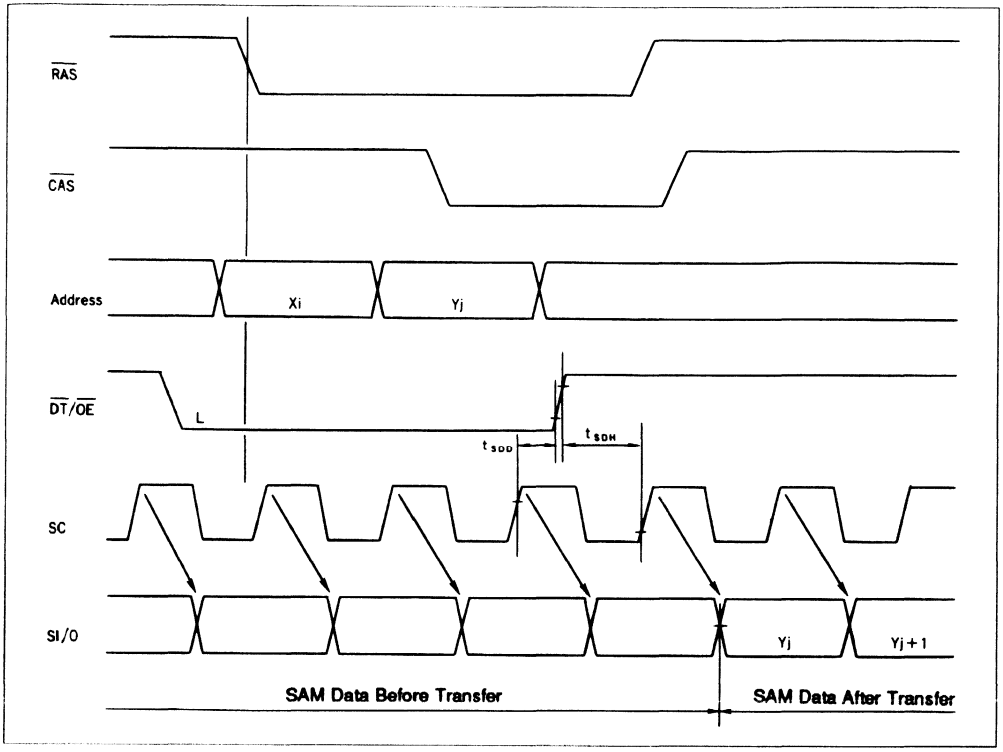


Figure 1. Real Time Read Transfer

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of $\overline{RAS}$)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of RAS. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data resister. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating $\overline{RAS}$ when $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	−1.0 to +7.0	V
Power supply voltage *1	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Note: *1. Relative to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	–	6.5	V
Input low voltage *1	V_{IL}	−0.5*2	–	0.8	V

Notes: *1. All voltages referenced to V_{SS}.
*2. −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Item	Symbol	HM534251-10 Min	HM534251-10 Max	HM534251-11 Min	HM534251-11 Max	HM534251-12 Min	HM534251-12 Max	HM534251-15 Min	HM534251-15 Max	Unit	Test Conditions: RAM port	Test Conditions: SAM port	Note
Operating current	I_{CC1}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC7}	—	120	—	120	—	100	—	85	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	*1, *2
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC8}	—	65	—	55	—	55	—	40	mA		$\overline{SE}$=V_{IL}, SC cycling t_{SCC} = Min	*1, *4
$\overline{RAS}$-only refresh current	I_{CC3}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ =V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC9}	—	120	—	120	—	100	—	85	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	*2
Page mode current	I_{CC4}	—	80	—	80	—	70	—	60	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC10}	—	130	—	130	—	110	—	90	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	*1, *3
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	60	—	60	—	50	—	40	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	
Data transfer current	I_{CC6}	—	95	—	95	—	90	—	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC12}	—	135	—	135	—	125	—	115	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling t_{SCC} = Min	*2
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA			
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA			
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: *1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while one $\overline{RAS}$ cycle.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
*4. Address must be fixed.

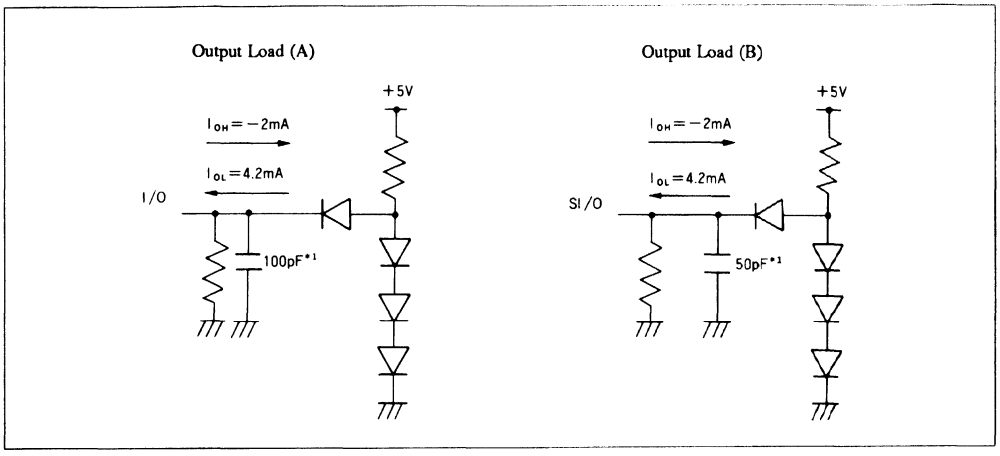
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics (Ta = 0 to 70°C, Vcc = 5 V ± 10%, Vss = 0 V) *1, *11

Test Conditions

Input rise and fall time:	5 ns
Output load:	See figures
Input timing reference levels:	0.8 V, 2.4 V
Output timing reference levels:	0.4 V, 2.4 V



Note: *1. Including scope & jig.

Common Parameter

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	tRC	190	—	190	—	220	—	260	—	ns	
RAS precharge time	tRP	80	—	80	—	90	—	100	—	ns	
RAS pulse width	tRAS	100	10000	100	10000	120	10000	150	10000	ns	
CAS pulse width	tCAS	30	10000	30	10000	35	10000	40	10000	ns	
Row address setup time	tASR	0	—	0	—	0	—	0	—	ns	
Row address hold time	tRAH	15	—	15	—	15	—	20	—	ns	
Column address setup time	tASC	0	—	0	—	0	—	0	—	ns	
Column address hold time	tCAH	20	—	20	—	20	—	25	—	ns	
RAS to CAS delay time	tRCD	25	70	25	70	25	85	30	110	ns	*5, *6
RAS hold time	tRSH	30	—	30	—	35	—	40	—	ns	
CAS hold time	tCSH	100	—	100	—	120	—	150	—	ns	
CAS to RAS precharge time	tCRP	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	tT	3	50	3	50	3	50	3	50	ns	*8
Refresh period	tREF	—	8	—	8	–	8	—	8	ms	
DT to RAS setup time	tDTS	0	—	0	—	0	—	0	—	ns	
DT to RAS hold time	tDTH	15	—	15	—	15	—	20	—	ns	
Data-in to OE delay time	tDZO	0	—	0	—	0	—	0	—	ns	
Data-in to CAS delay time	tDZC	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	*3, *6
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	*7
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	*7
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	*12
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	*12
$\overline{RAS}$ to column address delay time	t_{RAD}	20	55	20	55	20	65	25	80	ns	*5, *6
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100	—	100	—	100	—	100	µs	

Write Cycle (RAM), Page Mode Write Cycle

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	*9
Write command hold time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100	—	100	—	100	—	100	µs	

Read-Modify-Write Cycle

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ pulse width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	*9
Column address to $\overline{WE}$ delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	*9
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	*3,*5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	*3,*6
$\overline{RAS}$ to column address delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	*5,*6
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask data to RAS setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to RAS hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
RAS precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to $\overline{SC}$ delay time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
$\overline{SC}$ to $\overline{RAS}$ setup time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
$\overline{DT}$ hold time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
$\overline{DT}$ hold time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last $\overline{SC}$ to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First $\overline{SC}$ to $\overline{DT}$ hold time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ lead time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
$\overline{DT}$ hold time referenced to $\overline{RAS}$ high	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial data input to $\overline{RAS}$ delay time	t_{SZR}	—	10	—	10	—	10	—	10	ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	*7
$\overline{RAS}$ to Sout (Low-Z) delay time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial clock cycle time	t_{SCC}	40	—	40	—	40	—	60	—	ns	*13
Access time from $\overline{SC}$	t_{SCA}	—	30	—	35	–	40	—	50	ns	*4
Serial data out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	*4
$\overline{SC}$ pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
$\overline{SC}$ precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access time from $\overline{SC}$	t_{SCA}	—	30	—	35	—	40	—	50	ns	*4
Access time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	*4
Serial data-out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	*4
$\overline{SC}$ pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
$\overline{SC}$ precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	*7

Serial Write Cycle

Item	Symbol	HM534251-10		HM534251-11		HM534251-12		HM534251-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial write enable hold time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

Notes:

*1. AC measurements assume t_T = 5 ns.

*2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

*4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.

*5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.

*6. When $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max), access time is specified by t_{AA}.

*7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200 mV, V_{OL} + 200 mV).

*8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

*9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition.
When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.

*10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.

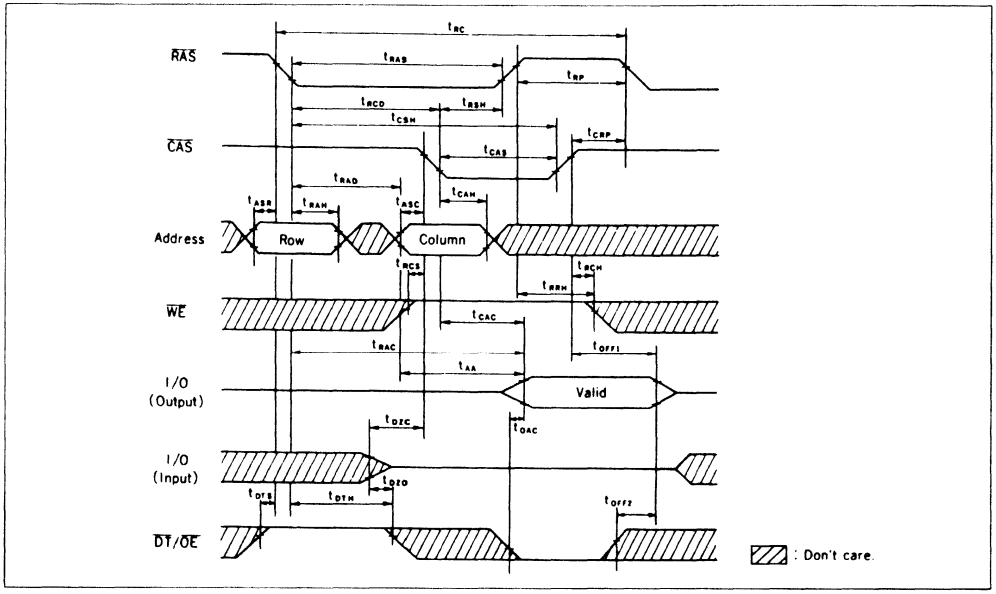
*11. After power-up, pause for 100 µs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.

*12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.

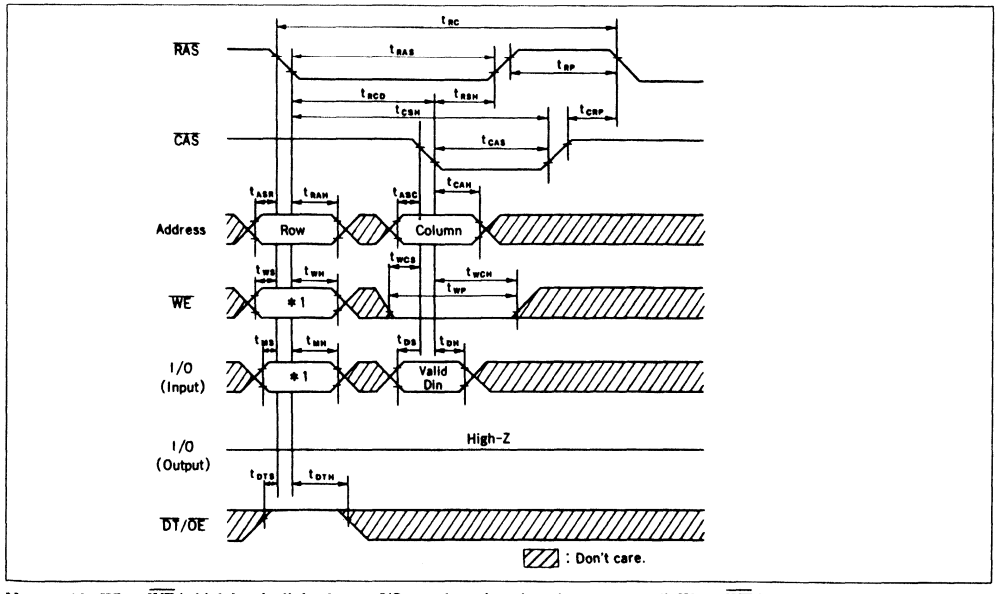
*13. tSCC is applied to the last SAM access cycle of read transfer cycle-1 before transfer.

Timing Waveforms

Read Cycle

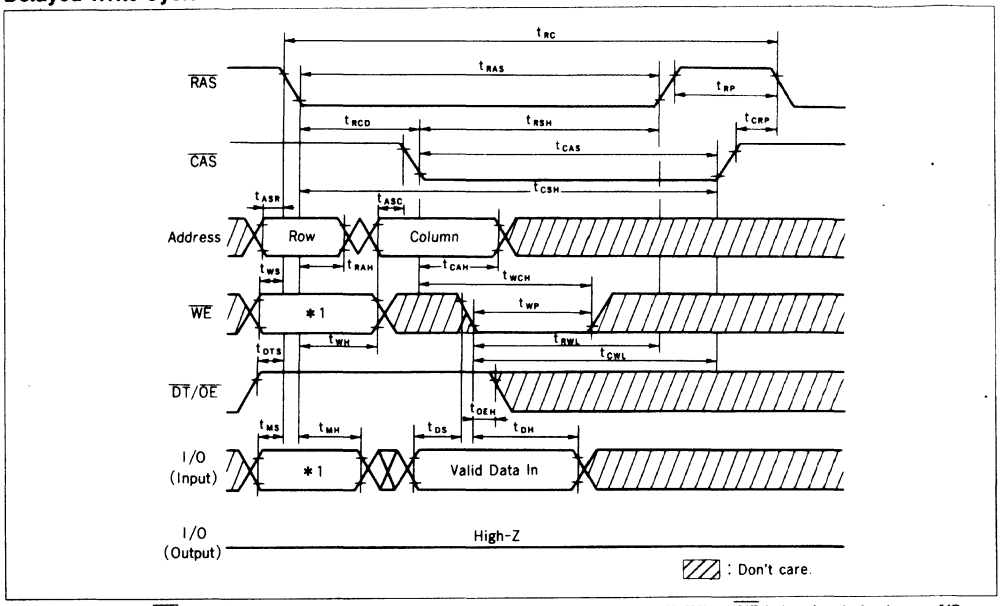


Early Write Cycle



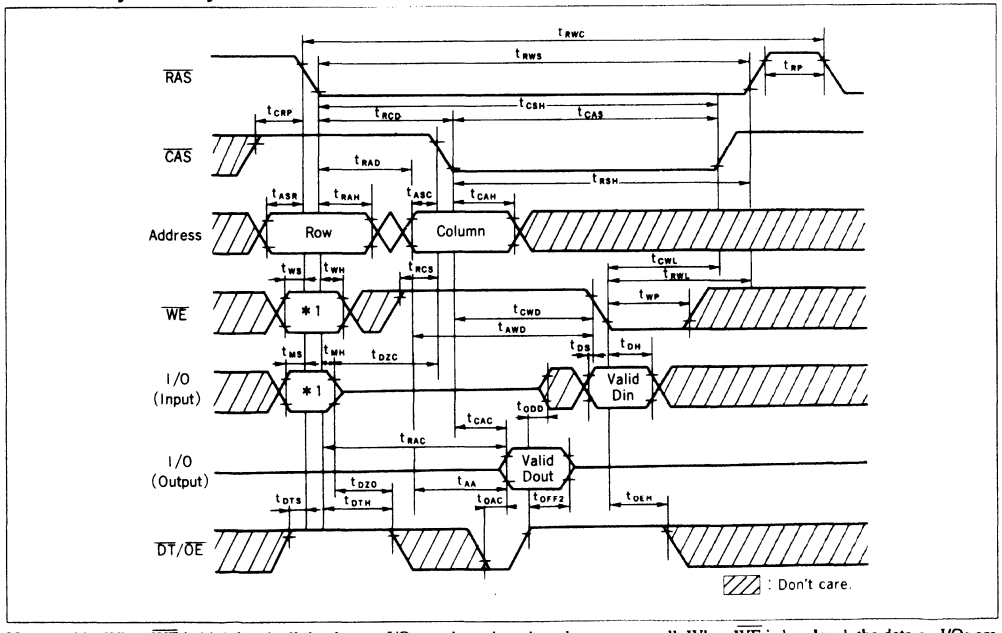
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



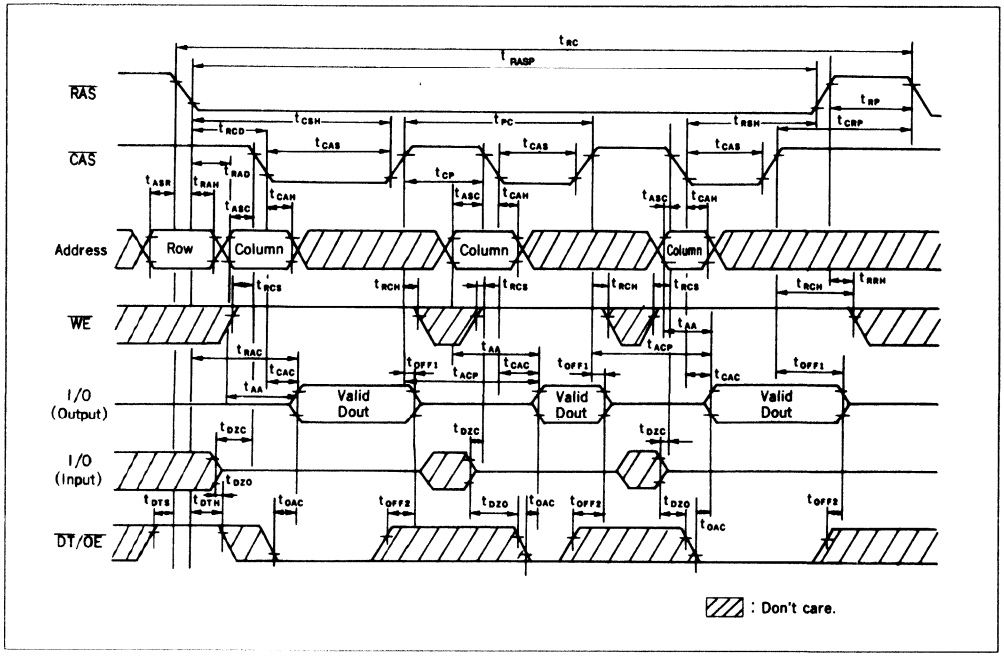
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

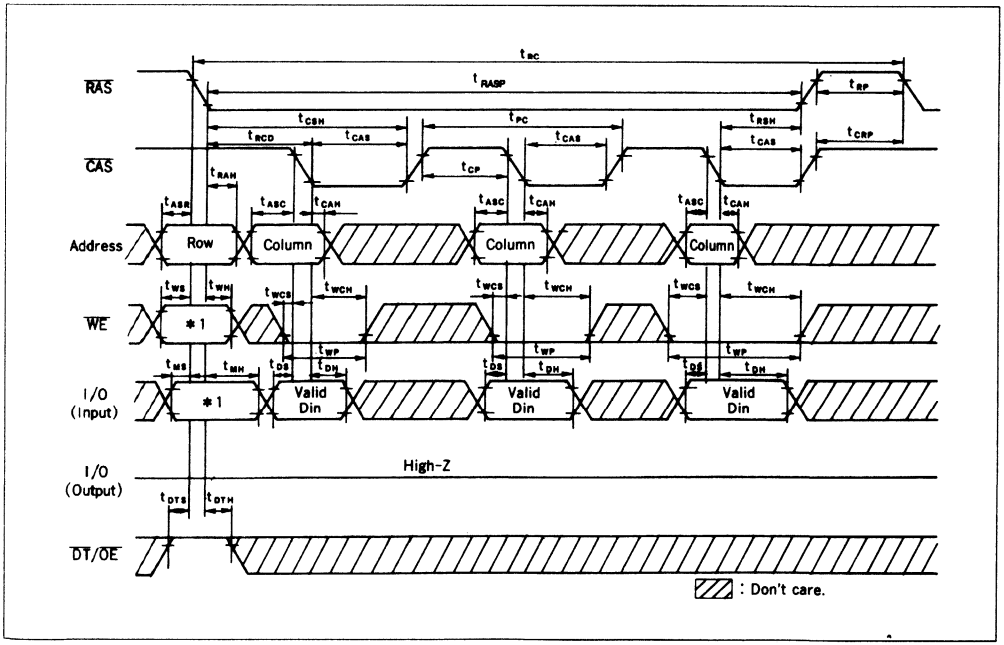


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

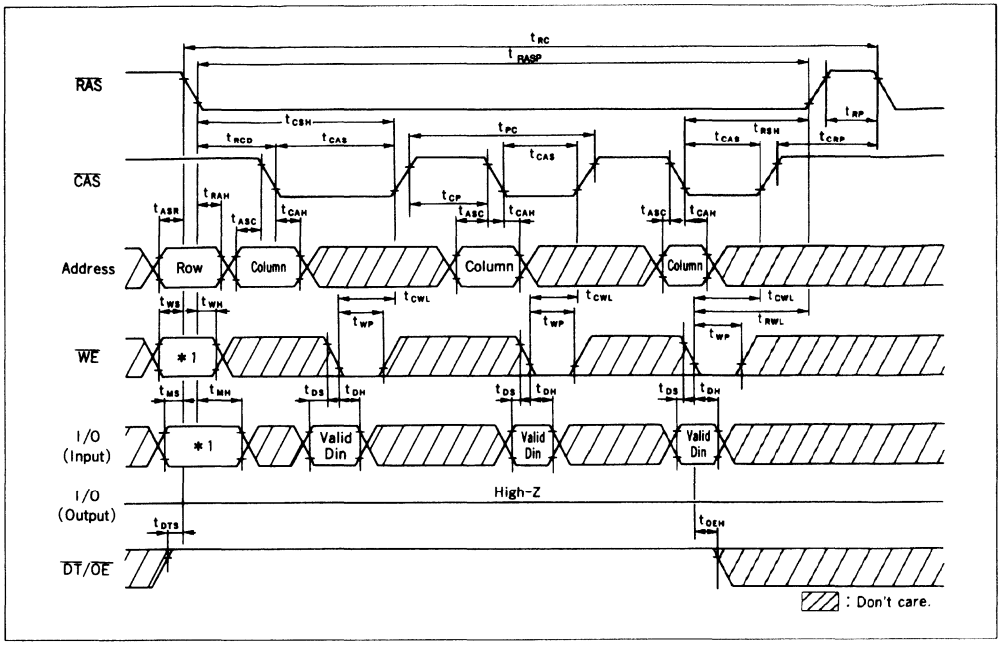


Page Mode Write Cycle (Early Write)



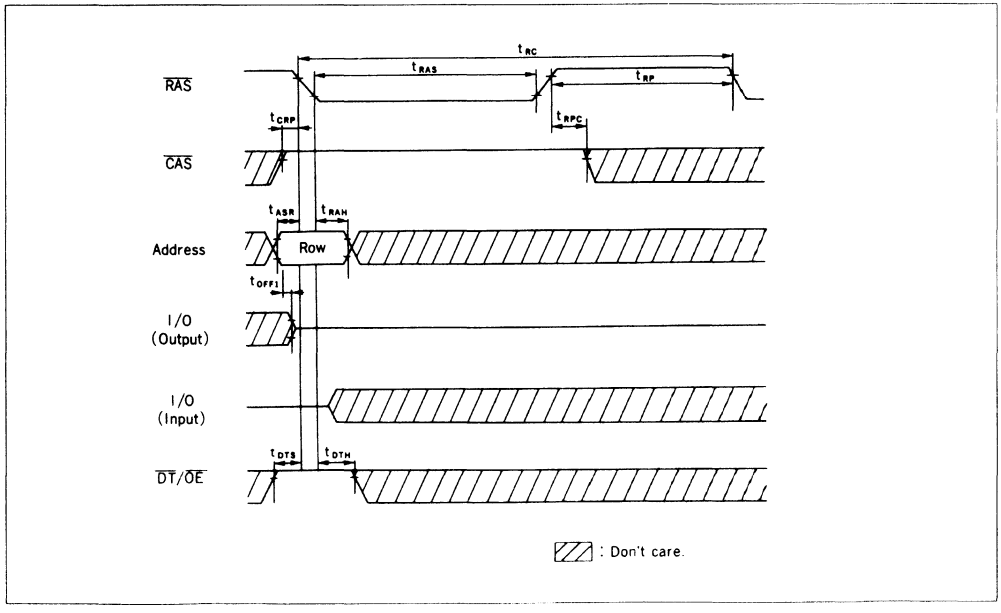
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

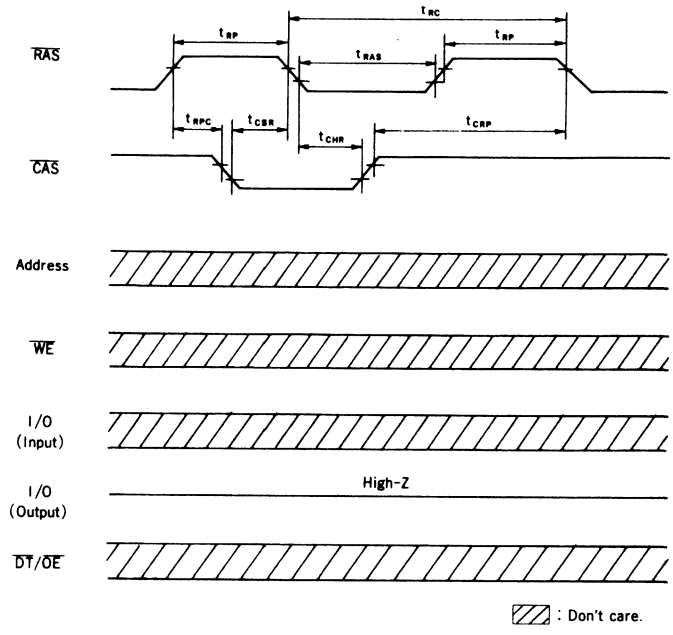


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

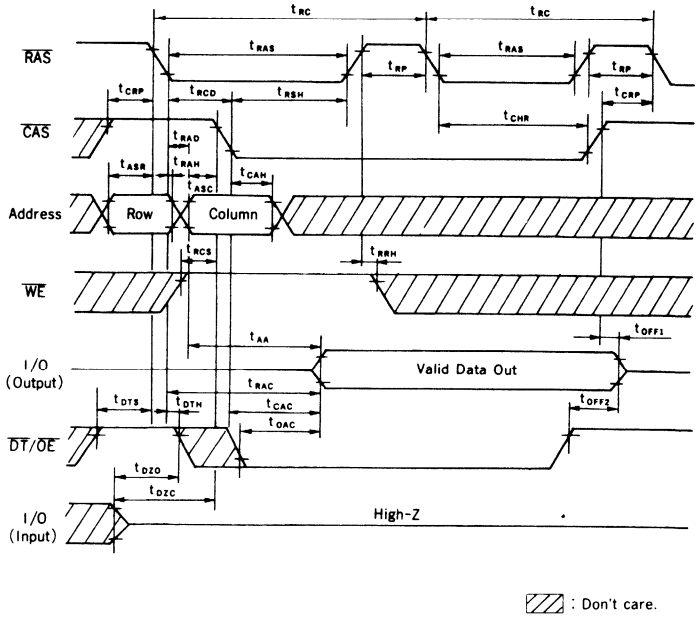
$\overline{RAS}$-Only Refresh Cycle



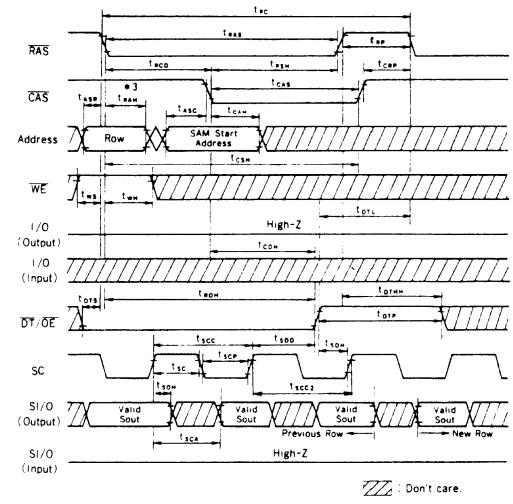
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle

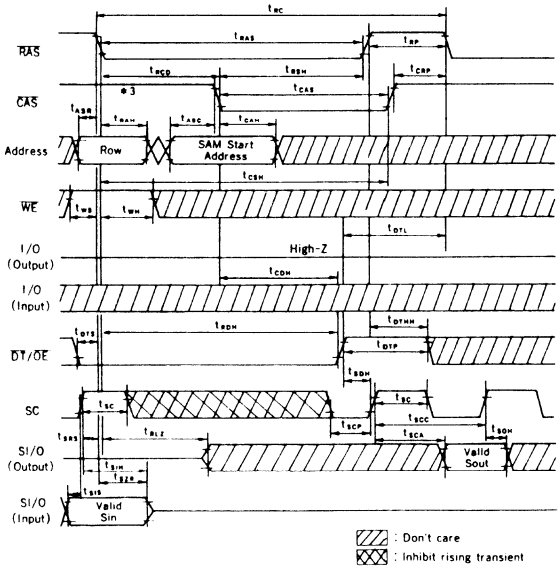


Read Transfer Cycle (1)*1,*2



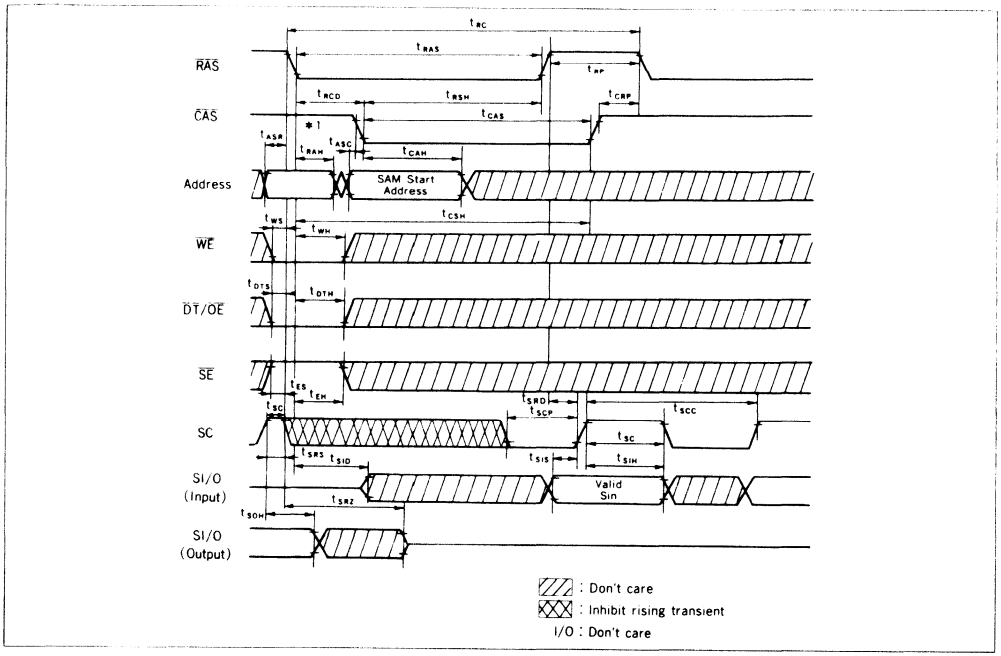
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

Read Transfer Cycle (2)*1,*2

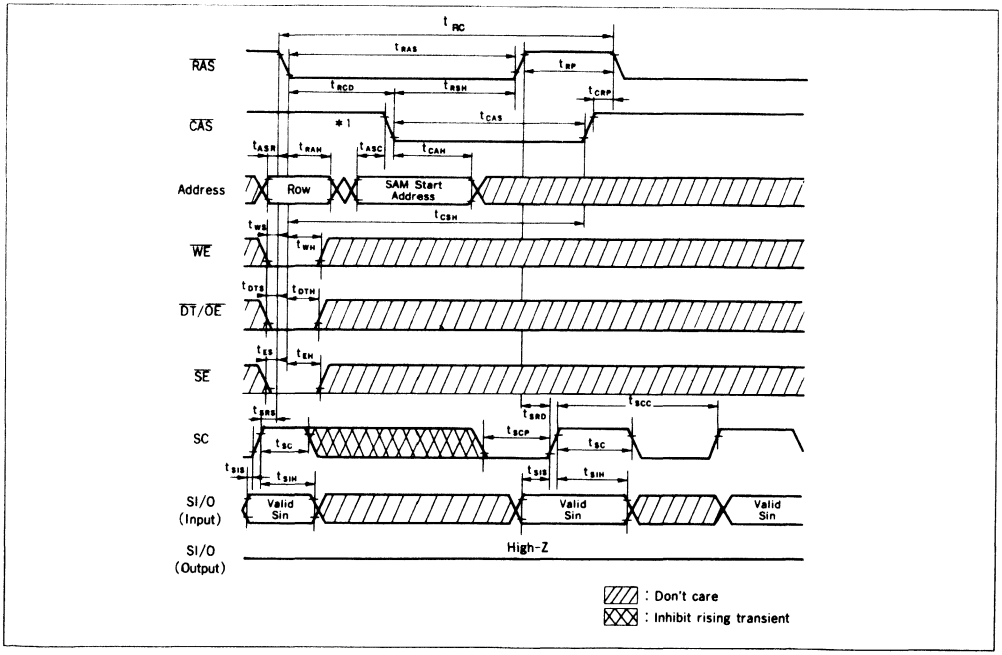


Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

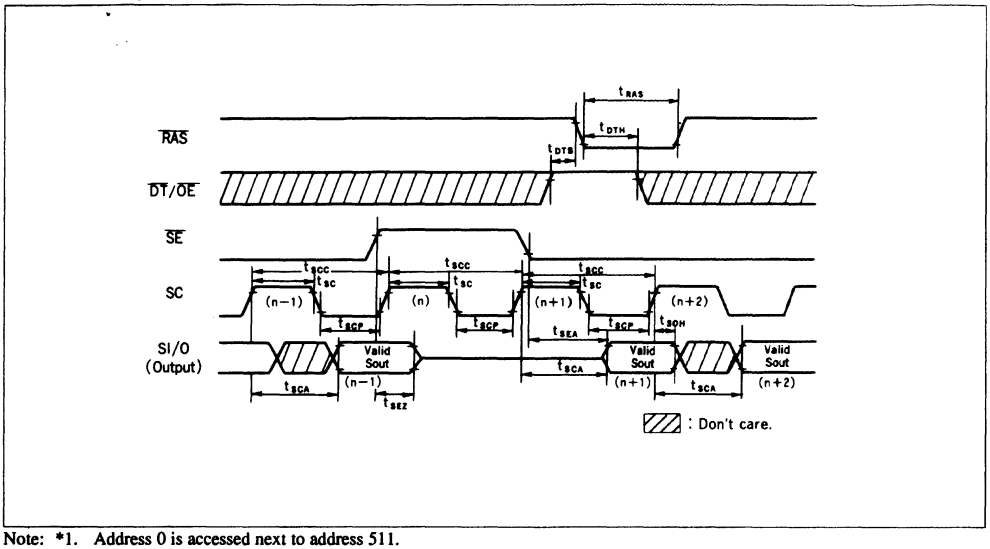
Pseudo Transfer Cycle



Write Transfer Cycle

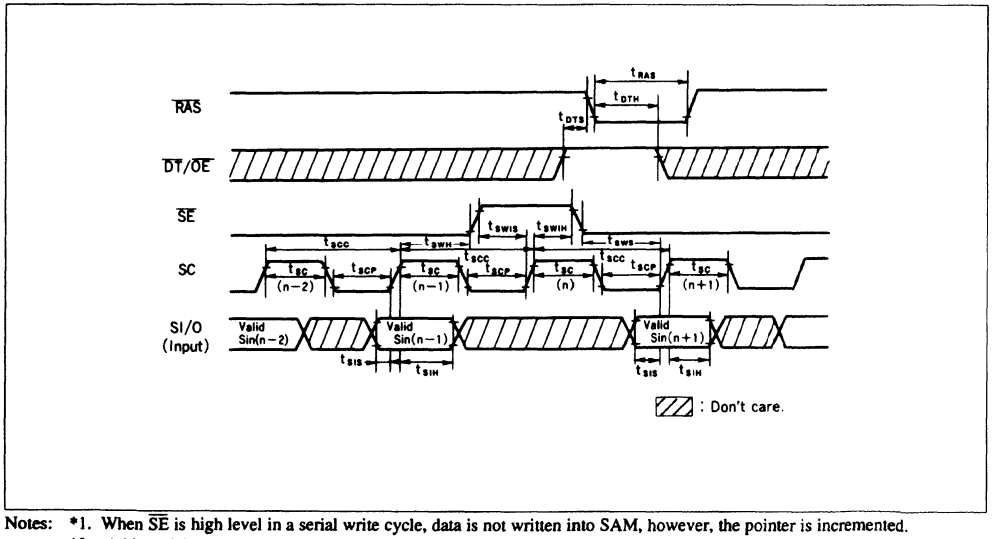


Serial Read Cycle



Note: *1. Address 0 is accessed next to address 511.

Serial Write Cycle



Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

HM534252 Series

262144-Word × 4-Bit Multiport CMOS Video RAM

The HM534252 is a 1-Mbit multiport video RAM equipped with a 256-kword x 4-bit dynamic RAM and a 512-word x 4-bit SAM (serial access memory).

Its RAM and SAM operate independently and asynchronously. It can transfer data between RAM and SAM and has a write mask function.

It also provides logic operation mode to simplify its operation. In this mode, logic operation between memory data and input data can be executed by using internal logic-arithmetic unit.

Features

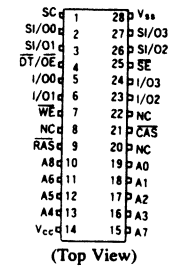
- Multiport organization
  - Asynchronous and simultaneous operation of RAM and SAM capability
  - RAM: 256-kword x 4-bit and SAM: 512-word x 4-bit
- Access time RAM: 100 ns/100 ns/120 ns/150 ns max
  SAM: 30 ns/35 ns/40 ns/50 ns max
- Cycle time RAM: 190 ns/190 ns/220 ns/260 ns min
  SAM: 30 ns/40 ns/40 ns/60 ns min
- Low power
  - Active RAM: 385 mW max
    SAM: 358 mW max
  - Standby 40 mW max
- High-speed page mode capability
- Logic operation mode capability
- 2 types of mask write mode capability
- Bidirectional data transfer cycle between RAM and SAM capability
- Real time read transfer capability
- 3 variations of refresh (8 ms/512 cycles)
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

Type No.	Access Time	Package
HM534252JP-10	100 ns	400-mil
HM534252JP-11	100 ns	28-pin
HM534252JP-12	120 ns	Plastic SOJ (CP-28D)
HM534252JP-15	150 ns	
HM534252ZP-10	100 ns	400-mil
HM534252ZP-11	100 ns	28-pin
HM534252ZP-12	120 ns	Plastic ZIP (ZP-28)
HM534252ZP-15	150 ns	

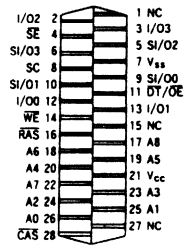
Pin Arrangement

HM534252JP Series



(Top View)

HM534252ZP Series

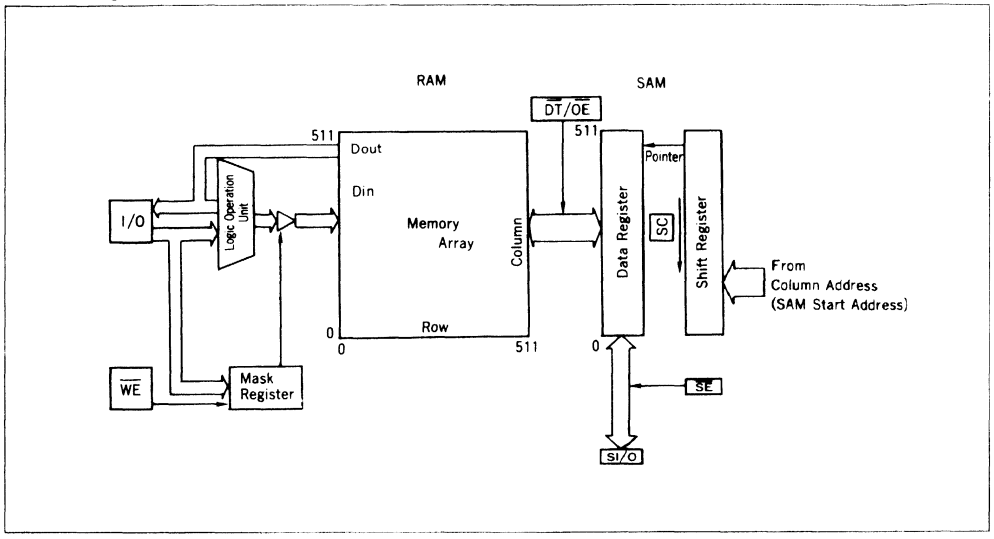


(Bottom View)

Pin Description

Pin Name	Function
A0–A8	Address inputs
I/O0–I/O3	RAM port data inputs/ outputs
SI/O0 – SI/O3	SAM port data inputs/ outputs
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{DT}}/\overline{\text{OE}}$	Data transfer/Output enable
SC	Serial clock
$\overline{\text{SE}}$	SAM port enable
Vcc	Power supply
Vss	Ground
NC	No connection

Block Diagram



Pin Function

RAS (input pin): RAS is a basic RAM signal. It is active in low level and standby in high level. Row address and signals as shown in table 1 are input at the falling edge of RAS. The input level of those signals determine the operation cycle of the HM534252.

Table 1. Operation Cycles of the HM534252

Input level at the falling edge of RAS				Operation Cycle
CAS	DT/OE	WE	SE	
H	H	H	×	RAM read/write
H	H	L	×	Mask write
H	L	H	×	Read transfer
H	L	L	H	Pseudo transfer
H	L	L	L	Write transfer
L	×	H	×	CBR refresh
L	×	L	×	Logic operation set/reset

Note: ×; Don't care.

CAS (input pin): Column address is put into chip at the falling edge of CAS. CAS controls output impedance of I/O in RAM.

A0–A8 (input pins): Row address is determined by A0–A8 level at the falling edge of RAS. Column address is determined by A0–A8 level at the falling edge of CAS. In transfer cycles, row address is the address on the word line which transfers data with SAM data register, and column address is the SAM start address after transfer.

WE (input pin): WE pin has two functions at the falling edge of RAS and after. When WE is low at the falling edge of RAS, the HM534252 turns to mask write mode. According to the I/O level at the time, write on each I/O can be masked. (WE level at the falling edge of RAS is don't care in read cycle.) When WE is high at the falling edge of RAS, a normal write cycle is executed. After that, WE switches read/write cycles as in a standard DRAM. In a transfer cycle, the direction of transfer is determined by WE level at the falling edge of RAS. When WE is low, data is transferred from SAM to RAM

(data is written into RAM), and when $\overline{WE}$ is high, data is transferred from RAM to SAM (data is read from RAM).

I/O0–I/O3 (input/output pins): I/O pins function as mask data at the falling edge of $\overline{RAS}$ (in mask write mode). Data is written only on high I/O pins. Data on low I/O pins are masked and internal data are retained. After that, they function as input/output pins as those of a standard DRAM.

$\overline{DT}/\overline{OE}$ (input pin): $\overline{DT}/\overline{OE}$ pin functions as $\overline{DT}$ (data transfer) pin at the falling edge of $\overline{RAS}$ and as $\overline{OE}$ (output enable) pin after that. When $\overline{DT}$ is low at the falling edge of $\overline{RAS}$, this cycle becomes a transfer cycle. When $\overline{DT}$ is high at the falling edge of $\overline{RAS}$, RAM and SAM operate independently.

SC (input pin): SC is a basic SAM clock. In a serial read cycle, data outputs from an SI/O pin synchronously with the rising edge of SC. In a serial write cycle, data on an SI/O pin at the rising edge of SC is put into the SAM data register.

$\overline{SE}$ (input pin): $\overline{SE}$ pin activates SAM. When $\overline{SE}$ is high, SI/O is in the high impedance state in serial read cycle and data on SI/O is not put into the SAM data register in serial write cycle. $\overline{SE}$ can be used as a mask for serial write because internal pointer is incremented at the rising edge of SC.

SI/O0–SI/O3 (input/output pins): SI/Os are input/output pins in SAM. Direction of input/output is determined by the previous transfer cycle. When it was a read transfer cycle, SI/O outputs data. When it was a pseudo transfer cycle or write transfer cycle, SI/O inputs data.

Operation of HM534252

Operation of RAM Port

RAM Read Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high, at the falling edge of $\overline{RAS}$)

Row address is entered at the $\overline{RAS}$ falling edge and column address at the $\overline{CAS}$ falling edge to the device as in standard DRAM. Then, when $\overline{WE}$ is high and $\overline{DT}/\overline{OE}$ is low while $\overline{CAS}$ is low, the selected address data outputs through I/O pin. At the falling edge of RAS, $\overline{DT}/\overline{OE}$ and $\overline{CAS}$ become high to distinguish RAM read cycle from transfer cycle and CBR refresh cycle. Address access time (t_{AA}) and $\overline{RAS}$ to column address delay time (t_{RAD}) specifications are added to enable high-speed page mode.

RAM Write Cycle

(Early Write, Delayed Write, Read-Modify-Write)

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

- Normal Mode Write Cycle
  ($\overline{WE}$ high at the falling edge of $\overline{RAS}$)

When $\overline{CAS}$ and $\overline{WE}$ are set low after $\overline{RAS}$ is set low, a write cycle is executed and I/O data is written at the selected addresses. When all 4 I/Os are written, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$ to distinguish normal mode from mask write mode.

If $\overline{WE}$ is set low before the $\overline{CAS}$ falling edge, this cycle becomes an early write cycle and I/O becomes high impedance. Data is entered at the $\overline{CAS}$ falling edge.

If $\overline{WE}$ is set low after the $\overline{CAS}$ falling edge, this cycle becomes a delayed write cycle. Data is input at the $\overline{WE}$ falling edge. I/O does not become high impedance in this cycle, so data should be entered with $\overline{OE}$ in high.

If $\overline{WE}$ is set low after t_{CWD} (min) and t_{AWD} (min) after the $\overline{CAS}$ falling edge, this cycle becomes a read-modify-write cycle and enables write after read to execute in the same address cycle. In this cycle also, to avoid I/O contention, data should be input after reading data and setting $\overline{OE}$ high.

- Mask Write Mode ($\overline{WE}$ low at the falling edge of $\overline{RAS}$)

If $\overline{WE}$ is set low at the falling edge of $\overline{RAS}$, the cycle becomes a mask write mode cycle which writes only to selected I/O. Whether or not an I/O is written depends on I/O level (mask data) at the falling edge of $\overline{RAS}$. Then the data is written in high I/O pins and masked in low ones and internal data is preserved. This mask data is effective during the $\overline{RAS}$ cycle. So, in high-speed page mode cycle, the mask data is preserved during the page access.

High-Speed Page Mode Cycle

($\overline{DT}/\overline{OE}$ high, $\overline{CAS}$ high at the falling edge of $\overline{RAS}$)

High-speed page mode cycle reads/writes the data of the same row address at high speed by toggling $\overline{CAS}$ while $\overline{RAS}$ is low. Its cycle time is one third of the random read/write cycle and is higher than the standard page mode cycle by 70–80%. This product is based on static column mode, therefore address access time (t_{AA}), $\overline{RAS}$

to column address delay time (t_{RAD}), and access time from $\overline{CAS}$ precharge (t_{ACP}) are added. In one $\overline{RAS}$ cycle, 512-word memory cells of the same row address can be accessed. It is necessary to specify access frequency within t_{RASP} max (100 µs).

Transfer Operation

The HM534252 provides the transfer cycle, pseudo transfer cycle, and write transfer cycle as data transfer cycles. These transfer cycles are set by driving $\overline{DT}/\overline{OE}$ low at the falling edge of $\overline{RAS}$.

They have following functions:

(1) Transfer data between row address and SAM data register (except for pseudo transfer cycle)

(2) Determine direction of data transfer
   (a) Read transfer cycle: RAM → SAM
   (b) Write transfer cycle: RAM ← SAM

(3) Determine input or output of SAM I/O pin (SI/O)
   Read transfer cycle: SI/O output
   Pseudo transfer cycle, write transfer cycle: SI/O input

(4) Determine first SAM address to access (SAM start address) after transferring at column address.

Read Transfer Cycle ($\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, WE high at the falling edge of $\overline{RAS}$)

This cycle becomes read transfer cycle by driving $\overline{DT}/\overline{OE}$ low and $\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address data (512x4 bit) determined by this cycle is transferred synchronously at the rising edge of $\overline{DT}/\overline{OE}$. After the rising edge of $\overline{DT}/\overline{OE}$, the new address data outputs from SAM start address determined by column address.

This cycle can access SAM serially even during transfer (real time read transfer). In this case, the timing t_{SDD} (min) is specified between the last SAM access before transfer and $\overline{DT}/\overline{OE}$ rising edge, and t_{SDH}(min) between the first SAM access and $\overline{DT}/\overline{OE}$ rising edge (see figure 1).

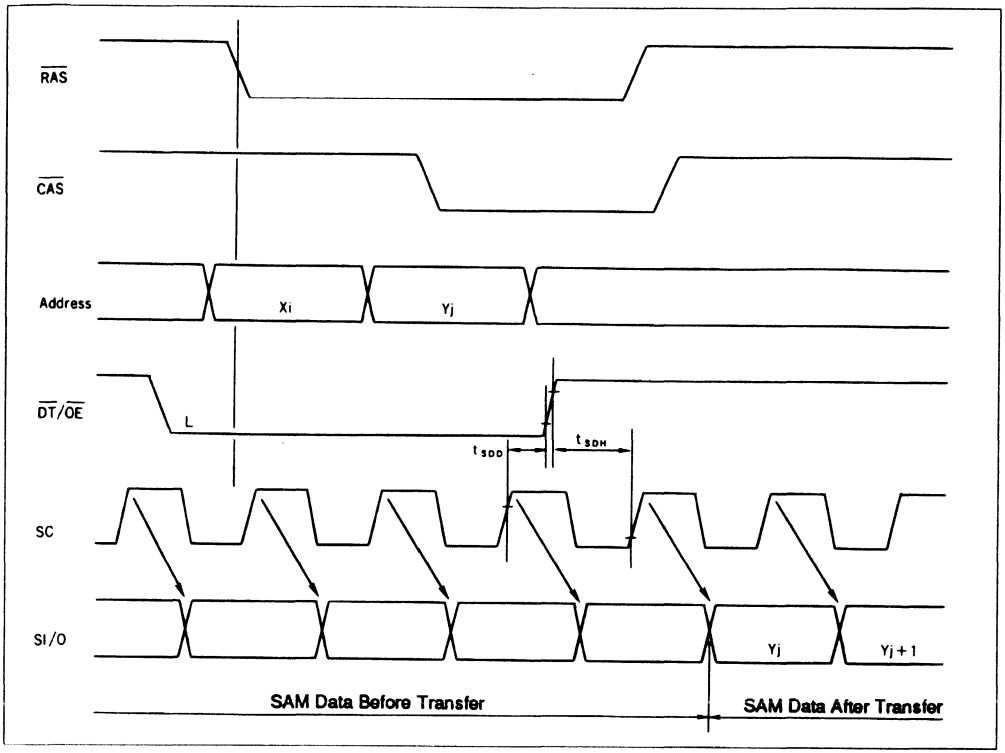


Figure 1. Real Time Read Transfer

If read transfer cycle is executed, SI/O becomes output state. When the previous transfer cycle is either pseudo transfer cycle or write transfer cycle and SI/O is in input state, uncertain data outputs after t_{RLZ} (min) after the $\overline{RAS}$ falling edge. Before that, input should be set high impedance to avoid data contention.

Pseudo Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high at the falling edge of RAS)

Pseudo transfer cycle is available for switching SI/O from output state to input state because data in RAM isn't rewritten. This cycle starts when $\overline{CAS}$ is high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ high, at the falling edge of $\overline{RAS}$. The output buffer in SI/O becomes high impedance within t_{SRZ} (max) from the $\overline{RAS}$ falling edge. Data should be input to SI/O later than t_{SID} (min) to avoid data contention. SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. In this cycle, SAM access is inhibited during $\overline{RAS}$ low, therefore, SC should not be raised.

Write Transfer Cycle ($\overline{CAS}$ high, $\overline{DT/OE}$ low, $\overline{WE}$ low, and $\overline{SE}$ low at the falling edge of $\overline{RAS}$)

Write transfer cycle can transfer a row of data input by serial write cycle to RAM. The row address of data transferred into RAM is determined by the address at the falling edge of $\overline{RAS}$. The column address is specified as the first address to serial write after terminating this cycle. Also in this cycle, SAM access becomes enabled after t_{SRD} (min) after $\overline{RAS}$ becomes high. SAM access is inhibited during $\overline{RAS}$ low. In this period, SC should not be raised.

SAM Port Operation

Serial Read Cycle

SAM port is in read mode when the previous data transfer cycle is read transfer cycle. Access is synchronized with SC rising, and SAM data is output from SI/O. If $\overline{SE}$ is set high SI/O becomes high impedance and internal pointer is incremented at the SC rising edge.

Serial Write Cycle

If previous data transfer cycle is pseudo transfer cycle or write transfer cycle, SAM port goes into write mode. In this cycle, SI/O data is programmed into data register at the SC rising edge like in the serial read cycle. If $\overline{SE}$ is high, SI/O data isn't input into data resister. Internal pointer is incremented according to the SC rising edge, so $\overline{SE}$ high can mask data for SAM.

Refresh

RAM Refresh

RAM, which is composed of dynamic circuits, requires refresh to retain data. Refresh is performed by accessing all 512 row addresses every 8 ms. There are three refresh cycles: (1) $\overline{RAS}$-only refresh cycle, (2) $\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh cycle, and (3) Hidden refresh cycle. Besides them, the cycles which activate $\overline{RAS}$ such as read/write cycles or transfer cycles can refresh the row address. Therefore, no refresh cycle is required for accessing all row addresses every 8 ms.

$\overline{RAS}$-Only Refresh Cycle: $\overline{RAS}$-only refresh cycle is performed by activating only $\overline{RAS}$ cycle with $\overline{CAS}$ fixed to high by inputting the row address (= refresh address) from external circuits. To distinguish this cycle from data transfer cycle, $\overline{DT}/\overline{OE}$ should be high at the falling edge of $\overline{RAS}$.

CBR Refresh Cycle: CBR refresh cycle is set by activating $\overline{CAS}$ before $\overline{RAS}$. In this cycle, refresh address need not to be input through external circuits because it is input through an internal refresh counter. In this cycle, output is in high impedance and power dissipation is lowered because $\overline{CAS}$ circuits don't operate. To distinguish this cycle from logic operation set/reset cycle, $\overline{WE}$ should be high at the falling edge of $\overline{RAS}$.

Hidden Refresh Cycle: Hidden refresh cycle performs refresh by reactivating RAS when DT/OE and CAS keep low in normal RAM read cycles.

SAM Refresh

SAM parts (data register, shift register, selector), organized as fully static circuitry, don't require refresh.

Logic Operation Mode

The HM534252 supports logic operation capability on RAM port. It performs logic operations between the memory cell data and input data in logic operation mode cycle, and writes the result into the memory cell (read modify write). This function realizes high speed raster operations and simplifies peripheral circuits for raster operations.

Logic Operation Set/Reset Cycle ($\overline{CAS}$ and $\overline{WE}$ Low at the falling edge of $\overline{RAS}$)

In logic operation set/reset cycle, the following operations are performed at the same time; 1. Selection of logic operations and logic operation mode set/reset, 2. Mask data programming, 3. $\overline{CAS}$-before-$\overline{RAS}$ refresh.

Figure 2 shows the timing for logic operation set/reset cycle. This cycle starts when $\overline{CAS}$ and $\overline{WE}$ are low at the falling edge of $\overline{RAS}$. In this cycle, logic operation codes and mask data are programmed by row address and I/O pin at the falling edge of $\overline{RAS}$ respectively. When write cycle is performed after this cycle, the logic operation write cycle starts. In the logic operation mode, the specification of cycle time is longer than that of normal mode because read-modify-write cycle is performed internally. In this cycle, logic operation codes and mask data programmed are available until reprogrammed. In normal mode, mask data is available only for one $\overline{RAS}$ cycle. Here, the mask data programmed in normal mode is named as "temporary mask data" and the one programmed in logic operation set/reset cycle is named as "mask data".

(1) Selection of logic operations and logic operation mode set/reset

Table 2 shows the logic operations. One operation is selected among sixteen ones by combinations of A0-A3 levels at the falling edge of $\overline{RAS}$. (A4–A8 are Don't care.) Logic operation codes (A3, A2, A1, A0) = (0,1,0,1) resets the logic operation mode. When write cycle is performed after that, normal write cycle starts. However, even in this case, mask data is still available. I/O should be at high level at the falling edge of $\overline{RAS}$ in logic operation set/reset cycle when mask data is not used.

(2) Mask data programming

High/low level of I/O at the falling edge of $\overline{RAS}$ functions as mask data. When I/O is high, the data is written in write cycle. When I/O is low, the input data is masked and the same memory cell data remains. Mask data, programmed in this cycle, is available until reprogrammed. It is advantageous when the same mask data continues.

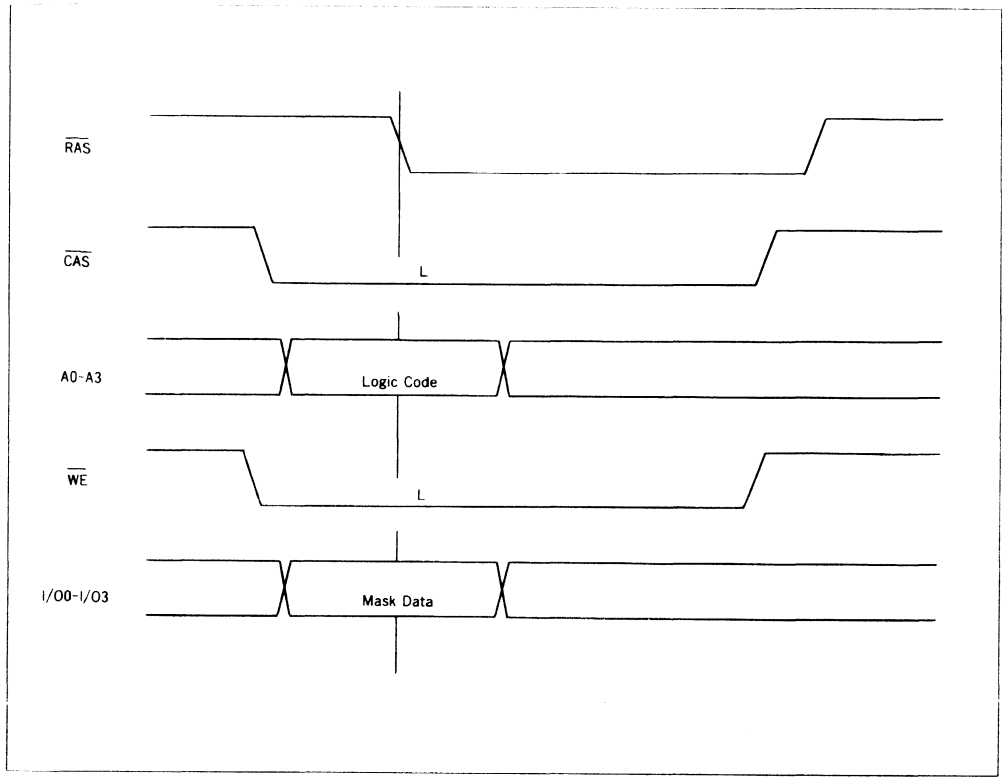


Figure 2. Logic Operation Set/Reset

Table 2. Logic Code

Logic Code				Symbol	Write Data	Note
A3	A2	A1	A0			
0	0	0	0	Zero	0	
0	0	0	1	AND1	$Di \cdot Mi$	
0	0	1	0	AND2	$\overline{Di} \cdot Mi$	Logic operation mode set
0	0	1	1	—	Mi	
0	1	0	0	AND3	$Di \cdot \overline{Mi}$	
0	1	0	1	THROUGH	Di	Logic operation mode reset
0	1	1	0	EOR	$\overline{Di} \cdot Mi + Di \cdot \overline{Mi}$	
0	1	1	1	OR1	$Di + Mi$	
1	0	0	0	NOR	$\overline{Di} \cdot Mi$	
1	0	0	1	ENOR	$Di \cdot Mi + \overline{Di} \cdot \overline{Mi}$	
1	0	1	0	INV1	$\overline{Di}$	Logic operation mode set
1	0	1	1	OR2	$\overline{Di} + Mi$	
1	1	0	0	INV2	$\overline{Mi}$	
1	1	0	1	OR3	$Di + \overline{Mi}$	
1	1	1	0	NAND	$\overline{Di} + \overline{Mi}$	
1	1	1	1	One	1	

Notes: Di; External data-in
Mi; The data of the memory cell

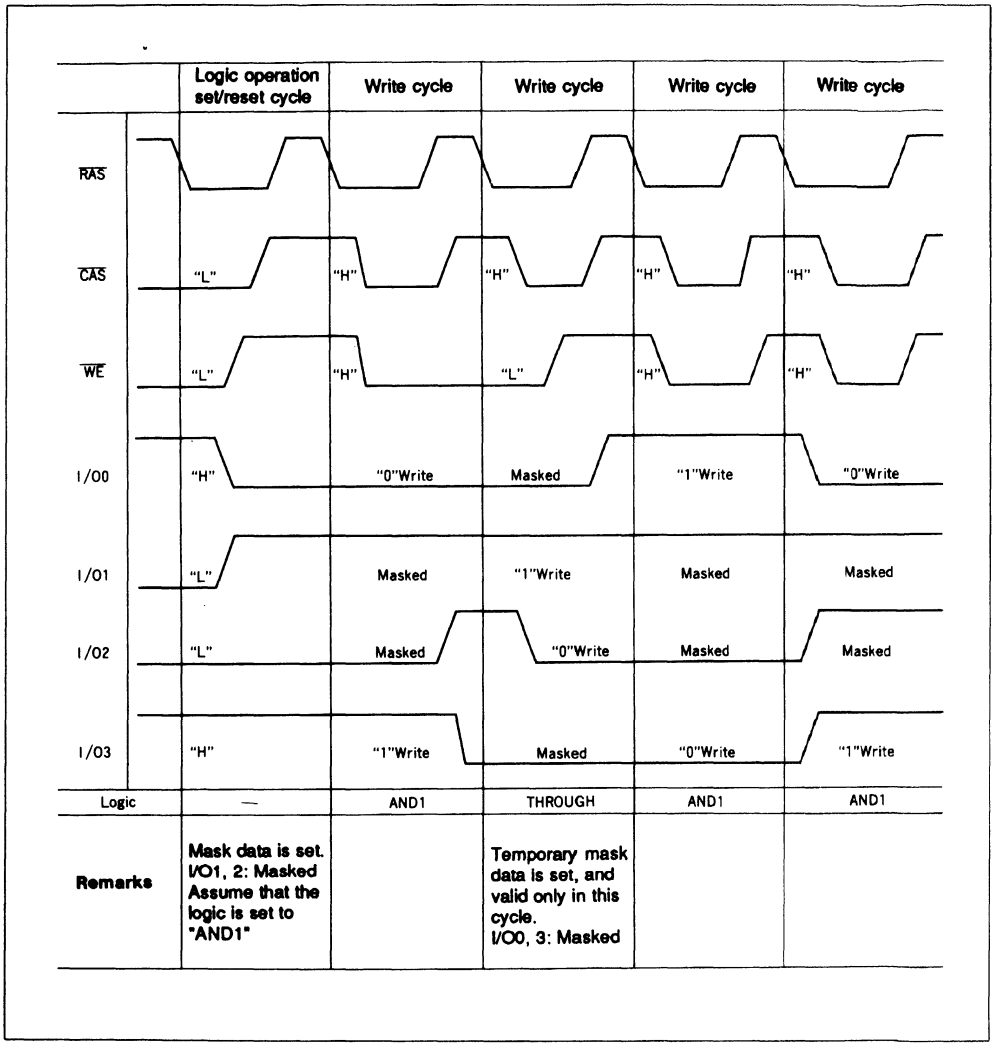


Figure 3. 2 Types of Mask Write Function and Logic Operation Function

Also, temporary mask data is programmed by falling $\overline{WE}$ at the falling edge of $\overline{RAS}$ in logic operation mode cycle after mask data is programmed in logic operation set/reset cycle. In this case, temporary mask data is available only for one cycle.

Logic operation is reset during temporary mask write cycle. It means that external input data is written into I/O when temporary mask data is set. Figure 4 shows write mask and logic operations. These functions are useful when RAM port is devided into frame buffer area and data area, as they save the need to reprogram logic operation codes and mask data.

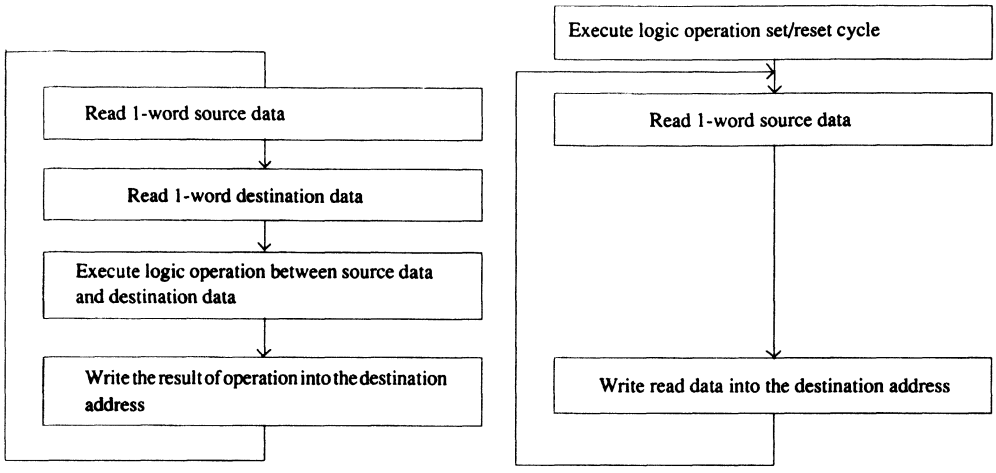
Write Cycle in Logic Operation Mode (Early Write, Delayed Write, Page Mode)

Write cycle after logic operation set cycle is logic operation mode cycle. In this cycle, the following read-modify-write operation is performed internally.

(1) Reading memory data in given address into internal bus.

2) Performing operation between input data and memory data

(3) Writing the result of (2) into address given by (1)



(a) Normal Mode

(b) Logic Operation Mode

Figure 4. Sequence of Raster Operation

Figure 4 shows sequence of raster operation. Raster operation which needs 3 cycles (destination read, operation, destination write) in normal mode can be executed in one write cycle of logic operation mode. It makes raster operation faster and simplifies peripheral hardware for raster operation.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	−1.0 to +7.0	V
Power supply voltage *1	V_{CC}	−0.5 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Note: *1. Relative to Vss.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage *1	V_{CC}	4.5	5.0	5.5	V
Input high voltage *1	V_{IH}	2.4	—	6.5	V
Input low voltage *1	V_{IL}	−0.5*2	—	0.8	V

Notes: *1. All voltages referenced to Vss.
*2. −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM534252-10 Min	HM534252-10 Max	HM534252-11 Min	HM534252-11 Max	HM534252-12 Min	HM534252-12 Max	HM534252-15 Min	HM534252-15 Max	Unit	Test Conditions RAM port	Test Conditions SAM port	Note
Operating current	I_{CC1}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC7}	—	120	—	120	—	100	—	85	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc = Min	*1, *2
Standby current	I_{CC2}	—	7	—	7	—	7	—	7	mA	$\overline{RAS}$,$\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC8}	—	65	—	55	—	55	—	40	mA		$\overline{SE}$ = V_{IL}, SC cycling tscc = Min	*1, *4
$\overline{RAS}$-only refresh current	I_{CC3}	—	70	—	70	—	60	—	55	mA	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC9}	—	120	—	120	—	100	—	85	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc = Min	*2
Page mode current	I_{CC4}	—	80	—	80	—	70	—	60	mA	$\overline{CAS}$ cycling $\overline{RAS}$ = V_{IL}	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC10}	—	130	—	130	—	110	—	90	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc = Min	*1, *3
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC5}	—	60	—	60	—	50	—	40	mA	$\overline{RAS}$ cycling t_{RC} = Min	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC11}	—	110	—	110	—	90	—	70	mA		$\overline{SE}$ = V_{IL}, SC cycling tscc = Min	
Data transfer current	I_{CC6}	—	95	—	95	—	90	—	85	mA	$\overline{RAS}$, $\overline{CAS}$ cycling	SC = V_{IL}, $\overline{SE}$ = V_{IH}	
	I_{CC12}	—	135	—	135	—	125	—	115	mA	t_{RC} = Min	$\overline{SE}$ = V_{IL}, SC cycling tscc = Min	*2
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	µA			
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	µA			
Output high voltage	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V	I_{OH} = −2 mA		
Output low voltage	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V	I_{OL} = 4.2 mA		

Notes: *1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while one $\overline{RAS}$ cycle.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
*4. Address must be fixed.

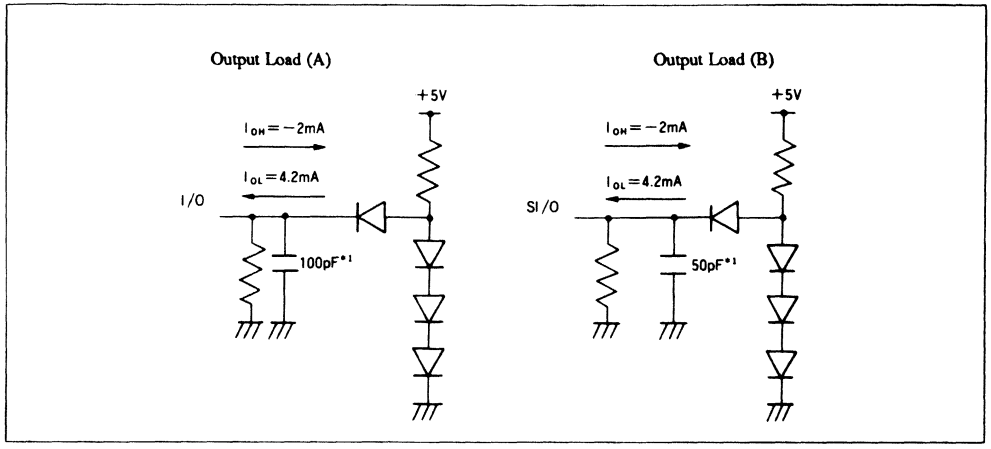
Capacitance (Ta = 25°C, V_{CC} = 5 V, f = 1MHz, Bias: Clock, I/O = V_{CC}, address = V_{SS})

Item	Symbol	Min	Typ	Max	Unit
Address	C_{I1}	—	—	5	pF
Clock	C_{I2}	—	—	5	pF
I/O, SI/O	$C_{I/O}$	—	—	7	pF

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *11

Test Conditions

Input rise and fall time:	5 ns
Output load:	See figures
Input timing reference levels:	0.8 V, 2.4 V
Output timing reference levels:	0.4 V, 2.4 V



Note: *1. Including scope & jig.

Common Parameter

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	190	—	190	—	220	—	260	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	80	—	80	—	90	—	100	—	ns	
$\overline{RAS}$ pulse width t	t_{RAS}	100	10000	100	10000	120	10000	150	10000	ns	
$\overline{CAS}$ pulse width t	t_{CAS}	30	10000	30	10000	35	10000	40	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	15	—	20	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	70	25	70	25	85	30	110	ns	*5,*6
$\overline{RAS}$ hold time	t_{RSH}	30	—	30	—	35	—	40	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	—	100	—	120	—	150	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Transition time (rise to fall)	t_T	3	50	3	50	3	50	3	50	ns	*8
Refresh period	t_{REF}	—	8	—	8	—	8	–	8	ms	
$\overline{DT}$ to $\overline{RAS}$ setup time	t_{DTS}	0	—	0	—	0	—	0	—	ns	
$\overline{DT}$ to $\overline{RAS}$ hold time	t_{DTH}	15	—	15	—	15	—	20	—	ns	
Data-in to $\overline{OE}$ delay time	t_{DZO}	0	—	0	—	0	—	0	—	ns	
Data–in to $\overline{CAS}$ delay time	t_{DZC}	0	—	0	—	0	—	0	—	ns	

Read Cycle (RAM), Page Mode Read Cycle

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	120	—	150	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	*3, *5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	*3, *6
Output buffer turn-off delay referenced to $\overline{CAS}$	t_{OFF1}	—	25	—	25	—	30	—	40	ns	*7
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	*7
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	*12
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	*12
$\overline{RAS}$ to column address delay time	t_{RAD}	20	55	20	55	20	65	25	80	ns	*5, *6
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	—	75	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100	—	100	—	100	—	100	µs	

Write Cycle (RAM), Page Mode Write Cycle

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	ns	*9
Write command hold time	t_{WCH}	25	—	25	—	25	—	30	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	
Page mode cycle time	t_{PC}	55	—	55	—	65	—	80	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	20	—	ns	
Page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100	—	100	—	100	—	100	µs	

Read-Modify-Write Cycle

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read modify write cycle time	t_{RWC}	255	—	255	—	295	—	350	—	ns	
$\overline{RAS}$ pulse width	t_{RWS}	165	10000	165	10000	195	10000	240	10000	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	65	—	65	—	75	—	90	—	ns	*9
Column address to $\overline{WE}$ delay	t_{AWD}	80	—	80	—	95	—	120	—	ns	*9
$\overline{OE}$ to data-in delay time	t_{ODD}	25	—	25	—	30	—	40	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	100	—	100	—	12	—	150	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	30	—	30	—	35	—	40	ns	*3,*5
Access time from $\overline{OE}$	t_{OAC}	—	30	—	30	—	35	—	40	ns	*3
Address access time	t_{AA}	—	45	—	45	—	55	—	70	ns	*3,*6
$\overline{RAS}$ to column address delay	t_{RAD}	20	55	20	55	20	65	25	80	ns	*5,*6
Output buffer turn-off delay referenced to $\overline{OE}$	t_{OFF2}	—	25	—	25	—	30	—	40	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	30	—	30	—	35	—	40	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	30	—	30	—	35	—	40	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	ns	*10
Data-in hold time	t_{DH}	25	—	25	—	25	—	30	—	ns	*10
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
Mask data to $\overline{RAS}$ setup time	t_{MS}	0	—	0	—	0	—	0	—	ns	
Mask data to $\overline{RAS}$ hold time	t_{MH}	15	—	15	—	15	—	20	—	ns	
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	10	—	10	—	15	—	20	—	ns	

Refresh Cycle

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	20	—	20	—	25	—	30	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	ns	

Transfer Cycle

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{WE}$ to $\overline{RAS}$ setup time	t_{WS}	0	—	0	—	0	—	0	—	ns	
$\overline{WE}$ to $\overline{RAS}$ hold time	t_{WH}	15	—	15	—	15	—	20	—	ns	
$\overline{SE}$ to $\overline{RAS}$ setup time	t_{ES}	0	—	0	—	0	—	0	—	ns	
$\overline{SE}$ to $\overline{RAS}$ hold time	t_{EH}	15	—	15	—	15	—	20	—	ns	
$\overline{RAS}$ to SC delay time	t_{SRD}	25	—	30	—	30	—	35	—	ns	
SC to $\overline{RAS}$ setup time	t_{SRS}	30	—	40	—	40	—	45	—	ns	
$\overline{DT}$ hold time from $\overline{RAS}$	t_{RDH}	80	—	90	—	90	—	110	—	ns	
$\overline{DT}$ hold time from $\overline{CAS}$	t_{CDH}	20	—	30	—	30	—	45	—	ns	
Last SC to $\overline{DT}$ delay time	t_{SDD}	5	—	5	—	5	—	10	—	ns	
First SC to $\overline{DT}$ hold time	t_{SDH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ to $\overline{RAS}$ lead time	t_{DTL}	50	—	50	—	50	—	50	—	ns	
$\overline{DT}$ hold time referenced to $\overline{RAS}$ high	t_{DTHH}	20	—	25	—	25	—	30	—	ns	
$\overline{DT}$ precharge time	t_{DTP}	30	—	35	—	35	—	40	—	ns	
Serial data input delay time from $\overline{RAS}$	t_{SID}	50	—	60	—	60	—	75	—	ns	
Serial data input to $\overline{RAS}$ delay time	t_{SZR}	—	10	—	10	—	10	–	10	ns	
Serial output buffer turn-off delay from $\overline{RAS}$	t_{SRZ}	10	50	10	60	10	60	10	75	ns	*7
$\overline{RAS}$ to Sout (Low-Z) delay time	t_{RLZ}	5	—	10	—	10	—	10	—	ns	
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Serial clock cycle time	t_{SCC2}	40	—	40	—	40	—	60	—	ns	*13
Access time from SC	t_{SCA}	—	30	—	35	—	40	–	50	ns	*4
Serial data out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	

Serial Read Cycle

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
Access time from SC	t_{SCA}	—	30	—	35	—	40	—	50	ns	*4
Access time from $\overline{SE}$	t_{SEA}	—	25	—	30	—	30	—	40	ns	*4
Serial data-out hold time	t_{SOH}	7	—	7	—	7	—	7	—	ns	*4
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial output buffer turn-off delay from $\overline{SE}$	t_{SEZ}	—	25	—	25	—	25	—	30	ns	*7

Serial Write Cycle

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Serial clock cycle time	t_{SCC}	30	—	40	—	40	—	60	—	ns	
SC pulse width	t_{SC}	10	—	10	—	10	—	10	—	ns	
SC precharge width	t_{SCP}	10	—	10	—	10	—	10	—	ns	
Serial data-in setup time	t_{SIS}	0	—	0	—	0	—	0	—	ns	
Serial data-in hold time	t_{SIH}	15	—	20	—	20	—	25	—	ns	
Serial write enable setup time	t_{SWS}	0	—	0	—	0	—	0	—	ns	
Serial write enable hold time	t_{SWH}	30	—	35	—	35	—	50	—	ns	
Serial write disable setup time	t_{SWIS}	0	—	0	—	0	—	0	—	ns	
Serial write disable hold time	t_{SWIH}	30	—	35	—	35	—	50	—	ns	

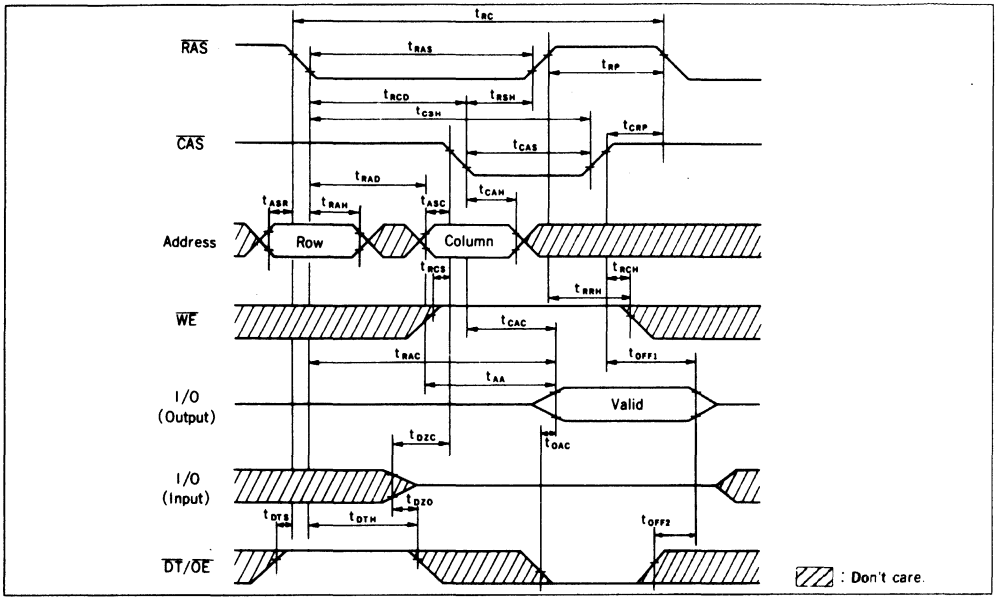
Logic Operation Mode

Item	Symbol	HM534252-10		HM534252-11		HM534252-12		HM534252-15		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ hold time (logic operation set/reset cycle	t_{FCHR}	90	—	90	—	100	—	120	—	ns	
$\overline{RAS}$ pulse width in write cycle	t_{RFS}	140	10000	140	10000	165	10000	200	10000	ns	
$\overline{CAS}$ pulse width in write cycle	t_{CFS}	60	10000	60	10000	70	10000	80	10000	ns	
$\overline{CAS}$ hold time in write cycle	t_{FCSH}	140	—	140	—	165	—	200	—	ns	
$\overline{RAS}$ hold time in write cycle	t_{FRSH}	60	—	60	—	70	—	80	—	ns	
Write cycle time	t_{FRC}	230	—	230	—	265	—	310	—	ns	
Page mode cycle time (write cycle)	t_{FPC}	85	—	85	—	100	—	120	—	ns	
Page mode $\overline{RAS}$ pulse width	t_{RFSP}	—	100	—	100	—	100	—	100	μs	

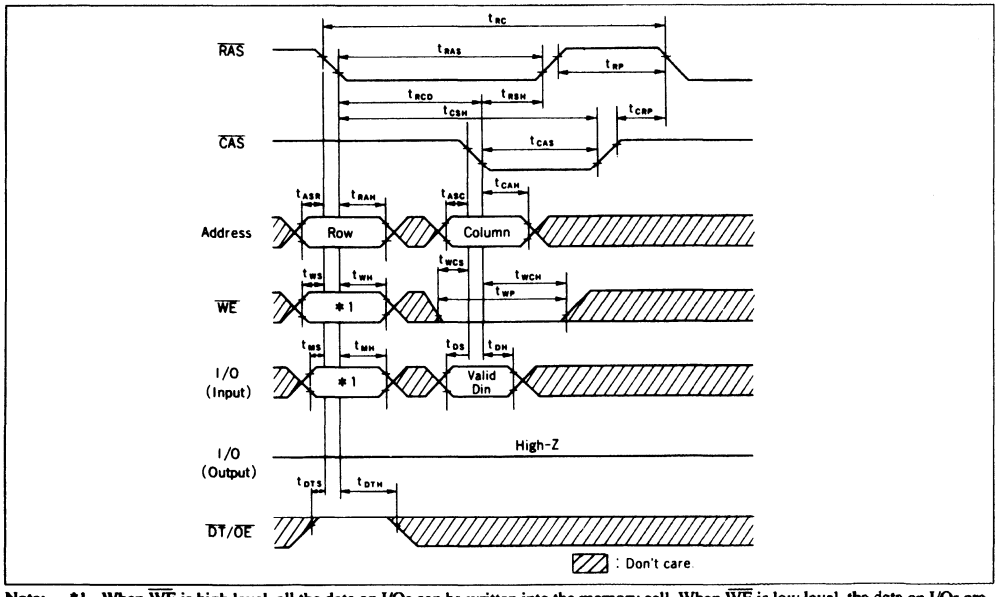
Notes:
*1. AC measurements assume $t_T = 5$ ns.
*2. Assume that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
*3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
*4. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
*5. When $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max), access time is specified by t_{CAC}.
*6. When $t_{RCD} \leq t_{RCD}$ (max) and $\overline{t_{RAD}} \geq t_{RAD}$ (max), access time is specified by t_{AA}.
*7. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition (V_{OH} – 200 mV, V_{OL} + 200 mV).
*8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
*9. When $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle, and I/O pins remain in an open circuit (high impedance) condition. When $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-modify-write cycle; the data of the selected address is read out from a data output pin and input data is written into the selected address. In this case, impedance on I/O pins is controlled by $\overline{OE}$.
*10. These parameters are referenced to $\overline{CAS}$ falling edge in early write cycles or to $\overline{WE}$ falling edge in delayed write or read-modify-write cycles.
*11. After power-up, pause for 100 μs or more and execute at least 8 initialization cycles (normal memory cycles or refresh cycles), then start operation.
*12. If either t_{RCH} or t_{RRH} is satisfied, operation is guaranteed.
*13. t_{SCC2} is applied to the last SAM access cycle of read transfer cycle-1 before transfer.

Timing Waveforms

Read Cycle

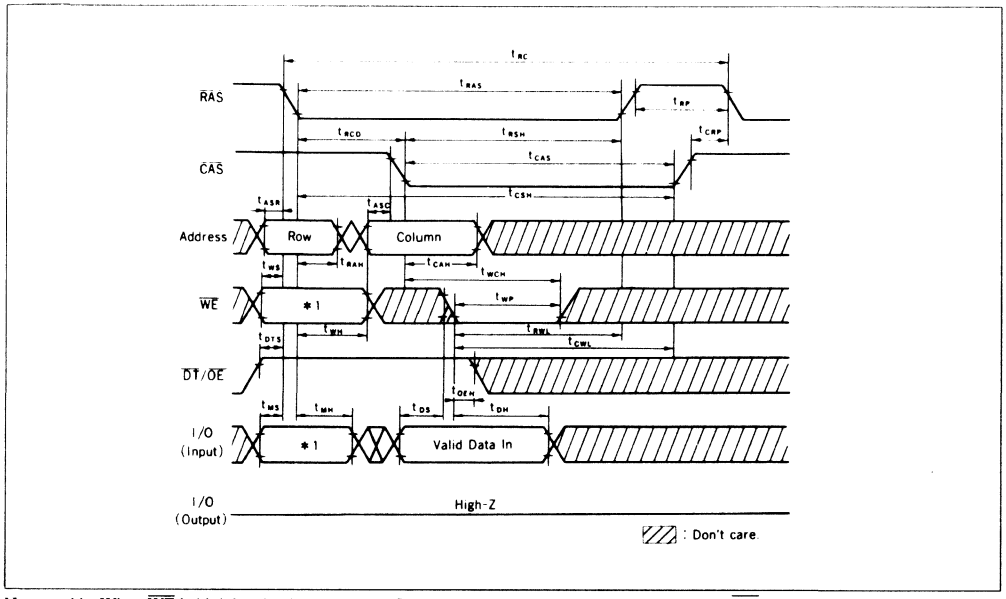


Early Write Cycle



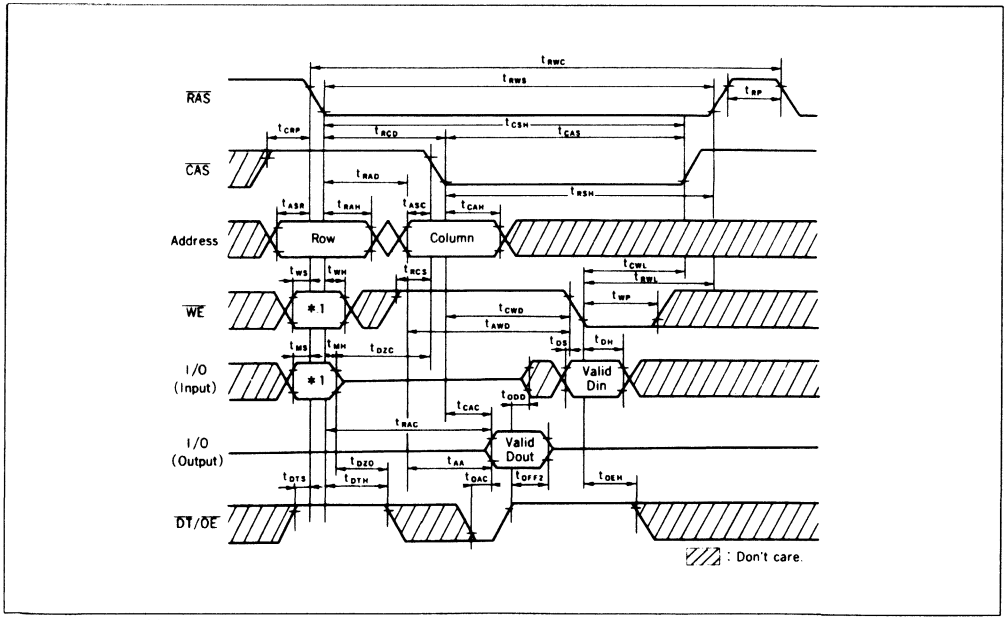
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



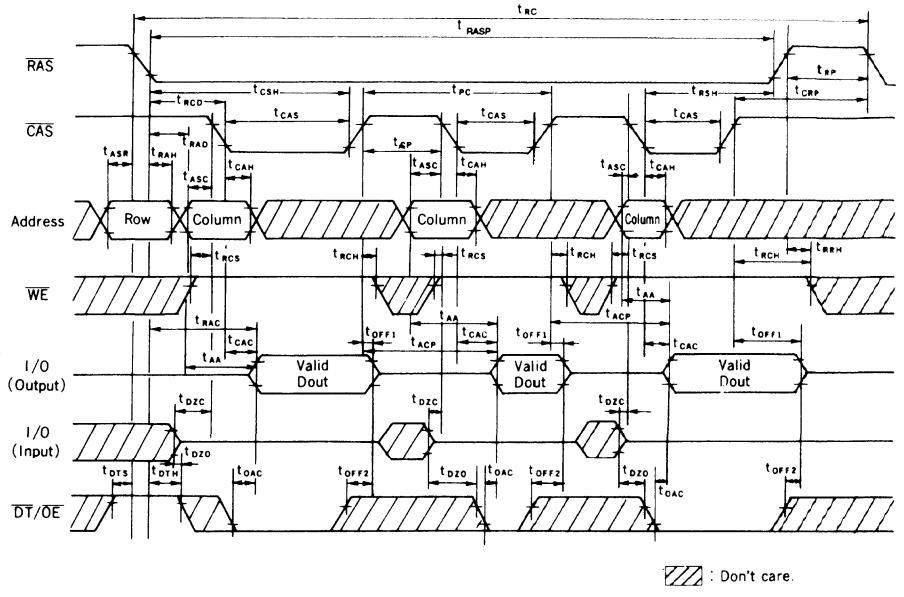
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Read-Modify-Write Cycle

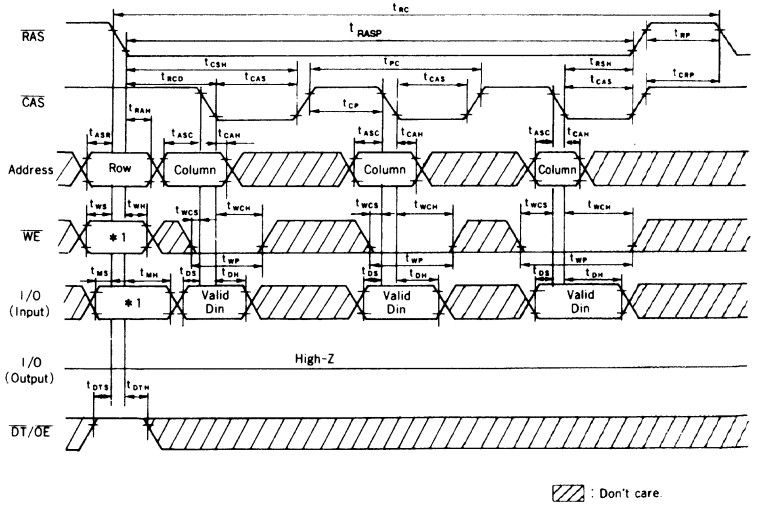


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Read Cycle

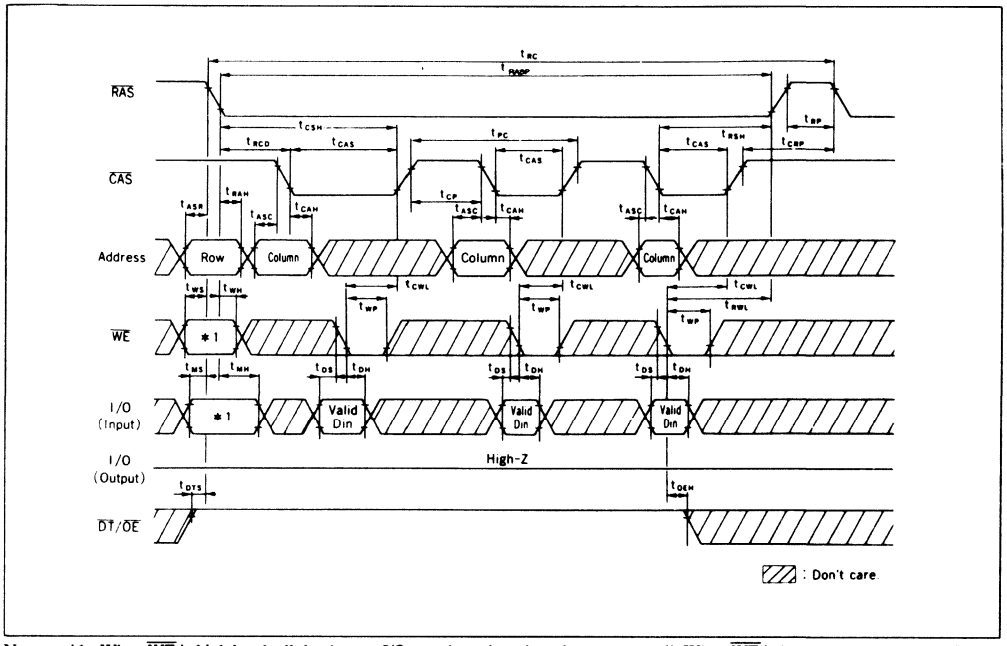


Page Mode Write Cycle (Early Write)



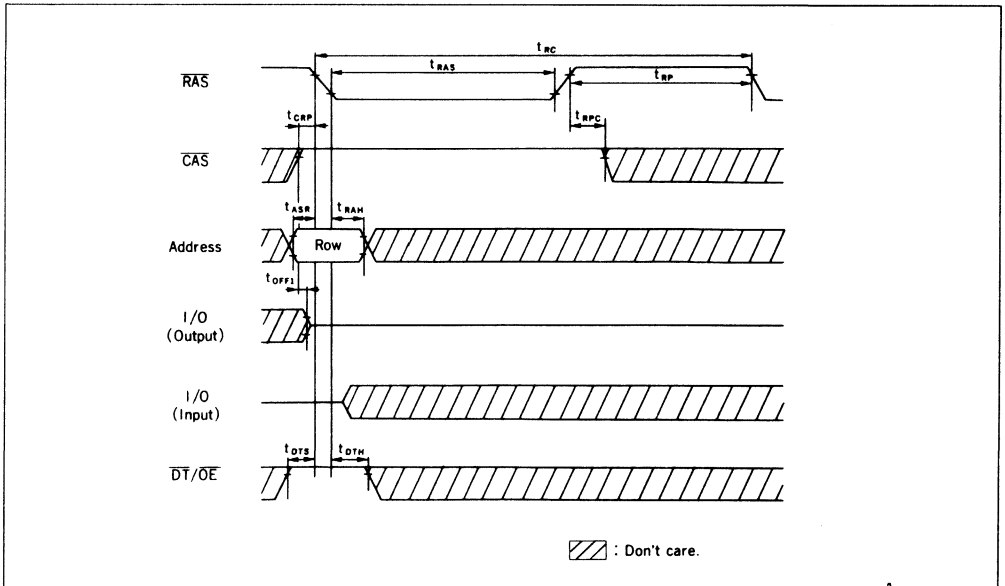
Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)

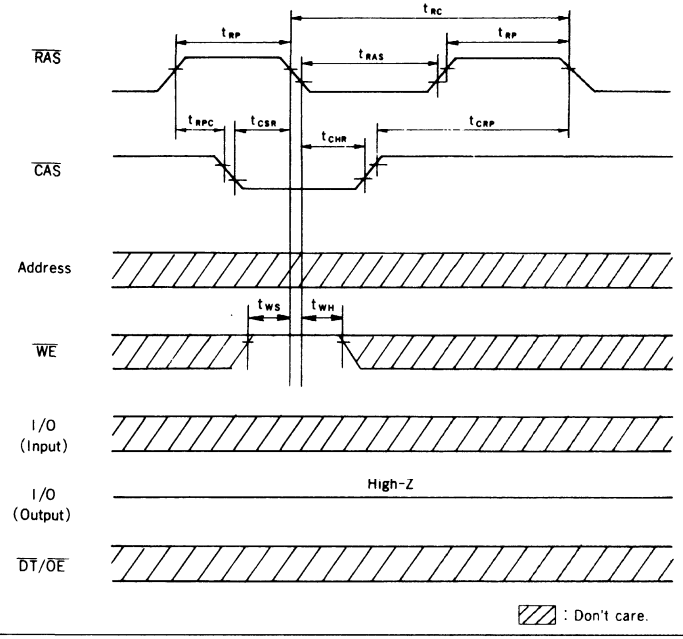


Note: *1. When $\overline{WE}$ is high level, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low level, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

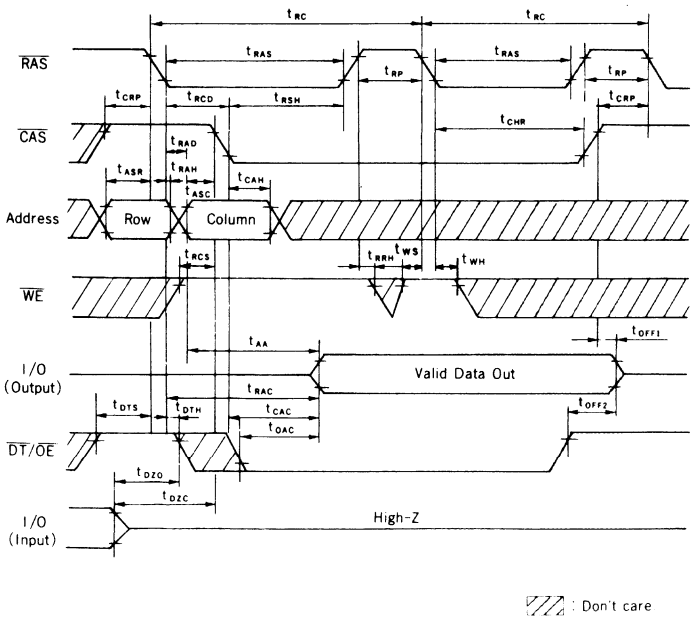
$\overline{RAS}$-Only Refresh Cycle



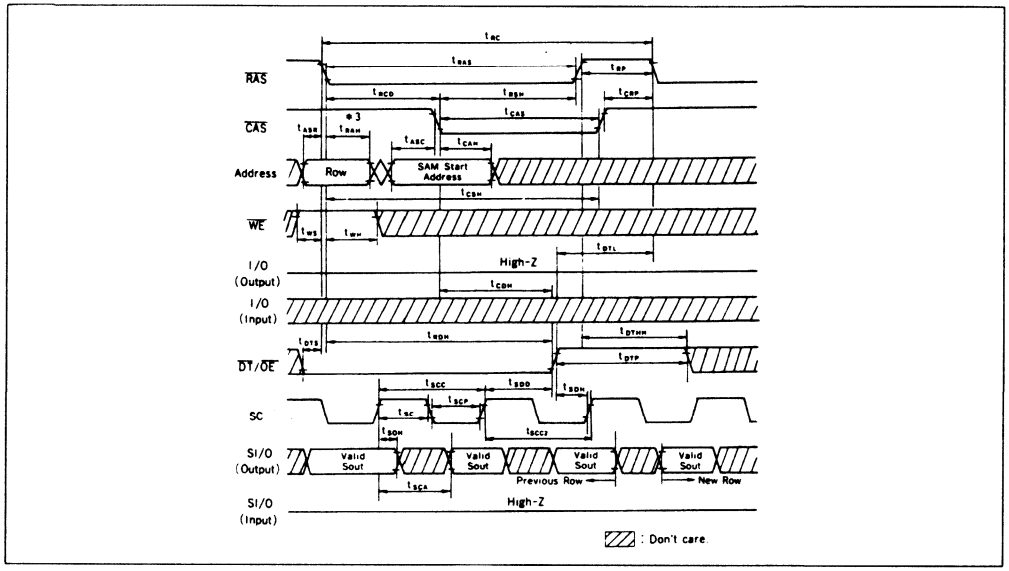
CAS-Before-RAS Refresh Cycle



Hidden Refresh Cycle

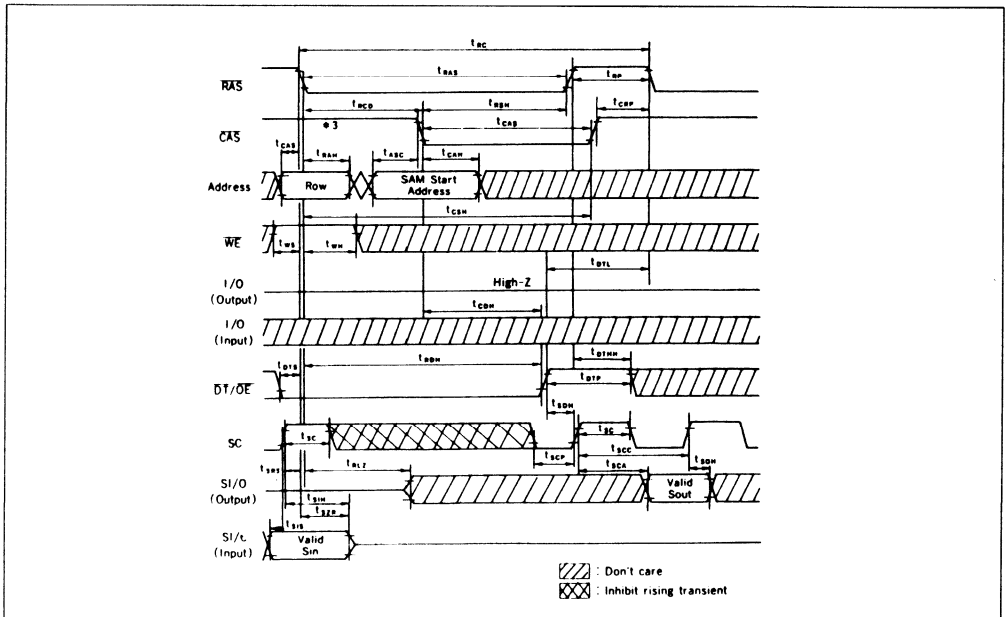


Read Transfer Cycle (1) *1,*2



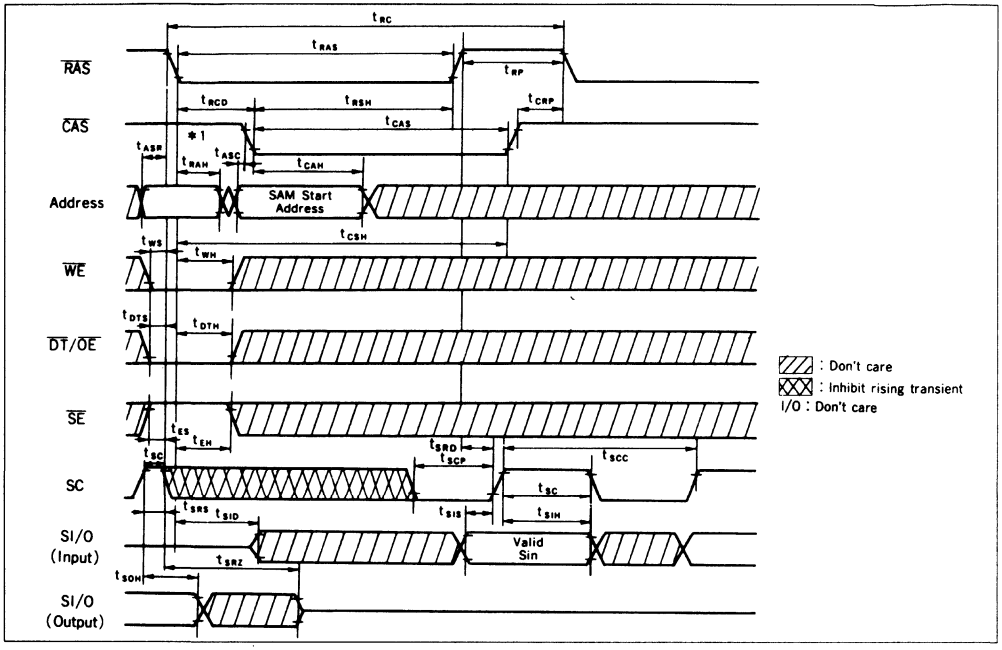
Notes: *1. When the previous data transfer cycle is a read transfer cycle, it is defined as read transfer cycle (1).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

Read Transfer Cycle (2) *1,*2

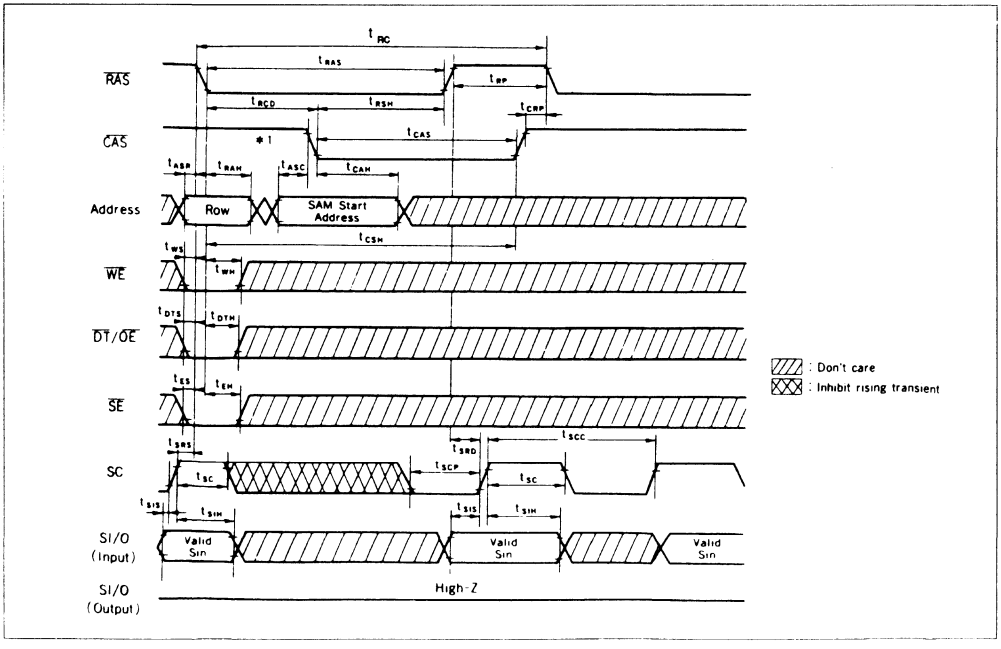


Notes: *1. When the previous data transfer cycle is a write or pseudo transfer cycle, it is defined as read transfer cycle (2).
*2. $\overline{SE}$ is in low level. (When $\overline{SE}$ is high, SI/O becomes high impedance.)

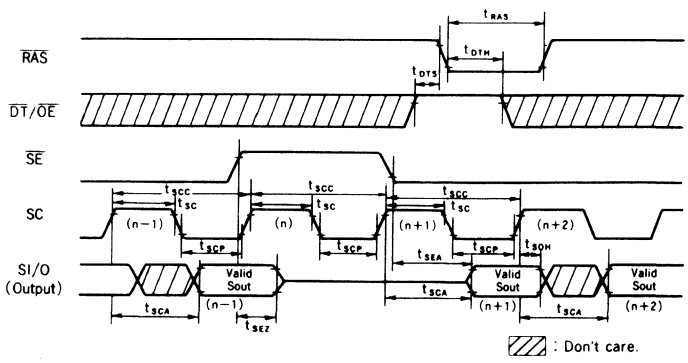
Pseudo Transfer Cycle



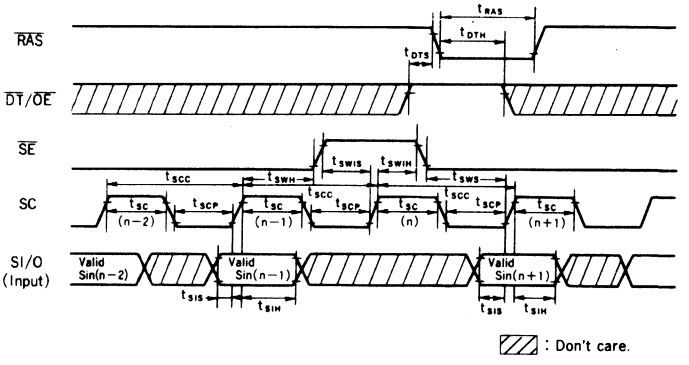
Write Transfer Cycle



Serial Read Cycle

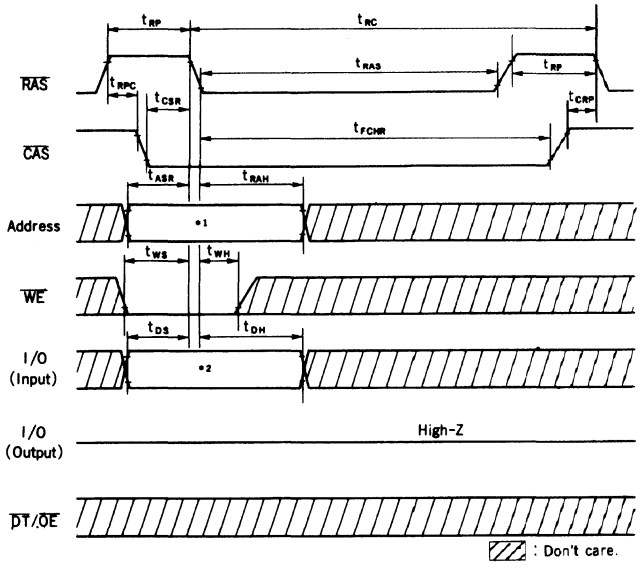


Serial Write Cycle



Notes: *1. When $\overline{SE}$ is high level in a serial write cycle, data is not written into SAM, however, the pointer is incremented.
*2. Address 0 is accessed next to address 511.

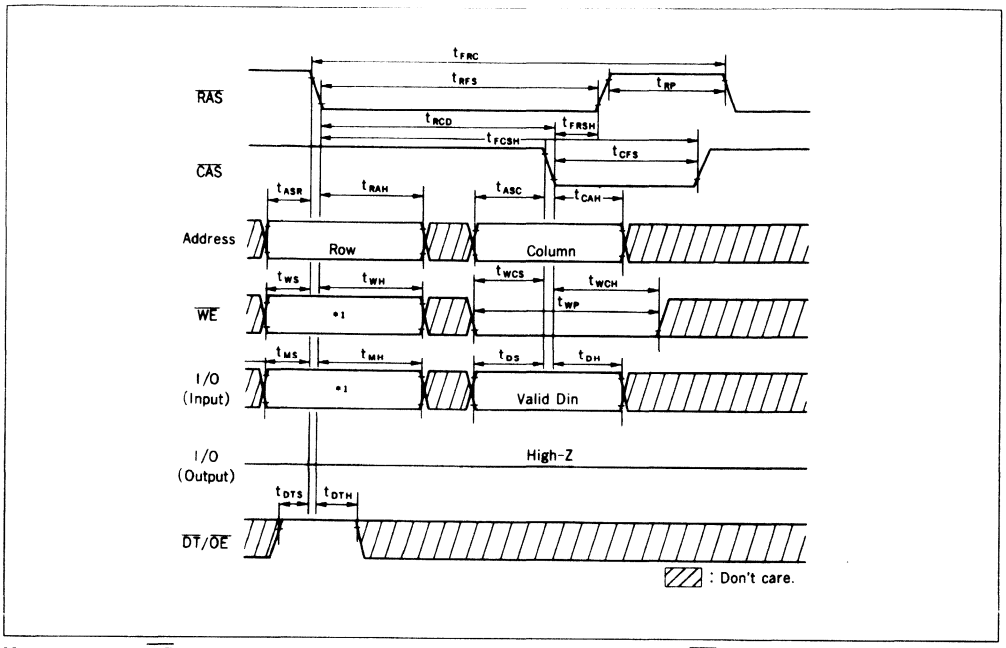
Logic Operation Set/Reset Cycle



Notes: *1. Logic code A0–A3
*2. Write mask data

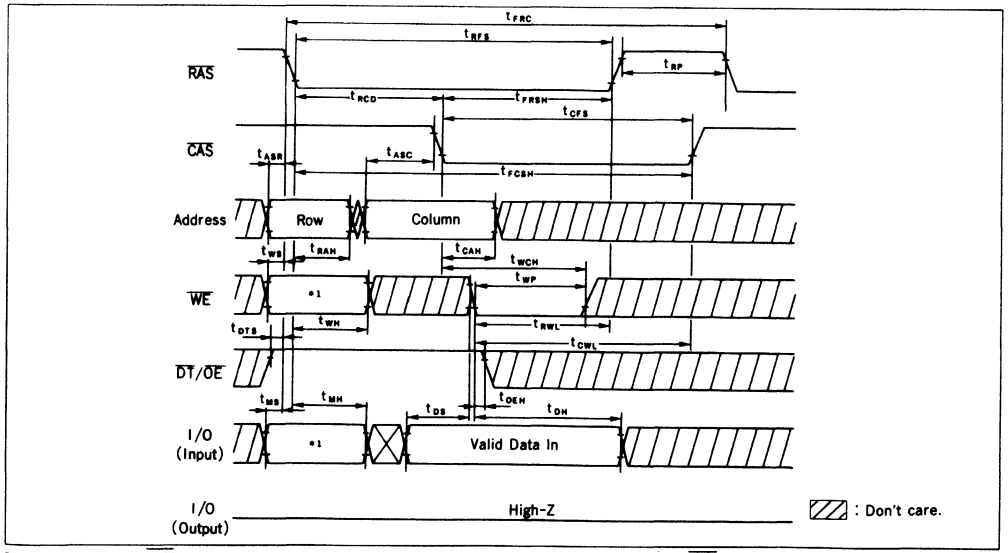
Logic Operation Mode Timing Waveforms

Early Write Cycle



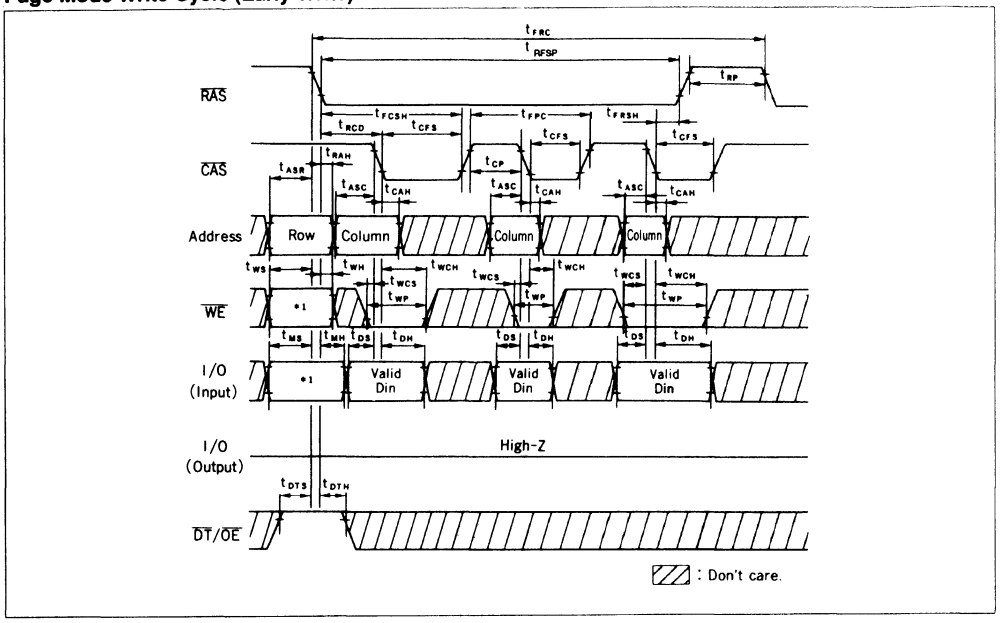
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Delayed Write Cycle



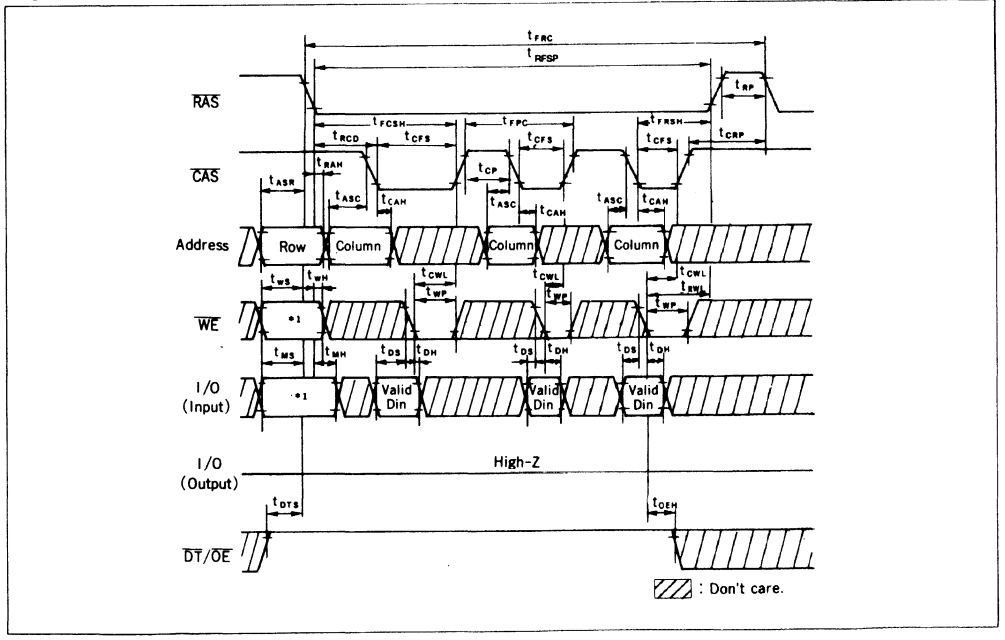
Note: *1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Early Write)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

Page Mode Write Cycle (Delayed Write)



Note: 1. When $\overline{WE}$ is high, all the data on I/Os can be written into the memory cell. When $\overline{WE}$ is low, the data on I/Os are not written except for the case that the I/O is high at the falling edge of $\overline{RAS}$.

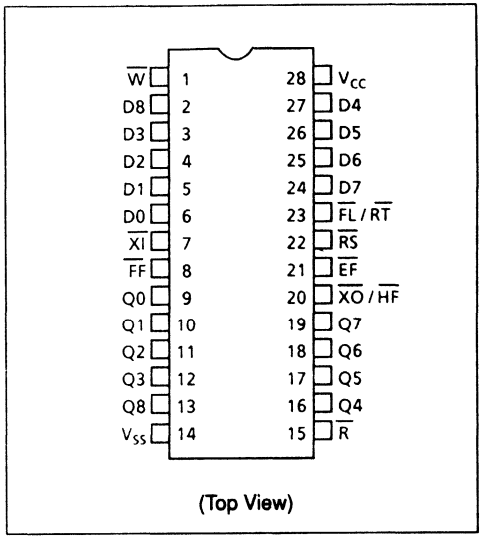
HM63921 Series — Preliminary

2 k × 9-Bit CMOS Parallel In-Out FIFO Memory

The HM63921 is a first-in, first-out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and half-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data. Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 30/35/45 ns. Organization of HM63921 provides a 9-bit data bus. The ninth bit could be used for control or parity for error checking at the option of the user. The HM63921 is fabricated using the Hitachi CMOS 1.3 micron technology. The device is available in DIP and SOJ.

Pin Arrangement



(Top View)

Features

- First-in, first-out dual port memory
- 2 k × 9 organization
- Low-power CMOS 1.3 micron technology
- Asynchronous and simultaneous read and write
- Fully expandable in depth and/or width
- Single 5 V (± 10%) power supply
- Empty and full warning flags
- Half-full flag
- Access time: 20/25/35 ns
- Package: 300-mil 28-pin plastic DIP package
  300-mil 28-pin plastic SOJ package

Ordering Information

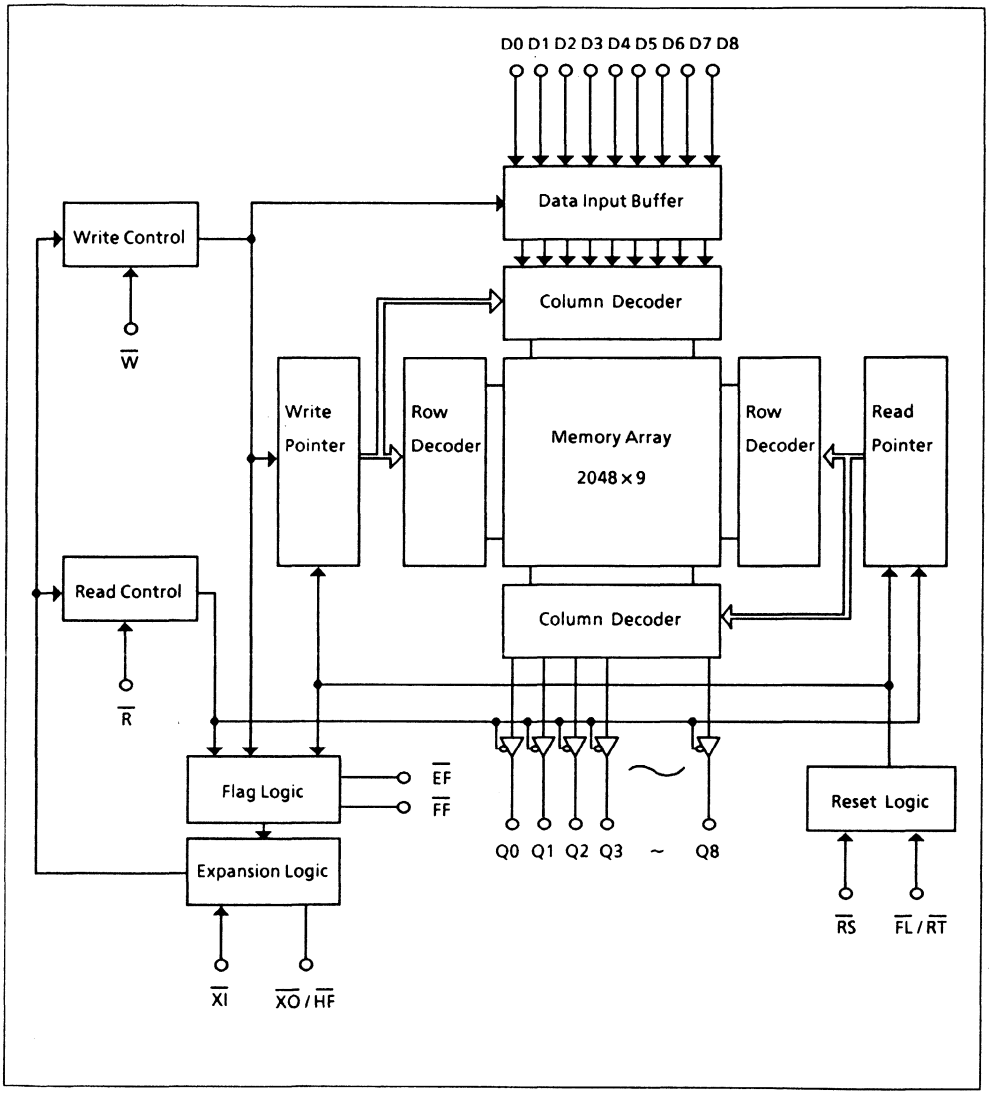
Type name	Access time	Package
HM63921P-20	20 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM63921P-25	25 ns	
HM63921P-35	35 ns	
HM63921JP-20	20 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM63921JP-25	25 ns	
HM63921JP-35	35 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Description

Pin name	Function
D0 – D8	Data inputs
$\overline{RS}$	Reset
$\overline{W}$	Write enable
$\overline{R}$	Read enable
$\overline{FL}$	First load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-in
$\overline{XO}$	Expansion-out
$\overline{HF}$	Half-full flag
$\overline{FF}$	Full flag
$\overline{EF}$	Empty flag
Q0 – Q8	Data outputs

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal voltage *1	V_T	−0.5 *2 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. Relative to V_{SS}
2. −3.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.4	—	6.0	V
	V_{IL}	−0.5 *1	—	0.8	V

Note: 1. −3.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol		Min	Typ	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$		—	—	2	µA	V_{CC} = 5.5 V, Vin = 0 V – V_{CC}
Output leakage current (Q0–Q8 pins)	$\|I_{LO}\|$		—	—	2	µA	$\overline{R}$ = V_{IH}, Vout = 0 V – V_{CC}
Operating power supply current	I_{CC1}	-20	—	—	120	mA	Average operating current
		-25	—	—	110	mA	
		-35	—	—	100	mA	
Standby power supply current	I_{SB1}		—	—	10	mA	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/$\overline{RT}$ = V_{IH}
	I_{SB2}		—	—	1	mA	All inputs ≥ V_{CC}−0.2 V

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA

Capacitance (Ta = 25°C, f = 1 MHz)

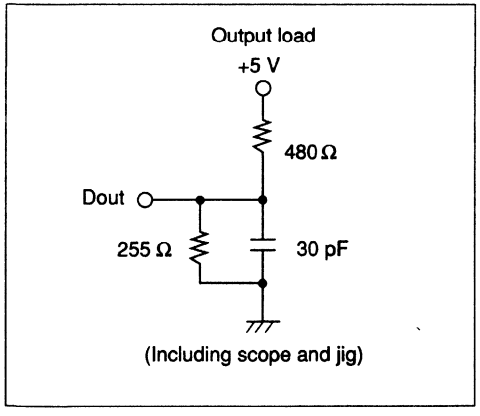
Parameter	Symbol	Typ	Max	Unit	Test conditons
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	Vout = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

- Input pulse levels : V_{SS} to 3.0 V
- Input rise and fall times : 5 ns
- Input and output timing reference level : 1.5 V
- Output load : See figure



Read Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	30	—	35	—	45	—	ns
Access time	t_A	—	20	—	25	—	35	ns
Read recovery time	t_{RR}	10	—	10	—	10	—	ns
Read pulse width	t_{RPW}	20	—	25	—	35	—	ns
Read low to DB low-Z	t_{RLZ}*1	5	—	5	—	5	—	ns
Read high to DB high-Z	t_{RHZ}*1	—	15	—	15	—	20	ns
Data valid from read high	t_{OH}	3	—	3	—	3	—	ns
Read pulse width after empty flag high	t_{RPE}	20	—	25	—	35	—	ns
Write high to DB low-Z (Read data flow through mode)	t_{WLZ}*1	3	—	3	—	3	—	ns

Note: 1. t_{RLZ}, t_{RHZ} and t_{WLZ} are sampled and not 100% tested.

Write Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	30	—	35	—	45	—	ns
Write recovery time	t_{WR}	10	—	10	—	10	—	ns
Write pulse width	t_{WPW}	20	—	25	—	35	—	ns
Data setup time	t_{DS}	10	—	15	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	5	—	ns
Effective write pulse width after full flag high	t_{WPF}	20	—	25	—	35	—	ns

Reset Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Reset cycle time	t_{RSC}	30	—	35	—	45	—	ns
Reset pulse width	t_{RS}	20	—	25	—	35	—	ns
Reset setup time	t_{RSS}	20	—	25	—	35	—	ns
Reset recovery time	t_{RSR}	10	—	10	—	10	—	ns
Read low to reset low delay time	t_{RRD}	20	—	25	—	35	—	ns
XI high setup time	t_{RXS}	5	—	5	—	5	—	ns
XI high hold time	t_{RXH}	10	—	10	—	10	—	ns

Retransmit Cycle

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Retransmit cycle time	t_{RTC}	30	—	35	—	45	—	ns
Retransmit pulse width	t_{RT}	20	—	25	—	35	—	ns
Retransmit setup time	t_{RTS}	20	—	25	—	35	—	ns
Retransmit recovery time	t_{RTR}	10	—	10	—	10	—	ns
Read low to retransmit low delay time	t_{RTD}	20	—	25	—	35	—	ns

Flag Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Reset to empty flag low	t_{EFL}	—	25	—	30	—	40	ns
Reset to full flag high	t_{FFH}	—	25	—	30	—	40	ns
Reset to expansion out/half-full flag high	t_{HFH}	—	15	—	20	—	30	ns
Retransmit to empty flag high	t_{TEF}	—	25	—	30	—	40	ns
Retransmit to full flag high/low	t_{TFF}	—	25	—	30	—	40	ns
Retransmit to half-full flag high/low	t_{THF}	—	40	—	45	—	50	ns
Read low to empty flag low	t_{REF}	—	20	—	25	—	35	ns
Read high to full flag high	t_{RFF}	—	20	—	25	—	35	ns
Write high to empty flag high	t_{WEF}	—	20	—	25	—	35	ns
Write low to full flag low	t_{WFF}	—	20	—	25	—	35	ns
Write low to half-full flag low	t_{WHF}	—	30	—	35	—	45	ns
Read high to half-full flag high	t_{RHF}	—	30	—	35	—	45	ns

Expansion Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min	Max	Min	Max	Min	Max	
Read/write low to expansion out low	t_{XOL}	—	15	—	20	—	30	ns
Read/write high to expansion out high	t_{XOH}	—	15	—	20	—	30	ns
Expansion in pulse width	t_{XI}	10	—	10	—	10	—	ns
Expansion in recovery time	t_{XIR}	10	—	10	—	10	—	ns
Expansion in setup time	t_{XIS}	10	—	10	—	15	—	ns

Signal Description

Inputs

• Reset ($\overline{RS}$)

The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and half-full ($\overline{HF}$) will go high during reset cycle.

• Write enable ($\overline{W}$)

Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of $\overline{W}$ are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.

• Read enable ($\overline{R}$)

Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.

• First load/retransmit ($\overline{FL}/\overline{RT}$)

For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.

• Expansion-in ($\overline{XI}$)

For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.

• Data-In (D0 to D8)

Data inputs for 9-bit wide data.

Outputs

• Full flag ($\overline{FF}$)

The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.

• Empty flag ($\overline{EF}$)

The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.

• Expansion-out ($\overline{XO}$)/half-full flag ($\overline{HF}$)

This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is half full.

• Data outputs (Q0 to Q8)

Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

Various Operations Mode

- Single device mode

If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.

- Width expansion mode

Width expansion by 9-bit increments may be acheived when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short period of time, the flag outputs should not be wired together.

- Depth expansion mode

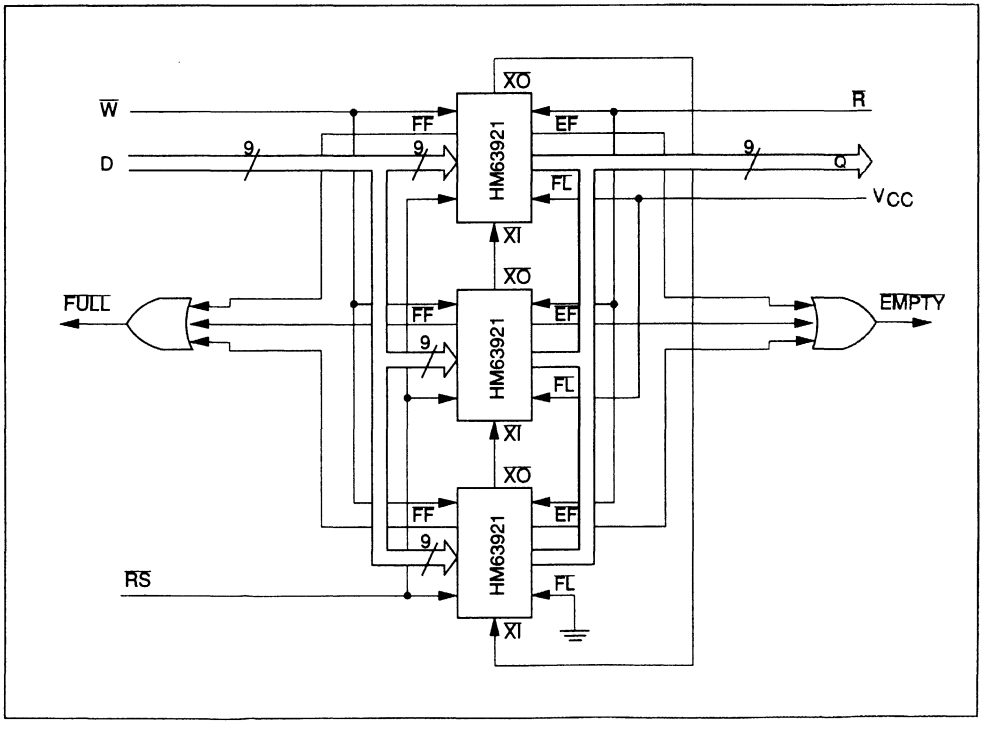
Multiple of FIFOs could provide multiple of 2 k × 9 as (N) × (2 k) by 9-bit wide, where N is the number of FIFOs connected in depth expansion mode. The following arrangement must be provided.

1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
2. All other ($\overline{FL}$) should be connected to V_{CC}.
3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
5. ($\overline{RT}$) and ($\overline{HF}$) will not be available in this mode.

- Compound expansion mode

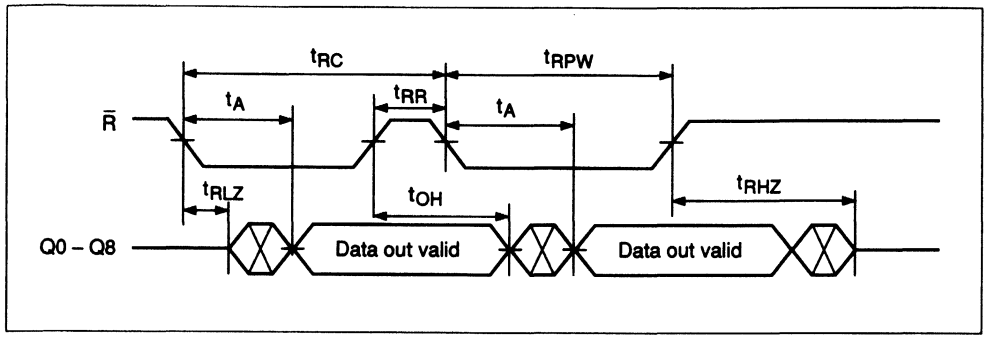
Combination of width and depth expansion modes will provide larger FIFO arrays.

Depth expansion mode

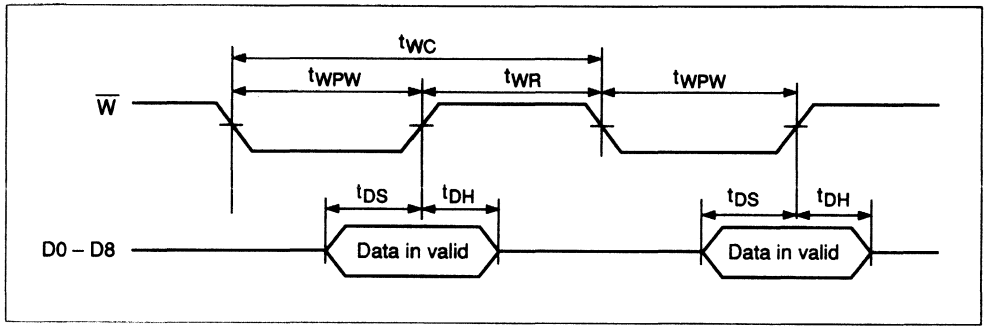


Timing Waveforms

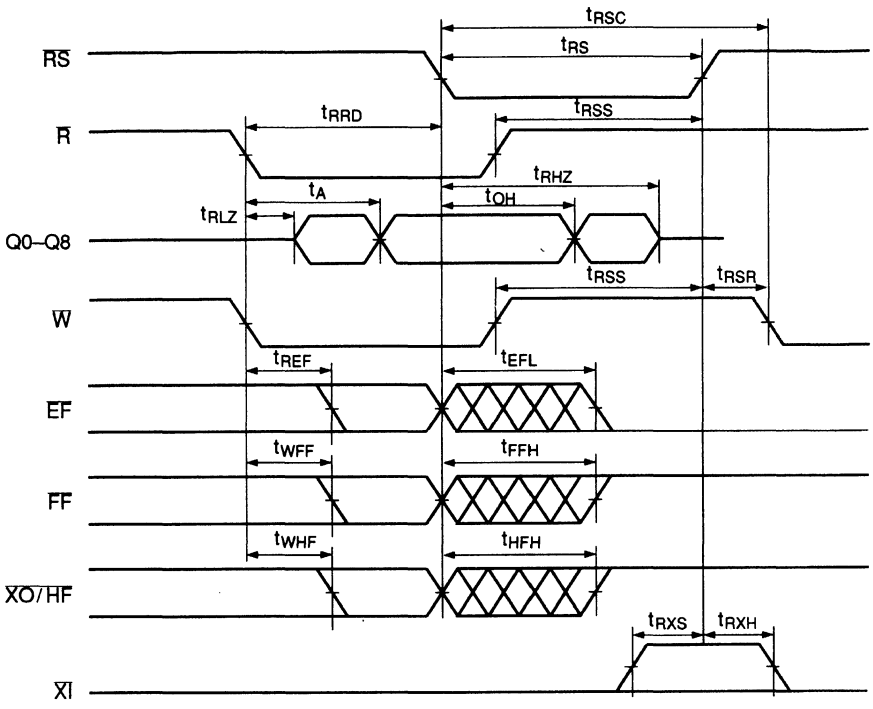
Read Cycle



Write Cycle



Reset Cycle

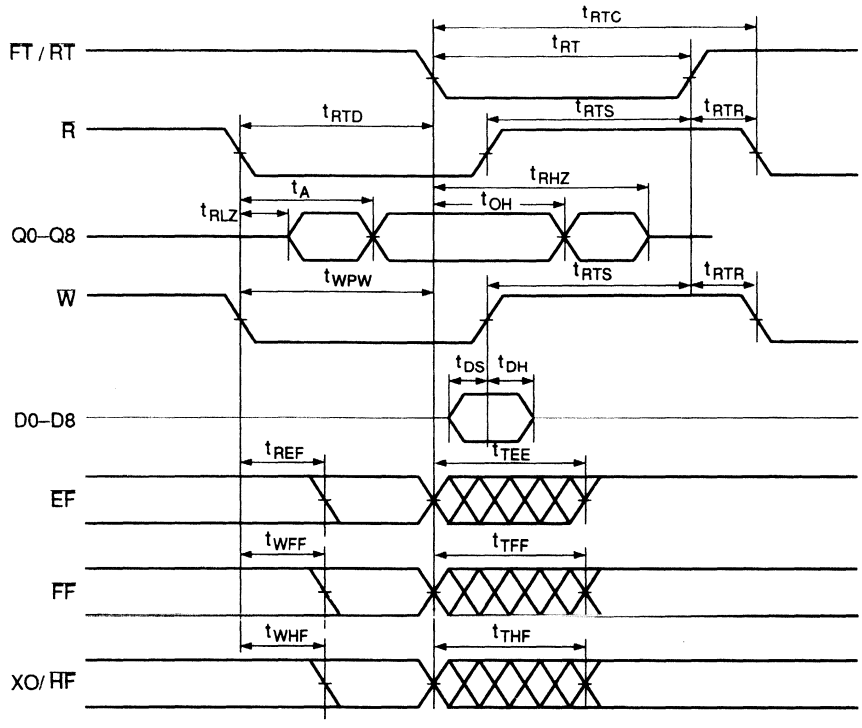


Notes: *1 $\overline{W} = \overline{R} = V_{IH}$ during reset

*2 $t_{RSC} = t_{RS} + t_{RSR}$

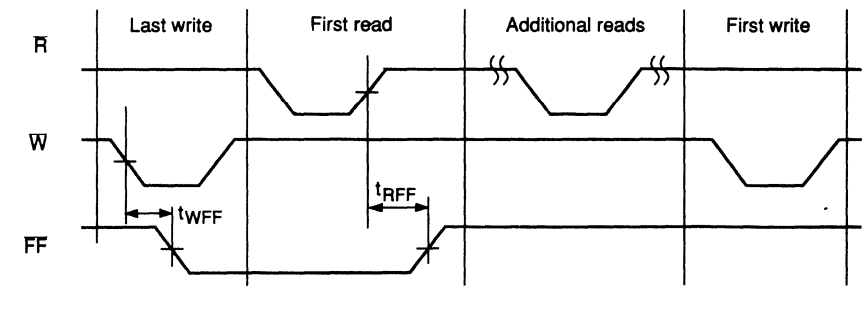
*3 t_{RXS} and t_{RXH} are parameters only for depth expansion mode.

Retransmit Cycle

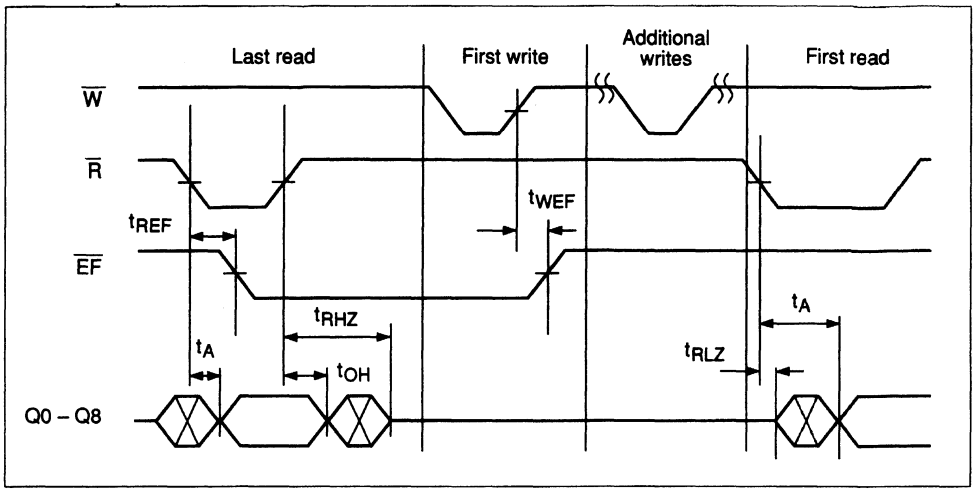


Note: *1 t_{TFF} and t_{THF} are specified by the later timing between $\overline{FL}/\overline{RT}$ falling edge and W rising edge.

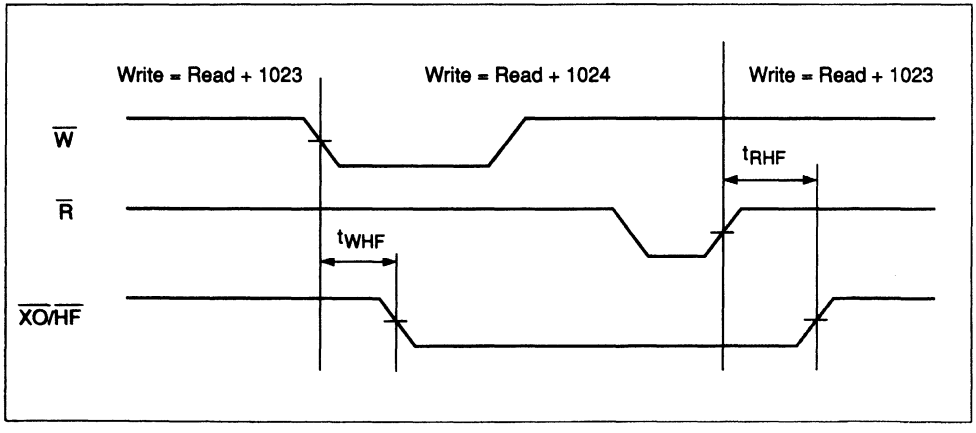
Full-Flag Cycle (From last write to first read)



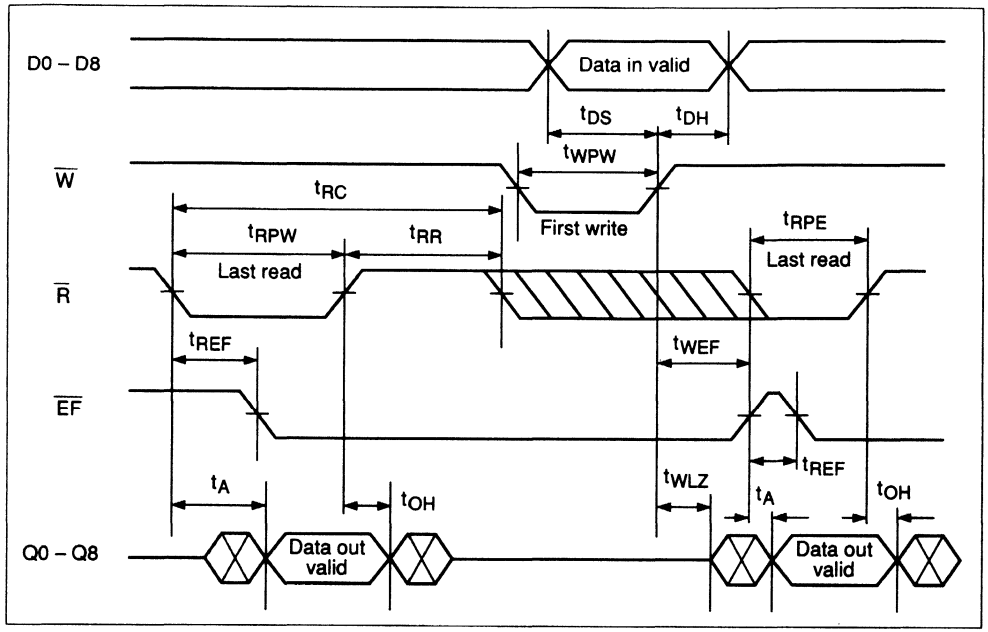
Empty-Flag Cycle (From last read to first write)



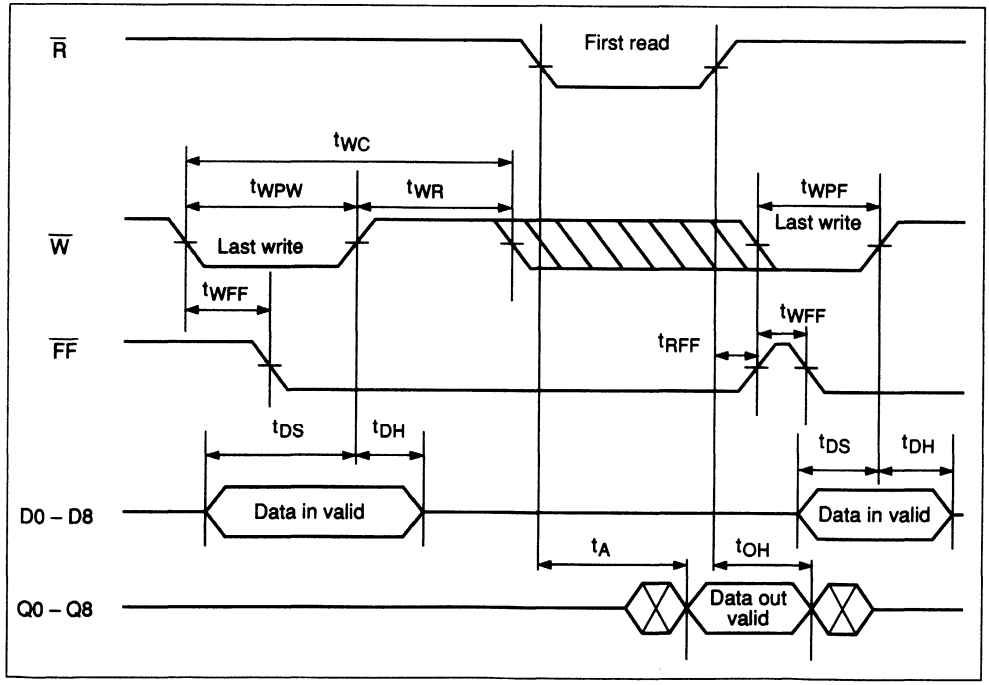
Half-Full Flag Cycle



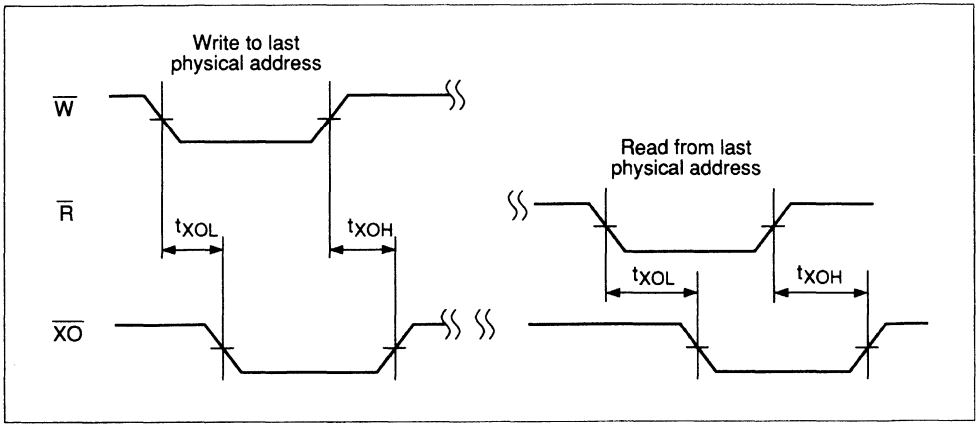
Read Data Flow Through Mode



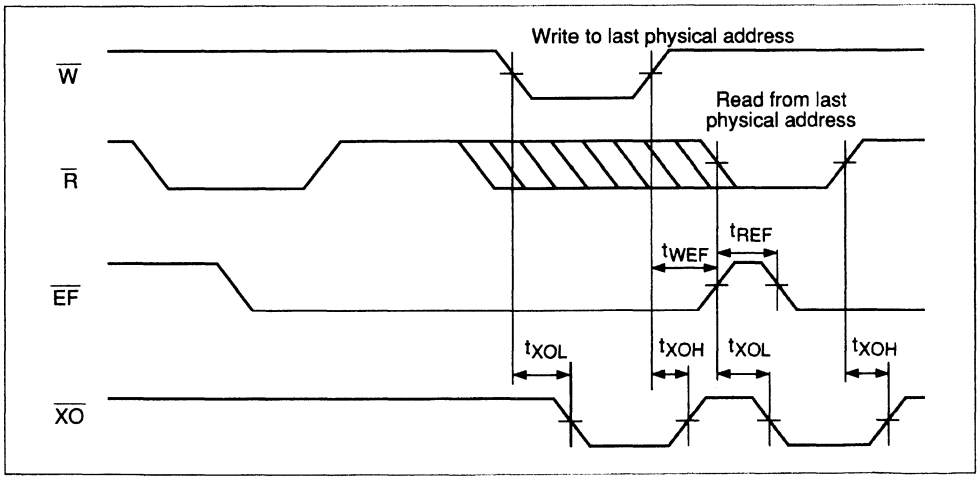
Write Data Flow Through Mode



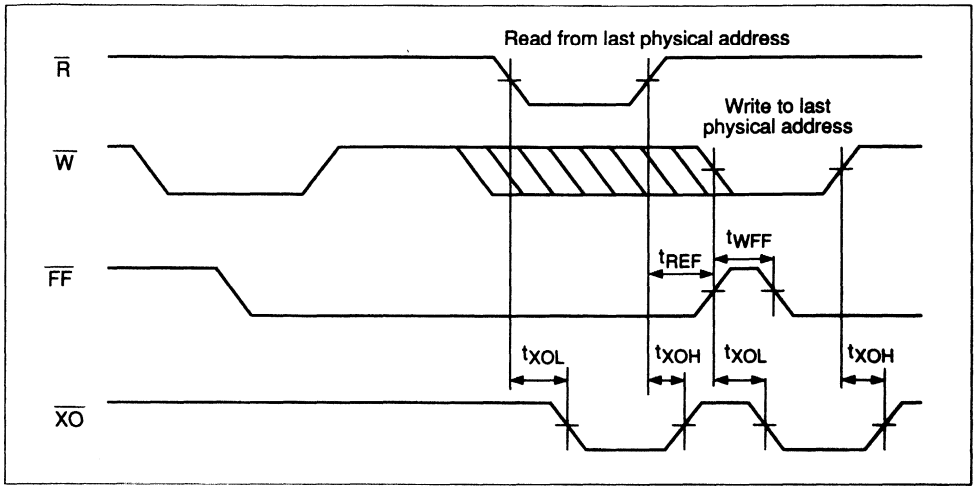
Expansion Out Cycle (1)



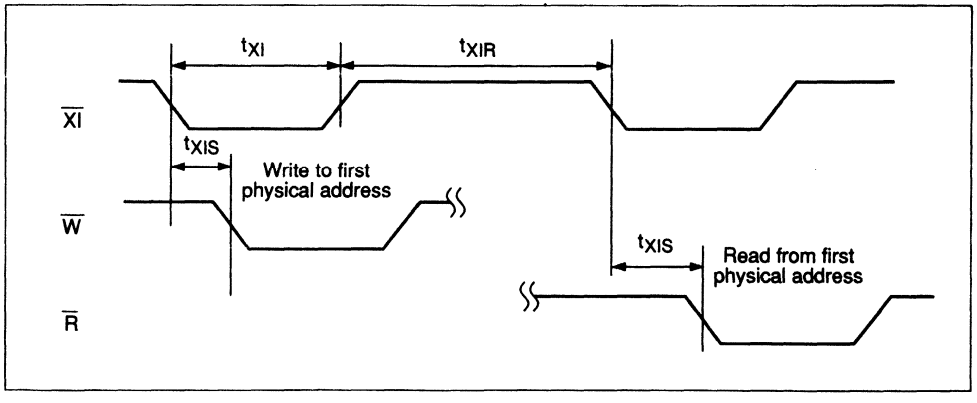
Expansion Out Cycle (2) (Read Data Flow Through Mode)



Expansion Out Cycle (3) (Write Data Flow Through Mode)



Expansion In Cycle



HM63941 Series — Under Development

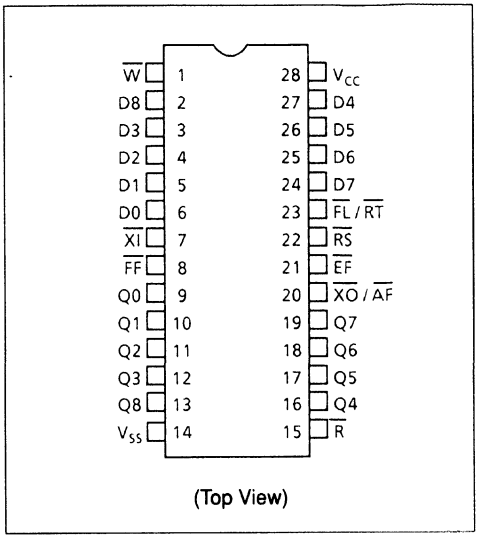
4 k × 9-Bit CMOS Parallel In-Out FIFO Memory

The HM63941 is a first-in, first-out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and half-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 35/45 ns. Organization of HM63941 provides a 9-bit data bus. The ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3 micron technology. The device is available in DIP.

Pin Arrangement



(Top View)

Features

- First-in, first-out dual port memory
- 4 k × 9 organization
- Low-power CMOS 1.3 micron technology
- Asynchronous and simultaneous read and write
- Fully expandable in depth and/or width
- Single 5 V (±10%) power supply
- Empty and full warning flags
- Almost-full flag
- Access time: 25/35 ns
- Package
  - 300-mil 28-pin plastic DIP package
  - 300-mil 28-pin plastic SOJ package

Ordering Information

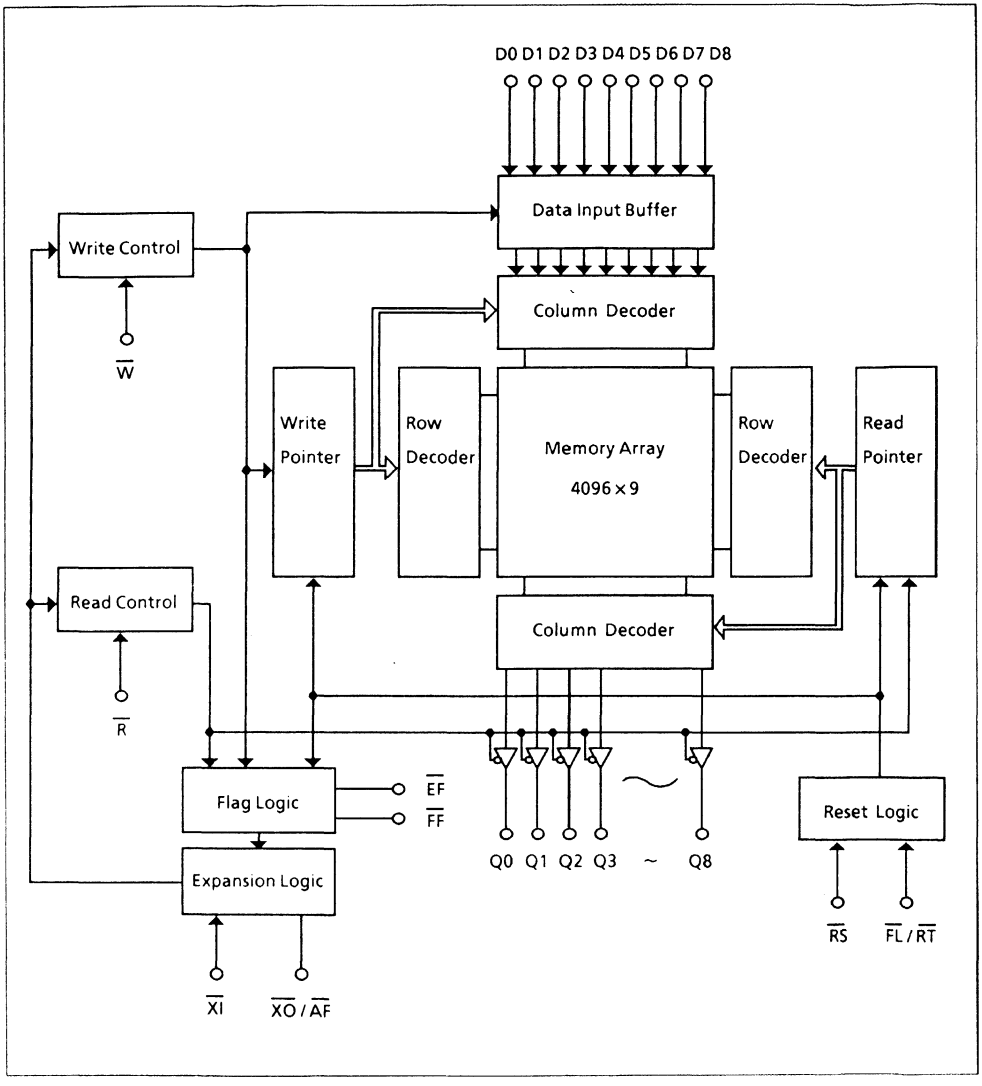
Type No.	Access time	Package
HM63941P-25 HM63941P-35	25 ns 35 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM63941JP-25 HM63941JP-35	25 ns 35 ns	300-mil 28-pin plastic SOJ (CP-28DN)

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Description

Pin name	Function
D0 – D8	Data inputs
$\overline{RS}$	Reset
$\overline{W}$	Write enable
$\overline{R}$	Read enable
$\overline{FL}$	First load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-in
$\overline{XO}$	Expansion-out
$\overline{AF}$	Almost-full flag
$\overline{FF}$	Full flag
$\overline{EF}$	Empty flag
Q0 – Q8	Data outputs

Block Diagram



HM644332 Series

Tag Memory

The HM644332 is a 512-entry × 4-way/1024-entry × 2-way TAG memory fabricated with CMOS technology. It offers compact cache systems with set associativity and a high level of performance for 32-bit microprocessor systems, when used together with fast static RAMs as data RAMs.

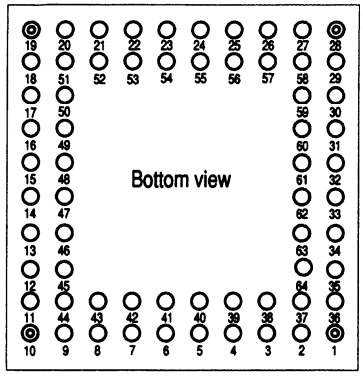
Features

- Programmable organization: 512-entry × 4-way or 1024-entry × 2-way
- Memory organization: 512 words × 98 bits
  98 bits = (20 tag bits + 1 parity bit + 2 validity bits) × 4 ways + 6 LRU bits
- Fast access time: 25/30 ns max from address inputs, 18 ns max from tag data inputs
- Single + 5 V supply
- TTL-compatible inputs and outputs
- LRU (least recently used) replacement algorithm
- Purge functions (all purge and partial purge)
- Internal parity generator/checker
- 64-pin pin-grid-array

Ordering Information

	Access Time		
Part No.	**From Address**	**From Tag Data**	**Package**
HM644332Y-25	25 ns	18 ns	64-pin PGA
HM644332Y-30	30 ns	18 ns	

Pin Arrangement



Pin No.	Function	Pin No.	Function	Pin No.	Function
1	NC	23	A_4	45	TD_6
2	$\overline{MHIT}$	24	A_5	46	TD_9
3	HIT_0/REP_0	25	A_7	47	V_{CC}
4	HIT_2/REP_2	26	A_9	48	TD_{13}
5	HIT_3/REP_3	27	NC	49	TD_{15}
6	TD_0	28	NC	50	TD_{17}
7	TD_2	29	$\overline{PINV}$	51	TD_{19}
8	EXTH	30	SBLK	52	A_0
9	MHENBL	31	SB_1	53	A_2
10	NC	32	$\overline{INH}$	54	V_{SS}
11	TD_7	33	$\overline{INVL}$	55	A_6
12	TD_8	34	$\overline{SET}$	56	A_8
13	TD_{10}	35	H/R	57	$\overline{PURGE}$
14	TD_{11}	36	$\overline{HIT}$	58	MODE
15	TD_{12}	37	HC_0/RC_0	59	$\overline{VINV}$
16	TD_{14}	38	HC_1/RC_1	60	SB_0
17	TD_{16}	39	HIT_1/REP_1	61	V_{CC}
18	TD_{18}	40	V_{SS}	62	$\overline{WRITE}$
19	NC	41	TD_1	63	RLATCH
20	NC	42	TD_3	64	$\overline{PERR}$
21	A_1	43	TD_4		
22	A_3	44	TD_5		

Pin Description

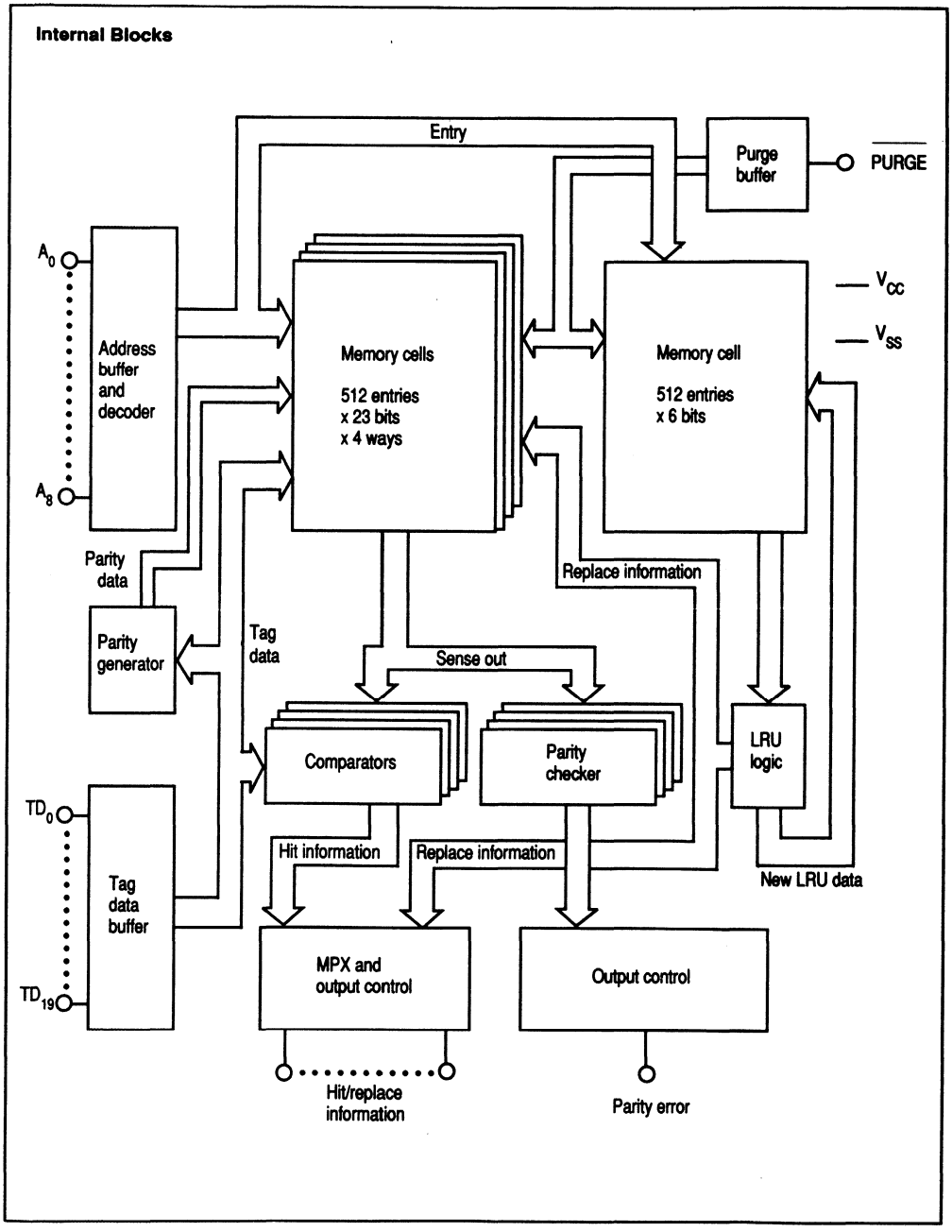
Symbol	Pin Name	Pin No.	I/O	Function
MODE	Mode	58	I	Mode selection MODE = H: 512-entry x 4-way MODE = L: 1024-entry x 2-way
A_0–A_9	Address	52, 21, 53, 22, 23, 24, 55, 25, 56, 26	I	Address inputs: A_9 is not used for 4-way; fix it to H or L
TD_0–TD_{19}	Tag Data	6, 41, 7, 42–45, 11, 12, 46, 13, 14, 15, 48, 16, 49, 17, 50, 18, 51	I	Tag information
$\overline{PURGE}$	Purge	57	I	All purge is done when $\overline{PURGE}$ = L
$\overline{INVL}$	Invalidate	33	I	Partial purge: V bit of specified address is forced to 0 (L)
SBLK	Way Select Enable	30	I	Enables external way selection in replacement and invalidation cycles
SB_0, SB_1	External Way Address	60, 31	I	External way address input: Enabled when SBLK = H
$\overline{WRITE}$	Write	62	I	Enables write
$\overline{SET}$	Set	34	I	Timing pulse Read cycle: Updates LRU Write cycle: Stores tag, sets V bits to H, and updates LRU Partial purge cycle: Shifts LRU and sets V bits to L
$\overline{INH}$	Inhibit	32	I	Inhibits all functions except all purge
H/R	Hit/Replace Selection	35	I	Output selection H/R = H: Hit information H/R = L: Replace information
RLATCH	Replace Latch	63	I	Latch control for replace information
$\overline{PINV}$	Parity Inversion	29	I	Used for testing only
$\overline{VINV}$	Validity Inversion	59	I	Used for testing only
MHENBL	$\overline{MHIT}$ Enable	9	I	Enables $\overline{MHIT}$ output
EXTH	External Hit Control	8	I	Forces $\overline{MHIT}$ output to L
$\overline{HIT}$	Hit	36	O	Hit output: NOR of HIT_0 to HIT_3
HC_0/RC_0 HC_1/RC_1	Hit/Replace Code	37, 38	O	Coded output of hit or replace information
HIT_{0-3}/ REP_{0-3}	Hit/Replace	3, 39, 4, 5	O	Uncoded output of hit or replace information
$\overline{PERR}$	Parity Error	64	O	Indicates parity error

Pin Description (cont.)

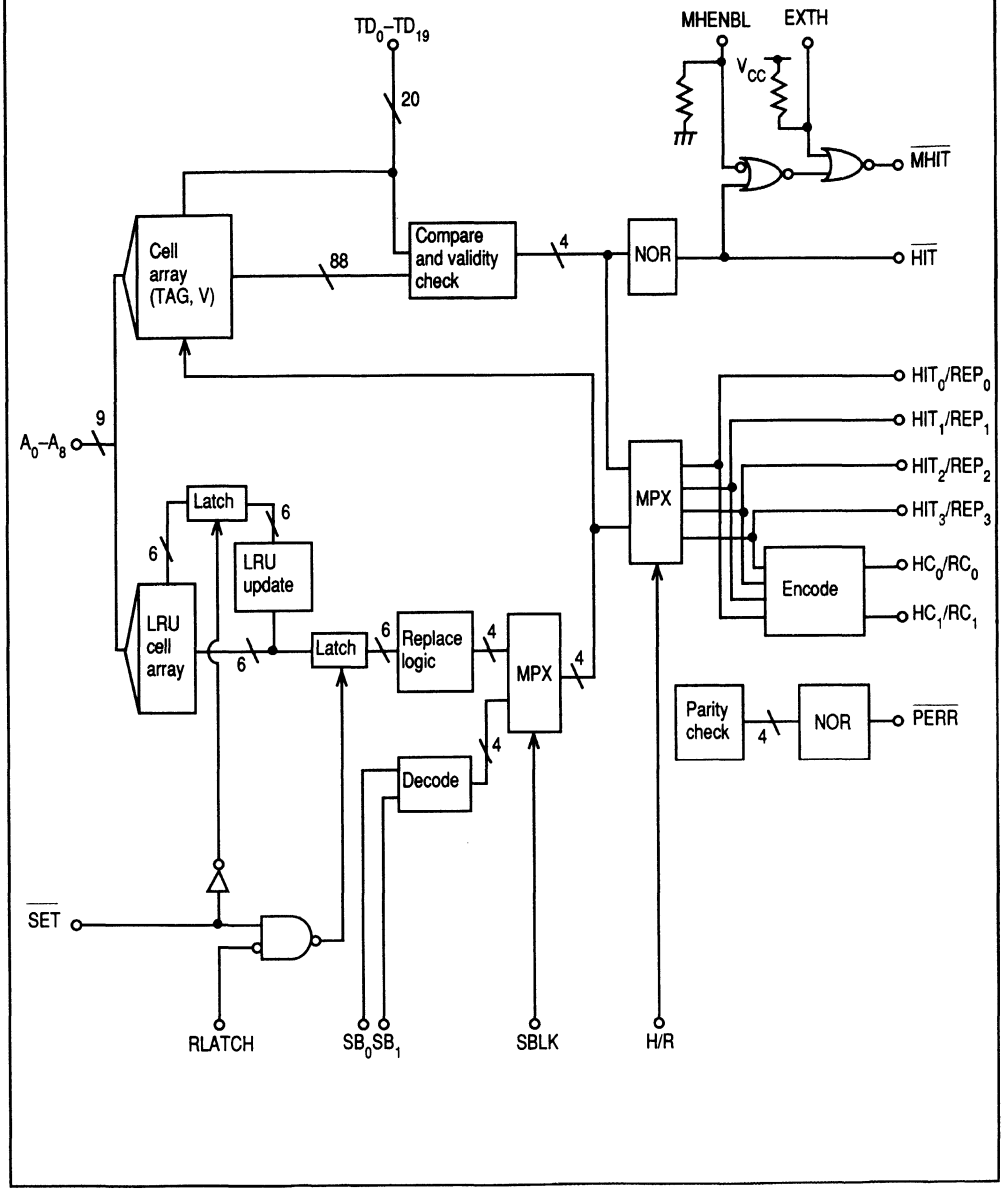
Symbol	Pin Name	Pin No.	I/O	Function
$\overline{MHIT}$	Modified Hit	2	O	Hit output modified by MHENBL and EXTH
V_{CC}	Power	47, 61	I	Connects to + 5V power supply
V_{SS}	Ground	40, 54	I	Connects to ground

Block Diagrams

Internal Blocks



Output Control Block



Function Tables

1. Basic Functions (all combinations not listed below are inhibited)

Input					Tag Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	Tag Bits	P Bit (Parity)	V Bits (Validity)	LRU Bits	Function Mode
L	H	×	×	×	No change	No change	No change	No change	Inhibit*3
H	H	H	×	×	No change	No change	No change	No change	Tag read
H	H	⊓	H	H	No change	No change	No change	No change*1 or updated	Tag read
H	H	⊓	L	H	TD_0–TD_{19}	Set	H	Updated	Tag write
×	L	H	×	×	Undefined	Undefined	L (All)	Initialized	All purge
H	H	⊓	H	L	No change	No change	No change L*2	No change*1 or shifted*4	Partial purge

×: H or L

Notes: *1 When SBLK = L and there is no hit, LRU is not changed.
*2 When SBLK = L and there is no hit, the V bits are not changed.
*3 In inhibit mode, $\overline{HIT}$ and $\overline{PERR}$ outputs are H but all other outputs are L with MHENBL and EXTH inputs, $\overline{MHIT}$ enters the logic state shown in the block diagram of output control block.
*4 Shifted means that the partially-purged way becomes the least recently used way.

2. Hit or Replace Information Output

Input		Internal Information*1, *2				Output							
MODE	A_9	hit_0/ rep_0	hit_1/ rep_1	hit_2/ rep_2	hit_3/ rep_3	HIT_0/ REP_0	HIT_1/ REP_1	HIT_2/ REP_2	HIT_3/ REP_3	HC_0/ RC_0	HC_1/ RC_1	$\overline{HIT}$*3	Mode
H	×	L	L	L	L	L	L	L	L	L	L	H	4-way
H	×	H	L	L	L	H	L	L	L	L	L	L	
H	×	L	H	L	L	L	H	L	L	H	L	L	
H	×	L	L	H	L	L	L	H	L	L	H	L	
H	×	L	L	L	H	L	L	L	H	H	H	L	
L	L	L	×	L	×	L	L	L	L	L	L	H	2-way
L	L	H	×	L	×	H	L	L	L	L	L	L	
L	L	L	×	H	×	L	L	H	L	L	H	L	
L	H	×	L	×	L	L	L	L	L	L	L	H	
L	H	×	H	×	L	L	H	L	L	H	L	L	
L	H	×	L	×	H	L	L	L	H	H	H	L	

×: H or L

Notes: *1 Internal information rep_0 to rep_3 is determined by on-chip LRU logic when SBLK = L. When SBLK = H, the internal information is determined by external signals SB_0 and SB_1.
*2 Correct operation is not guaranteed if 2 or more ways are hit at the same time.
*3 $\overline{HIT}$ output is valid when H/R = H.

3. Partial Purge ($\overline{INVL}$ = L)

Input					Internal Info.				Purged Way				$\overline{SET}$	
MODE	A_9	SBLK	SB_0	SB_1	hit_0	hit_1	hit_2	hit_3	0	1	2	3	LRU	Mode
H	×	L	×	×	L	L	L	L	—	—	—	—	No change	4-way
H	×	L	×	×	H	L	L	L	◎	—	—	—	Shifted	
H	×	L	×	×	L	H	L	L	—	◎	—	—	Shifted	
H	×	L	×	×	L	L	H	L	—	—	◎	—	Shifted	
H	×	L	×	×	L	L	L	H	—	—	—	◎	Shifted	
H	×	H	L	L	×	×	×	×	◎	—	—	—	Shifted	
H	×	H	H	L	×	×	×	×	—	◎	—	—	Shifted	
H	×	H	L	H	×	×	×	×	—	—	◎	—	Shifted	
H	×	H	H	H	×	×	×	×	—	—	—	◎	Shifted	
L	L	L	×	×	L	×	L	×	—	—	—	—	No change	2-way
L	L	L	×	×	H	×	L	×	◎	—	—	—	Shifted	
L	L	L	×	×	L	×	H	×	—	—	◎	—	Shifted	
L	L	H	L	L	×	×	×	×	◎	—	—	—	Shifted	
L	L	H	L	H	×	×	×	×	—	—	◎	—	Shifted	
L	H	L	×	×	×	L	×	L	—	—	—	—	No change	
L	H	L	×	×	×	H	×	L	—	◎	—	—	Shifted	
L	H	L	×	×	×	L	×	H	—	—	—	◎	Shifted	
L	H	H	H	L	×	×	×	×	—	◎	—	—	Shifted	
L	H	H	H	H	×	×	×	×	—	—	—	◎	Shifted	

Note: Correct operation is not guaranteed if 2 or more ways are hit at the same time.

4. Parity Error and V Bits*1

(n: 0 to 3)

pen	vn_0	vn_1	PEn	Hit Info.*2
L	L	L	L	—
L	L	H	H	Hit
L	H	L	H	Hit
L	H	H	L	Hit
H	L	L	L	—
H	L	H	H	Hit
H	H	L	H	Hit
H	H	H	H	Hit

pen: Internal parity error in way n
vn_0/vn_1: Duplicate validity bits.
PEn: Determined by the following equation:

$$PEn = (vn_0 + vn_1) \cdot pen + (vn_0 \oplus vn_1)$$

Notes: *1 $\overline{PERR}$ is the NOR of PE0 to PE3.
*2 Output information when internal hit is valid.

Absolute Maximum Ratings*1

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} *2	–0.5 to +7.0	V
Input Voltage at Any Pin Relative to V_{SS}	V_{in} *2	–3.0 to +7.0	V
Output Voltage at Any Pin Relative to V_{SS}	V_{out} *2	–0.5 to +7.0	V
Output Current	I_{out}	20	mA
Power Dissipation	P_T	1.5	W
Operating Temperature	T_{opr}	–10 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C

Note: *1 Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*2 All voltages are relative to V_{SS}.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC} *1	4.5	5.0	5.5	V
Input Low Voltage	V_{IL} *1	–0.5 *2	—	0.8	V
Input High Voltage	V_{IH} *1	2.2	—	6.0	V

Notes: *1 All voltages are relative to V_{SS}.

*2 –3.0 V for pulse width of 20 ns or less.

DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Power Supply Current	I_{CC}	Min. cycle, I_{out} = 0 mA	—	—	250	mA
Input Leakage Current	I_{IL}	V_{in} = V_{SS} to V_{CC}	–10	—	10	µA
Output Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V

Capacitances (T_a = 25°C, f = 1 MHz)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0 V	—	—	10	pF

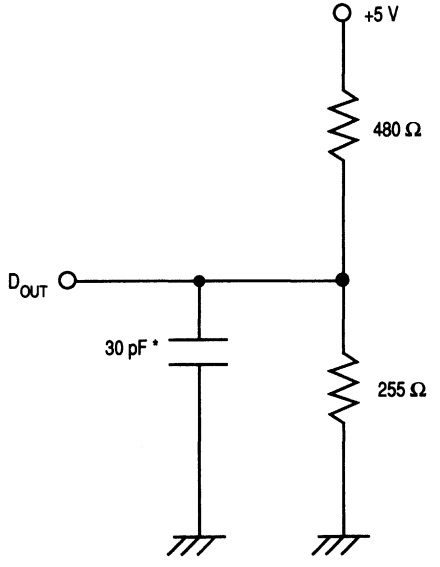
Note: These parameters are sampled, not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC}= 5 V ±10%, V_{SS}=0V, unless otherwise noted)

AC Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input pulse rise and fall times: 0 ns to 5 ns (time between 0.8 V and 2.2 V)
- Input and output timing reference levels: 1.5 V
- Output load: See figure.

Output Load



*Including scope and jig

1. Tag Read Cycle ($\overline{MODE}$ = H or L, $\overline{PURGE}$ = H, $\overline{WRITE}$ = H, $\overline{INVL}$ = H, $\overline{PINV}$ = H or L, $\overline{VINV}$ = H or L, $\overline{INH}$ = H)

Item	Symbol	HM644332Y-25 Min.	HM644332Y-25 Max.	HM644332Y-30 Min.	HM644332Y-30 Max.	Unit
Read Cycle Time	t_{RC}	50	—	50	—	ns
Address Valid to $\overline{HIT}$, HC_n, HIT_n	t_{AH}	—	25	—	30	ns
Address Valid to $\overline{MHIT}$	t_{AMH}	—	27	—	32	ns
Tag Data Valid to $\overline{HIT}$, HC_n, HIT_n	t_{TH}	—	18	—	18	ns
Tag Data Valid to $\overline{MHIT}$	t_{TMH}	—	20	—	20	ns
$\overline{HIT}$, HC_n, HIT_n Hold Time	t_{HH}	0	—	0	—	ns
Address Valid to RC_n, REP_n	t_{AR}	—	35	—	40	ns
Address Valid to $\overline{PERR}$	t_{AP}	—	35	—	40	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{SET}$	t_{TS}	25	—	25	—	ns
$\overline{SET}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{SET}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
RC_n, REP_n Hold Time for RLATCH	t_{RH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for RC_n, REP_n	t_{SBR}	—	25	—	25	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns
RC_n, REP_n Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{SET}$	t_{SBS}	25	—	25	—	ns
$\overline{PERR}$ Hold Time	t_{PH}	0	—	0	—	ns
H/R to Multiplex Output Change	t_{HR}	—	10	—	12	ns
MHENBL, EXTH to $\overline{MHIT}$ Output	t_{MMH}	—	10	—	12	ns

2. Tag Write Cycle (MODE = H or L, $\overline{\text{PURGE}}$ = H, $\overline{\text{WRITE}}$ = L, $\overline{\text{INVL}}$ = H, H/$\overline{\text{R}}$ = L, $\overline{\text{INH}}$ = H)

		HM644332Y-25		HM644332Y-30		
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Write Cycle Time	t_{WC}	50	—	50	—	ns
Address Valid to RC_n, REP_n	t_{AR}	—	35	—	40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25	—	25	—	ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Setup Time for RC_n, REP_n	t_{SBR}	—	25	—	25	ns
RC_n, REP_n Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK Hold Time	t_{SBH}	5	—	5	—	ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Setup Time for $\overline{\text{SET}}$	t_{IS}	25	—	25	—	ns
$\overline{\text{PINV}}$, $\overline{\text{VINV}}$ Recovery Time for $\overline{\text{SET}}$	t_{IR}	5	—	5	—	ns

3. Partial Purge (MODE = H or L, $\overline{\text{PURGE}}$ = H, $\overline{\text{WRITE}}$ = H, $\overline{\text{INVL}}$ = L, H/$\overline{\text{R}}$ = H or L, $\overline{\text{INH}}$ = H, RLATCH = L, $\overline{\text{PINV}}$ = H or L, $\overline{\text{VINV}}$ = H or L)

		HM644332Y-25		HM644332Y-30		
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Partial Purge Cycle	t_{PPC}	50	—	50	—	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25	—	25	—	ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5	—	5	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns

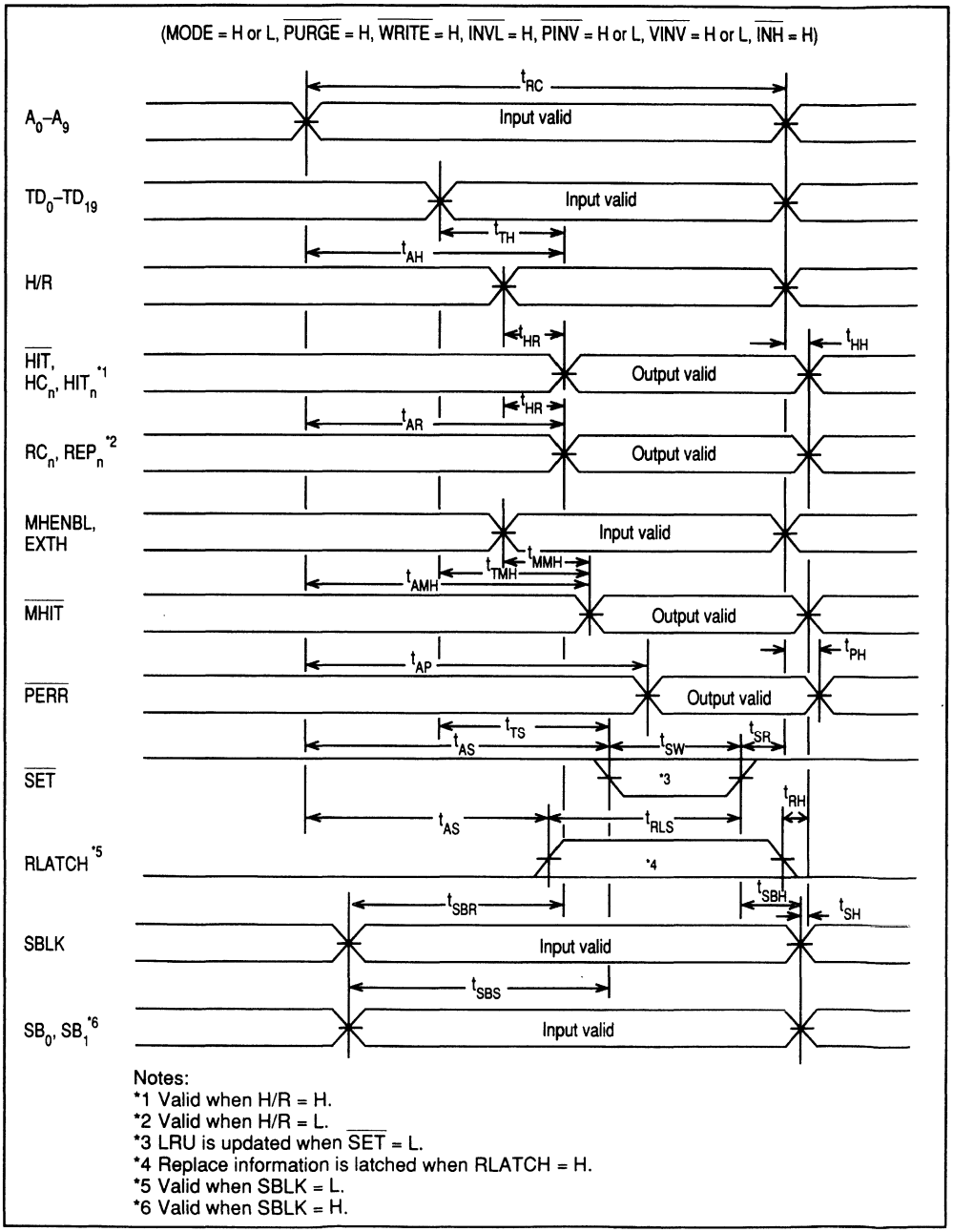
4. All Purge ($\overline{SET}$ = H, other control inputs are H or L)

Item	Symbol	HM644332Y-25 Min.	HM644332Y-25 Max.	HM644332Y-30 Min.	HM644332Y-30 Max.	Unit
All Purge Cycle Time	t_{APC}	100	—	100	—	ns
Purge Pulse Width	t_{PPW}	50	—	50	—	ns
Purge Recovery Time	t_{PR}	50	—	50	—	ns

Notes: 1. One cycle is defined as the time from address valid to address change. In all purge cycle, it is defined as the time from $\overline{PURGE}$ fall to the start of the next cycle.
2. The signals specified as H or L in the timing waveforms must be fixed in the cycle. The signals not specified can be H or L and changed in one cycle.
3. $\overline{INH}$, $\overline{PURGE}$, $\overline{WRITE}$ and $\overline{INVL}$, input signals to set modes, must be valid earlier than 25 ns before $\overline{SET}$ falls and held for move than 5 ns after $\overline{SET}$ rises. In all purge cycle, $\overline{PURGE}$ must be risen earlier than 50 ns before the next cycle starts and fixed H for more than 75 ns before $\overline{SET}$ falls.
4. MODE, $\overline{PINV}$ and $\overline{VINV}$ must be fixed H or L in the operation. The pins not used in the operation, such as A9 pin of 4-way organization, must be fixed H or L.
5. H/R, MHENBL and EXTH are input signals to control only outputs and those timings can be set asynchronously with the other inputs.

Timing Charts

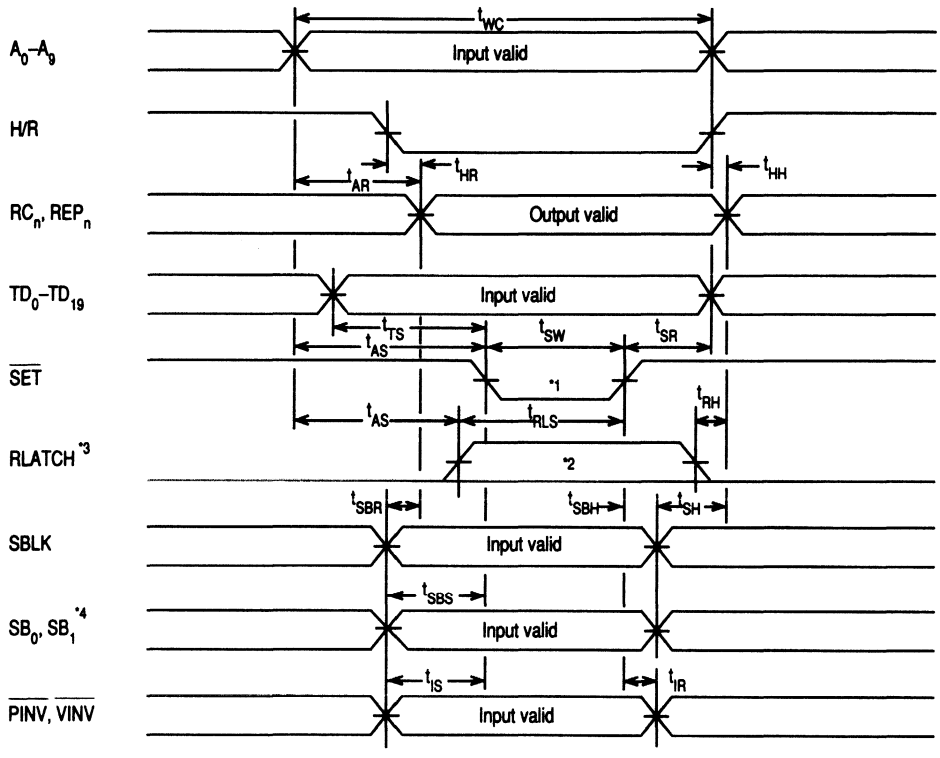
1. Tag Read Cycle



Notes:
*1 Valid when H/R = H.
*2 Valid when H/R = L.
*3 LRU is updated when $\overline{SET}$ = L.
*4 Replace information is latched when RLATCH = H.
*5 Valid when SBLK = L.
*6 Valid when SBLK = H.

2. Tag Write Cycle

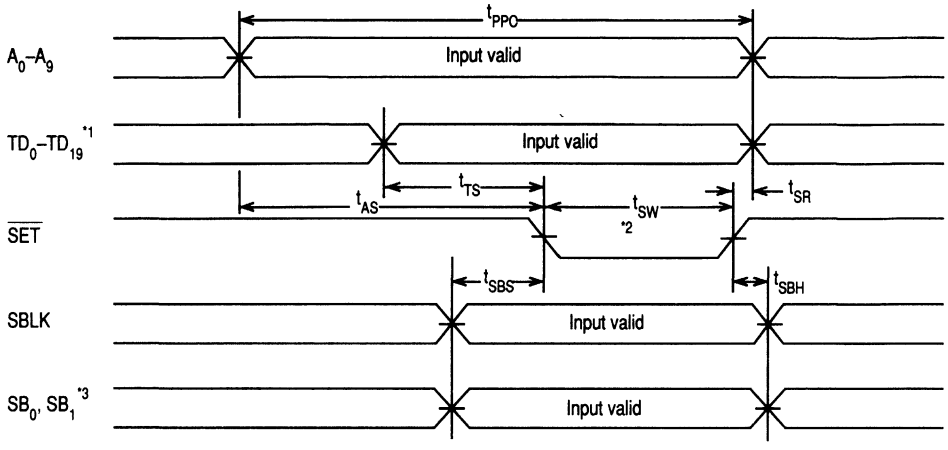
(MODE = H or L, $\overline{\text{PURGE}}$ = H, $\overline{\text{WRITE}}$ = L, $\overline{\text{INVL}}$ = H, $\overline{\text{INH}}$ = H)



Notes:
*1 Tag is stored, V bits go H, and LRU is updated.
*2 Replace information is latched when RLATCH = H.
*3 Valid when SBLK = L.
*4 Valid when SBLK = H.

3. Partial Purge Cycle

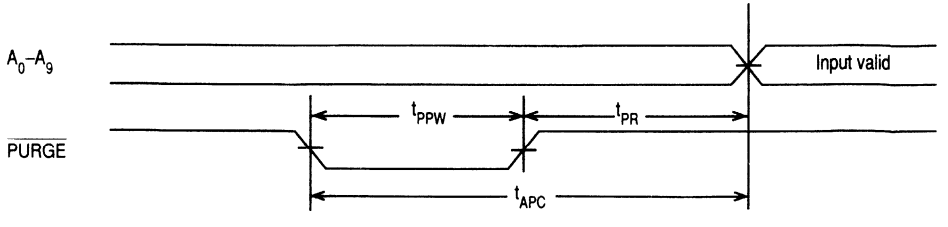
(MODE = H or L, $\overline{\text{PURGE}}$ = H, $\overline{\text{WRITE}}$ = H, $\overline{\text{INVL}}$ = L, H/$\overline{\text{R}}$ = H or L, $\overline{\text{INH}}$ = H, RLATCH = L, $\overline{\text{PINV}}$ = H or L, $\overline{\text{VINV}}$ = H or L)



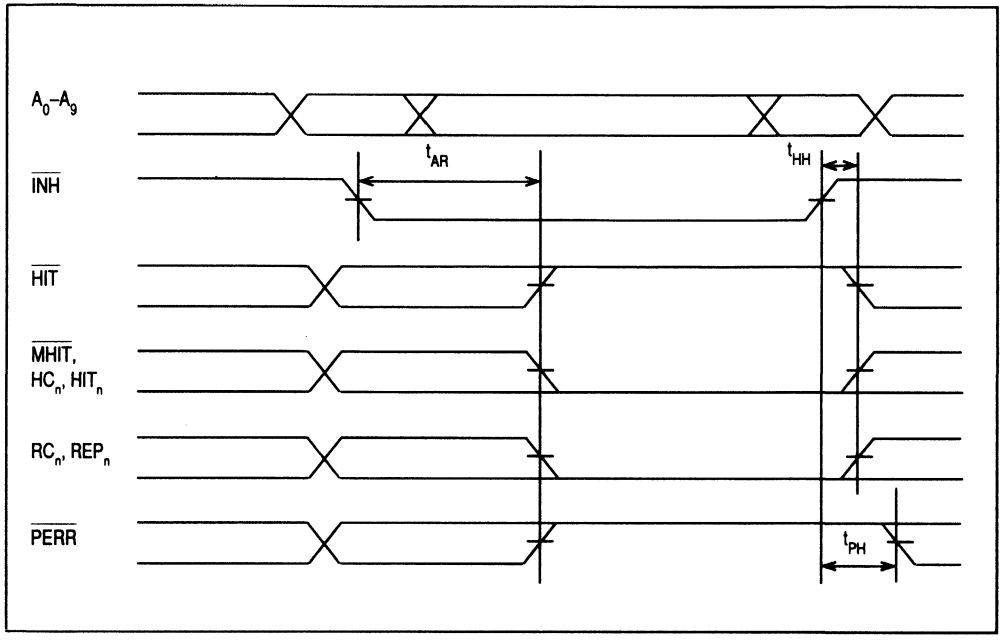
Notes:
*1 Valid when SBLK = L.
*2 LRU is shifted and V bits go L.
*3 Valid when SBLK = H.

4. All Purge Cycle

($\overline{\text{SET}}$ = H, other control inputs are H or L)



5. Inhibit Mode Cycle



Function Description

Tag Read

The TAG input data (TD_0–TD_{19}) and the contents of the addressed location are compared. If they are the same, a hit is assumed. $\overline{HIT}$ goes low and the HCn and HITn outputs indicate the hit way associatively. If there is no hit, the LRU logic of the tag RAM automatically specifies which way is to be replaced.

The replacement information is presented at the RCn and REPn outputs by forcing the H/R input low. These signals will be latched and used for writing data into data memory.

Tag Write

If there is no hit, the tag RAM must be updated. A write operation is performed by setting $\overline{WRITE}$ low and inputting a $\overline{SET}$ pulse. The tag data will be written into the appropriate way by the internal LRU logic.

The way can be also specified externally by using SBLK, SB_0, and SB_1 inputs. In tag write mode, the V bits (validity bits) and the parity bit are set, and the LRU is updated.

All Purge

By asserting the $\overline{PURGE}$ input low, all the V bits are reset and LRU is initialized.

In this operation, the contents of each tag and its parity will not be identified.

Partial Purge

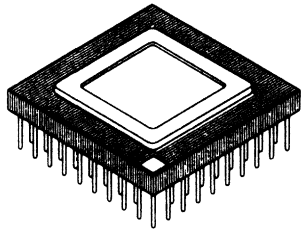
A partial purge operation is performed by setting $\overline{INVL}$ low and inputting a $\overline{SET}$ pulse.

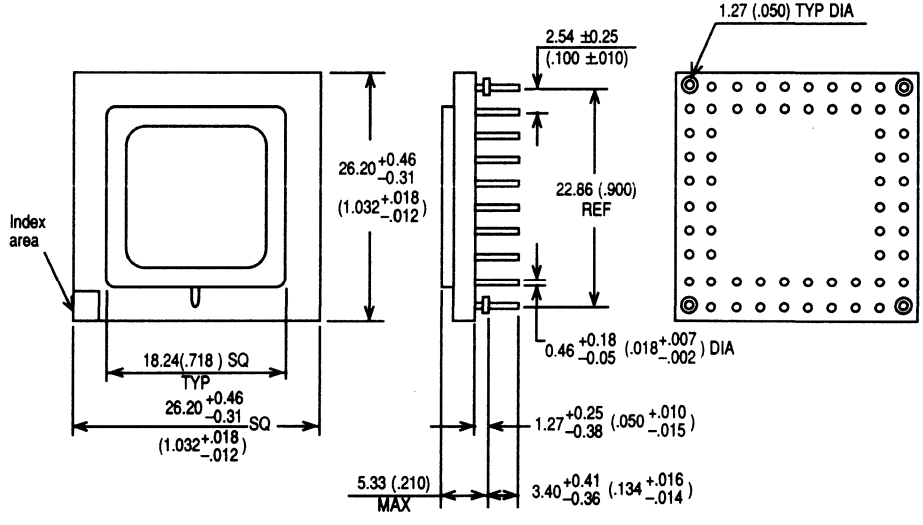
The V bit specified by the address input is reset and the LRU is shifted so that the partially-purged way becomes the least recently used way.

Package Dimensions

Unit: mm (inches)

64-Pin Ceramic PGA





HM62A168, HM62A188 Series

Direct Mapped 8,192-Word × 16 (18)-Bit/2-Way 4,096-Word × 16 (18)-Bit Static Cache Memory

The Hitachi HM62A168/188 is a high speed 128 (144)-k cache memory organized as 2-way set associative 4 k × 16 (18) or direct mapped 8 k × 16 (18).
By using two HM62A168/188 with INTEL's 82385 cache controller can be achieved high performance 80386 system.
The HM62A168/188, packaged in a 52-pin PLCC is available for high density mounting.

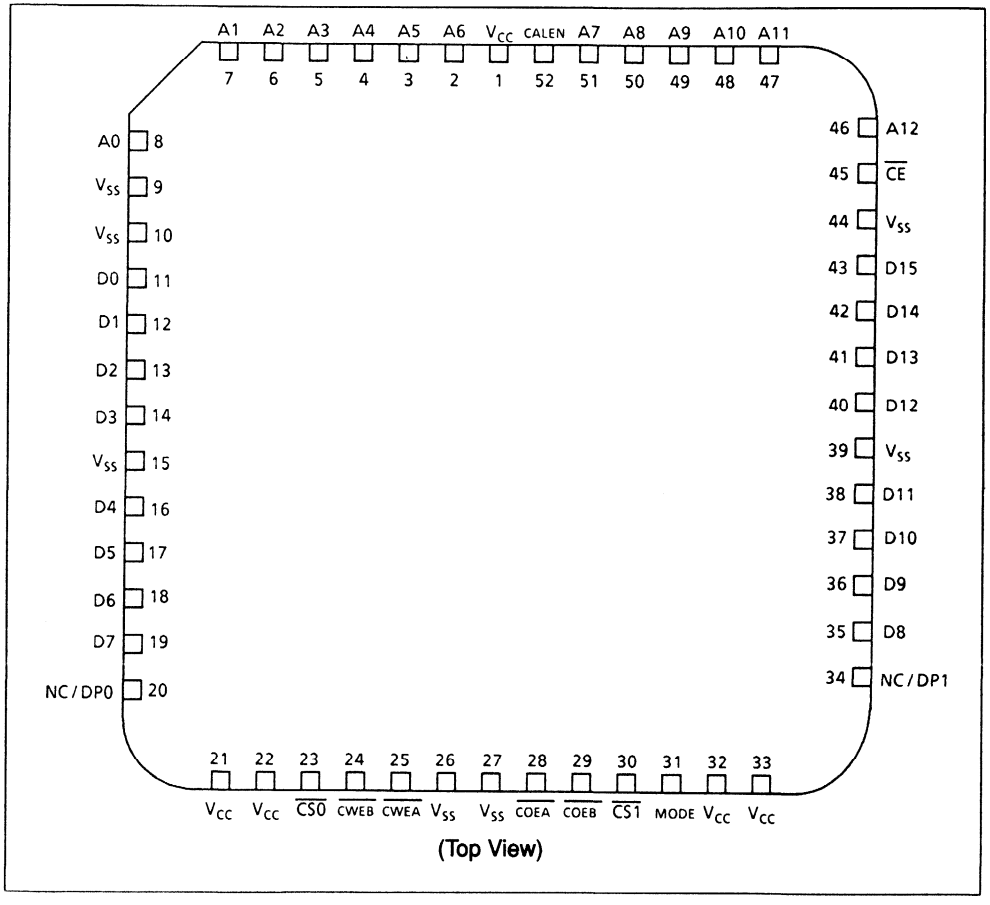
Features

- Single 5 V supply and high density 52-pin PLCC package
- Meets INTEL 82385 cache memory controller
- High speed:
  Access time: 25/35/45 ns (max)
- Directly TTL compatible
  All inputs and outputs
- Address latch
- Pin programmable for 8 k × 16 (18) or 2-way 4 k × 16 (18)

Ordering Information

Type No.	Access	Package
HM62A168CP-25	25 ns	52-pin PLCC (CP-52)
HM62A168CP-35	35 ns	
HM62A168CP-45	45 ns	
HM62A188CP-25	25 ns	
HM62A188CP-35	35 ns	
HM62A188CP-45	45 ns	

Pin Arrangement



(Top View)

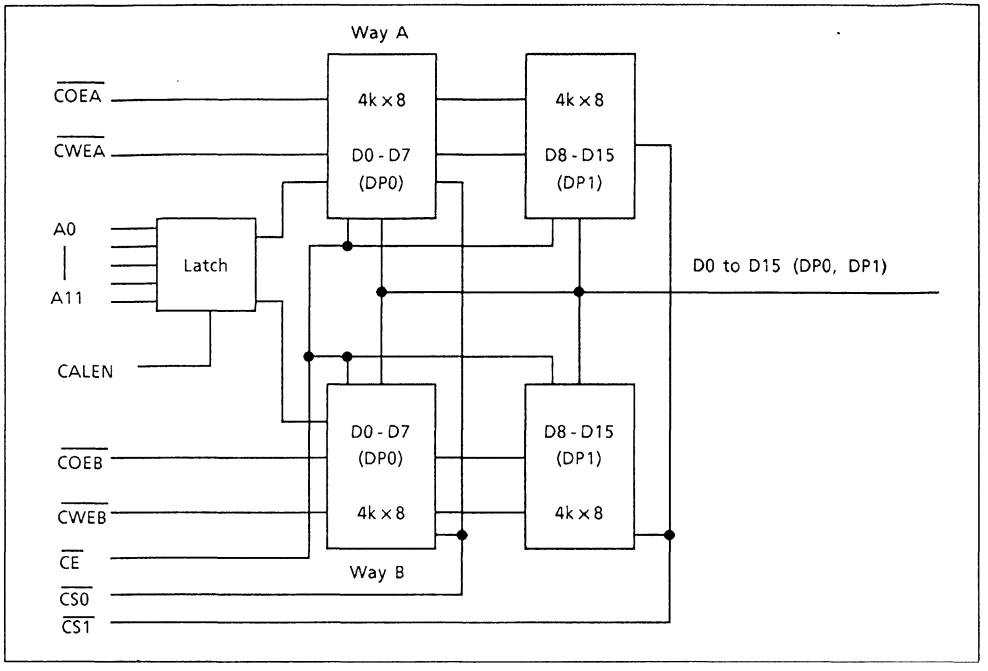
Pin Description

Pin name	Function
CALEN	Cache address latch enable
MODE	Mode select
A0 to A12	Address
$\overline{CS0}$, $\overline{CS1}$	Cache chip select
$\overline{COEA}$, $\overline{COEB}$	Cache output enable

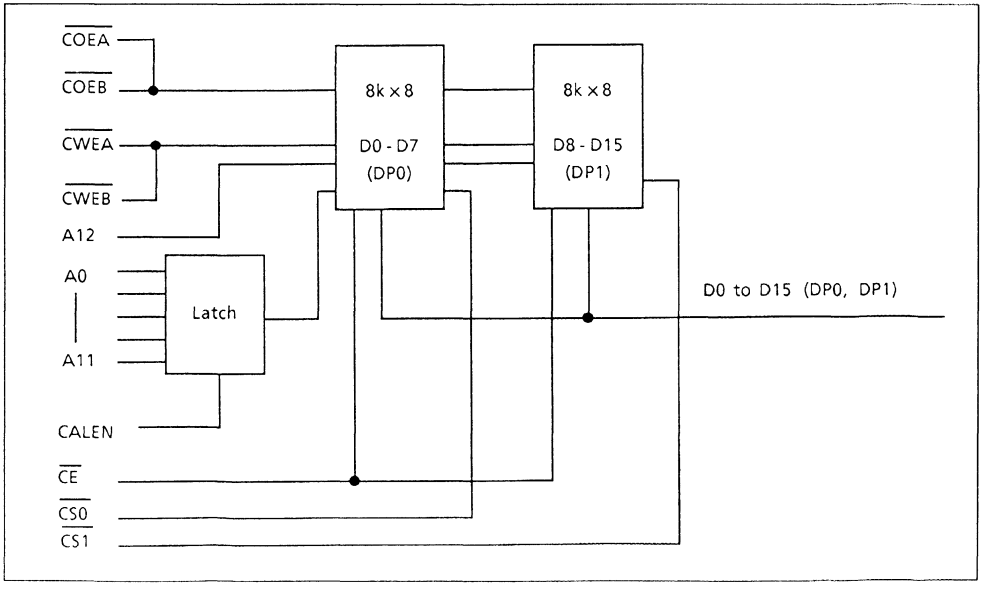
Pin name	Function
$\overline{CWEA}$, $\overline{CWEB}$	Cache write enable
D0 to D15	Data input/output
$\overline{CE}$	Cache chip enable
NC	No connection
DP0, DP1	Parity input/output

Block Diagram

Topology Two-Way Set Associative (MODE = logic high)



Topology Direct Mapped(MODE = logic low)



Signal Description

Signal name	Pin No.	Signal Description
A0 – A6 A7 – A11	8 – 2 51 – 47	Address inputs to the memory array. A0 – A11 are latched on the falling edge of CALEN.
A12	46	A12 address input. In the two-way mode, address input A12 will be a "don't care" and should be externally wired to ground. In the direct-mapped mode, when MODE is connected to V_{SS}, A12 selects which of the two 4 k × 16 (18) banks is read from or written to. A12 is not latched by CALEN, as are the other address inputs.
CALEN	52	Cache address latch enable input. This signal controls the internal address latches for inputs A0 – A11. When CALEN is high, the latch is transparent. The falling edge of CALEN latches the current address input levels. A12 is static and is not controlled by CALEN.
D0 – D15	11 – 14, 16 – 19 35 – 38, 40 – 43	Data inputs and outputs. These are the three-state lines that provide data access to the memory array.
MODE	31	MODE input. This signal controls whether the memory device is to be used in a direct-mapped configuration (8 k × 16 (18)) or as a two-way set-associative configuration (two 4 k × 16 (18)). When the MODE signal is high, the device is placed in the two-way mode. When the mode input is low, the cache is in the direct-mapped mode. This is a hardwired strap option and must not be changed dynamically.
$\overline{CS0}$, $\overline{CS1}$	23, 30	Cache chip select inputs. These active low signals selectively enable the two bytes of memory. $\overline{CS0}$ low enables bits D0 – D7 and DP0. $\overline{CS1}$ low enables bits D8 – D15 and DP1. This applies to both the direct-mapped and two-way modes.
$\overline{CE}$	45	Cache chip enable input (active low). This signal functions as a global chip enable. It gates the $\overline{OEA}$, $\overline{OEB}$, $\overline{WEA}$, and $\overline{WEB}$ inputs. A chip enable controlled write can be done by taking $\overline{CE}$ inactive high while one of the $\overline{WEX}$ signals is active (assuming all other timings for a write cycle are met).
$\overline{OEA}$, $\overline{OEB}$	28, 29	Cache output enable inputs. These active low inputs enable cache bank A or bank B to drive the data bus when in the two-way mode. In the two-way mode, bank A is enabled when $\overline{OEA}$ is low and bank B is enabled when $\overline{OEB}$ is low. If both banks are activated at the same time, then both banks become deselected. In the direct-mapped mode, $\overline{OEA}$ and $\overline{OEB}$ must be tied together externally. A low on $\overline{OEA}$ and $\overline{OEB}$ then enables the outputs of the 8 k × 16 (18) memory. A12 is used to determine which 4 k × 16 (18) bank is accessed.
$\overline{WEA}$, $\overline{WEB}$	25, 24	Cache write enable inputs (active low). In the two-way mode when $\overline{WEA}$ ($\overline{WEB}$) is active, data is written into memory bank A (B). In the direct-mapped mode, $\overline{WEA}$ and $\overline{WEB}$ must be tied together externally. A low on $\overline{WEA}$ and $\overline{WEB}$ enables data to be written into the 8 k × 16 (18) memory. A12 is used to determine which 4 k × 16 (18) bank is accessed.

Signal Description (cont)

Signal name	Pin No.	Signal Description
DP0 or NC, DP1 or NC	20, 34	Parity data inputs and outputs (HM62A188). These are three-state lines that provide parity data access to the memory array. For the HM62A168, these two pins are not used (NC) and must not be physically tied to V_{CC}, V_{SS}, or any other device inputs.
V_{CC}	1, 21, 22, 32, 33	System power +5 V
V_{SS}	9, 10, 15, 26, 27, 39, 44	System ground

Function Table

Two-Way Mode (Mode = High), 2-4 k × 16 (18)

Input signal							I/O pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	D0 – D7 (DP0)	D8 – D15 (DP1)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output high-Z
X	X	X	L	L	X	X	High-Z	High-Z	Output high-Z
L	L	H	L	H	H	H	Output	High-Z	Read way A
L	L	H	H	L	H	H	Output	High-Z	Read way B
L	H	L	L	H	H	H	High-Z	Output	Read way A
L	H	L	H	L	H	H	High-Z	Output	Read way B
L	L	L	L	H	H	H	Output	Output	Read way A
L	L	L	H	L	H	H	Output	Output	Read Way B
L	L	H	X	X	L	H	Input	High-Z	Write way A
L	L	H	X	X	H	L	Input	High-Z	Write way B
L	H	L	X	X	L	H	High-Z	Input	Write way A
L	H	L	X	X	H	L	Hihg-Z	Input	Write way B
L	L	L	X	X	L	H	Input	Input	Write way A

Two-Way Mode (Mode = High), 2-4 k × 16 (18) (cont)

Input signal							I/O pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	D0 – D7 (DP0)	D8 – D15 (DP1)	Function
L	L	L	X	X	H	L	Input	Input	Write way B
L	L	H	X	X	L	L	Input	High-Z	Write way A and B
L	H	L	X	X	L	L	High-Z	Input	Write way A and B
L	L	L	X	X	L	L	Input	Input	Write way A and B

Direct Mode (Mode = Low), 8 k × 16 (18)

Input signal							I/O pin		
$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	D0 – D7 (DP0)	D8 – D15 (DP1)	Function
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Output High-Z
L	L	H	L	L	H	H	Output	High-Z	Read D0 to D7
L	H	L	L	L	H	H	High-Z	Output	Read D8 to D15
L	L	L	L	L	H	H	Output	Output	Read D0 to D15
L	L	H	X	X	L	L	Input	High-Z	Write D0 to D7
L	H	L	X	X	L	L	High-Z	Input	Write D8 to D15
L	L	L	X	X	L	L	Input	Input	Write D0 to D15

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Vin	−0.5 *1 to +7.0	V
Power dissipation	P_T	2.0	W
Operation temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: 1. Vin min = −2.5 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5 *1	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ *1	Max	Unit	Test conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	V_{CC} = max Vin = V_{SS} to V_{CC}
Output leakage current	$\|I_{LO}\|$	—	—	10.0	µA	Output disable $V_{I/O}$ = V_{SS} to V_{CC}
Active Operating power supply current	I_{CC1}	—	—	220	mA	Vin = V_{SS}/V_{CC} $I_{I/O}$ = 0 mA Min cycle, duty = 100%
Operating power supply current	I_{CC2}	—	—	120	mA	Vin = V_{SS}/V_{CC}, Iout = 0 mA 2 x Min cycle, duty = 100%
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −1.0 mA

Note: 1. Typical limits are at V_{CC} = 5.0 V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz) *1

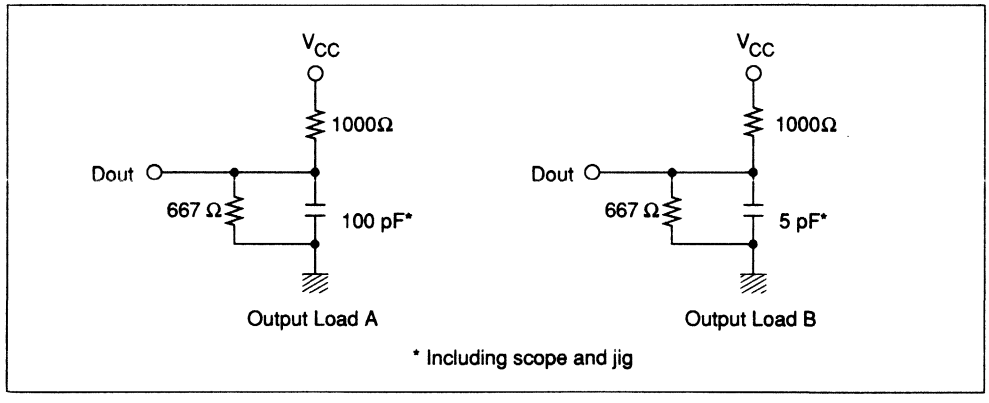
Parameter	Symbol	Min	Max	Unit	Test conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	TBD	pF	$V_{I/O}$ = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

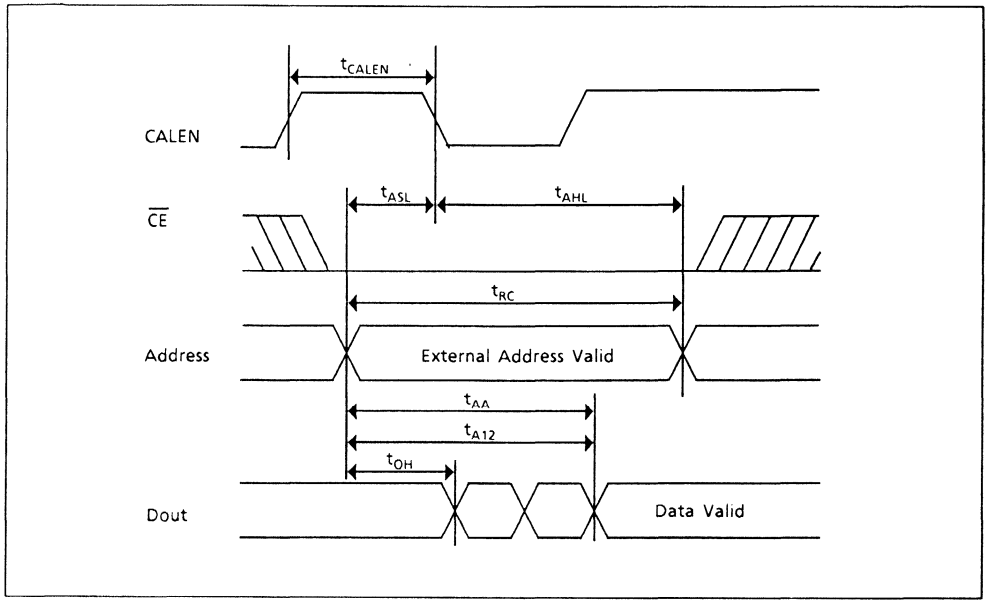
- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



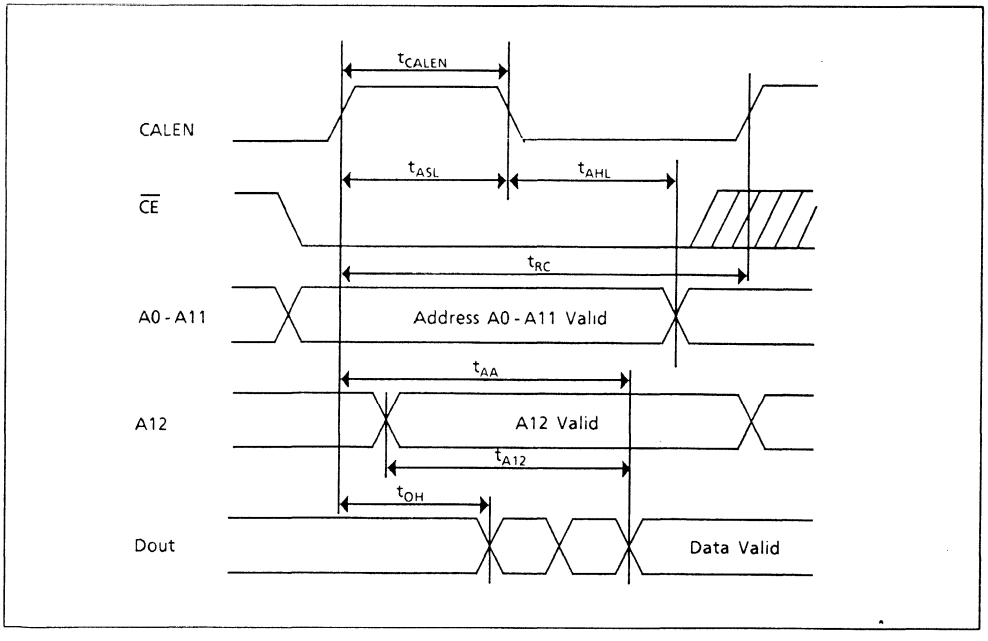
Read Cycle

Parameter	Symbol	HM62A168/188 -25		HM62A168/188 -35		HM62A168/188 -45		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	45	—	ns
Address access time	t_{AA}	—	25	—	35	—	45	ns
A12 address access time	t_{A12}	—	17	—	25	—	30	ns
Chip select access time	t_{CS}	—	20	—	25	—	35	ns
Chip enable access time	t_{CE}	—	20	—	25	—	35	ns
Output enable to output valid	t_{OE}	—	10	—	13	—	16	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Chip select to output low-Z	t_{LZ}	3	—	3	—	3	—	ns
Chip enabnle low to output low-Z	t_{LZE}	5	—	5	—	5	—	ns
Output enable to output low-Z	t_{OLZ}	2	—	2	—	2	—	ns
Chip deselect to output high-Z	t_{HZ}	—	15	—	25	—	30	ns
Chip enable high to output high-Z	t_{HZE}	—	15	—	25	—	30	ns
Output disable to output high-Z	t_{OHZ}	—	10	—	14	—	14	ns
Address latch enable pulse width	t_{CALEN}	8	—	10	—	15	—	ns
Address setup to latch low	t_{ASL}	4	—	6	—	10	—	ns
Address hold to latch low	t_{AHL}	5	—	5	—	5	—	ns

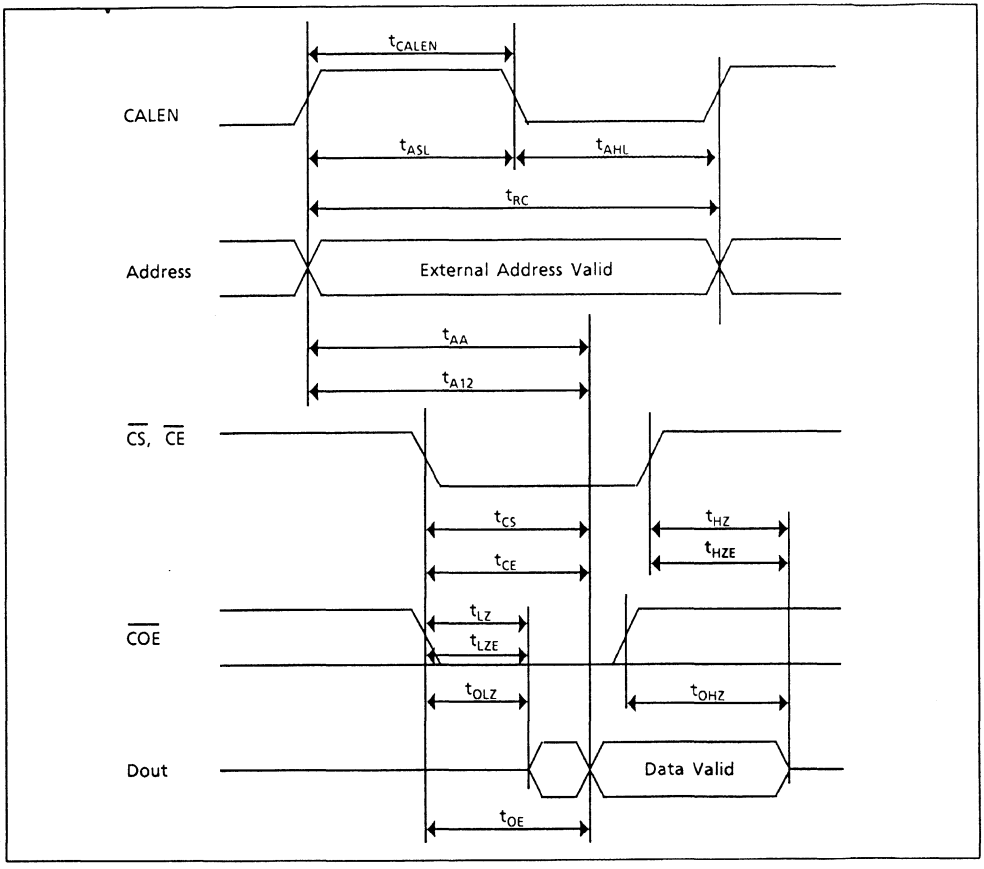
Read Timing Waveform (1) ($\overline{CWE}$ = high, $\overline{COE}$ = low, $\overline{CS}$ = low)



Read Timing Waveform (2) ($\overline{CWE}$ = high, $\overline{COE}$ = low, $\overline{CS}$ = low)



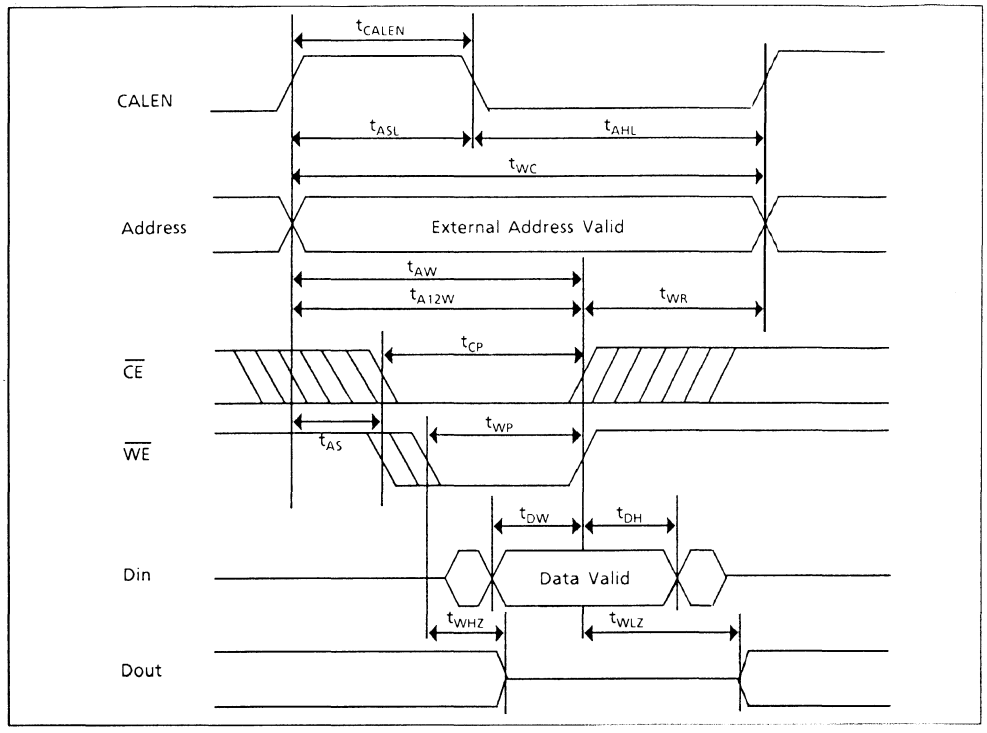
Read Timing Waveform (3) ($\overline{CWE}$ = high)



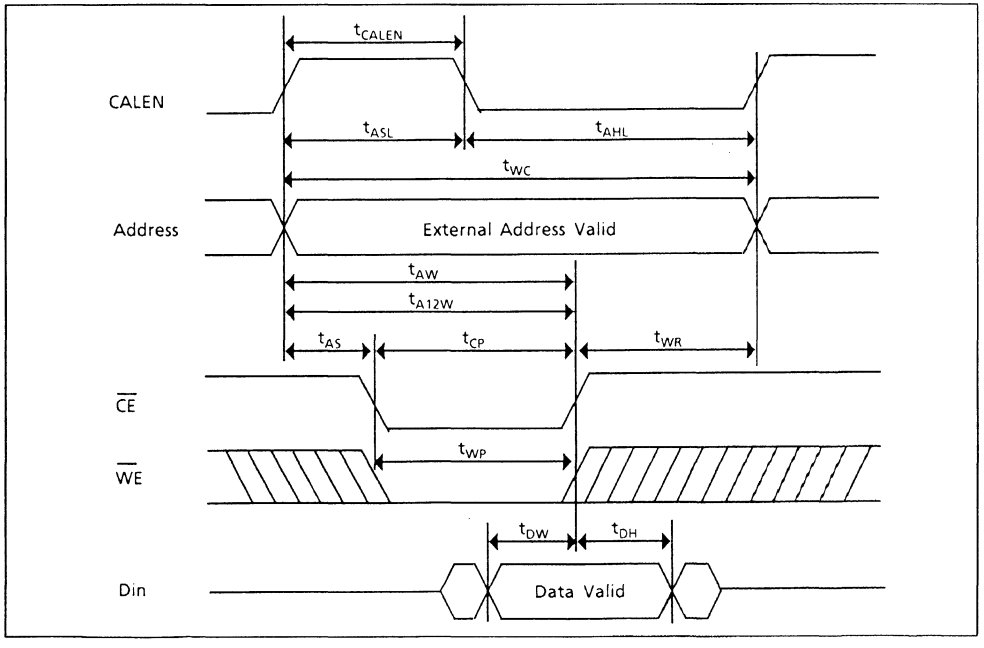
Write Cycle

Parameter	Symbol	HM62A168/188 -25		HM62A168/188 -35		HM62A168/188 -45		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	45	—	ns
Address valid to end of write	t_{AW}	18	—	25	—	40	—	ns
A12 valid to end of write	t_{A12W}	18	—	25	—	40	—	ns
Chip select to end of write	t_{CW}	18	—	25	—	30	—	ns
Data valid to end of write	t_{DW}	10	—	10	—	15	—	ns
Data hold from end of write	t_{DH}	0	—	0	—	0	—	ns
Write enable active to high-Z	t_{WHZ}	—	15	—	15	—	20	ns
Write enable inactive to low-Z	t_{WLZ}	3	—	3	—	3	—	ns
Write pulse width	t_{WP}	18	—	25	—	30	—	ns
$\overline{CE}$ pulse width during chip enable controlled write	t_{CP}	18	—	25	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time	t_{WR}	0	—	0	—	2	—	ns
Address latch enable pulse width	t_{CALEN}	8	—	10	—	15	—	ns
Address setup to latch low	t_{ASL}	4	—	6	—	10	—	ns
Address hold to latch low	t_{AHL}	5	—	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{COE}$ = high, $\overline{WE}$ controlled)



Write Timing Waveform (2) ($\overline{COE}$ = high, $\overline{CE}$ controlled)



MOS DYNAMIC RAM

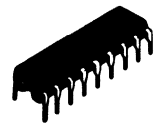
HM50464 Series

65536-word x 4-bit Dynamic Random Access Memory

■ FEATURES

- Page mode capability
- Single 5V (±10%)
- On chip substrate bias generator
- Low power: 350 mW active, 20 mW standby
- High speed: Access Time 120ns/150ns/200ns
- Output data controlled by $\overline{CAS}$ or $\overline{OE}$
- TTL compatible
- 256 refresh cycles . . . . . 4 ms
- 3 variations of refresh . . . . . $\overline{RAS}$ only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh
  Hidden refresh

HM50464P Series



(DP-18B)

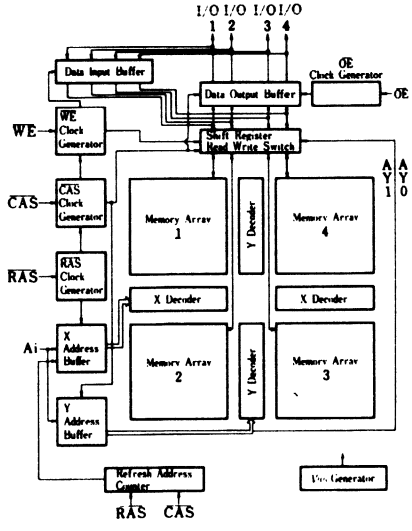
HM50464CP Series

(CP-18)

■ ORDERING INFORMATION

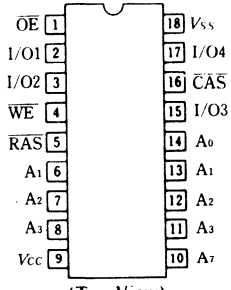
Type No.	Access Time	Package
HM50464P-12	120ns	300 mil 18 pin Plastic DIP
HM50464P-15	150ns	
HM50464P-20	200ns	
HM50464CP-12	120ns	18 pin PLCC
HM50464CP-15	150ns	
HM50464CP-20	200ns	

■ BLOCK DIAGRAM



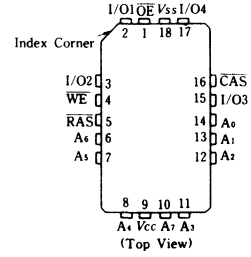
■ PIN ARRANGEMENT

● HM50464P Series



(Top View)

● HM50464CP Series



(Top View)

$A_0 - A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/O1 – I/O4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_7$ (Row)	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1 to +7	V
Supply Voltage relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature (Ambient)	*Topr*	0 to +70	°C
Storage Temperature (Ambient)	*Tstg*	−55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	*Iout*	50	mA

■ RECOMMENDED DC OPERATING CONDITION (Ta = 0 to +70°C)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	–	6.5	V
Input Low Voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltage referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Operating Current (t_{RC} = min.)	I_{CC1}	–	83	–	70	–	55	mA	1
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Disable)	I_{CC2}	–	4.5	–	4.5	–	4.5	mA	
Refresh Current ($\overline{RAS}$ only refresh, t_{RC} = min.)	I_{CC3}	–	62	–	53	–	42	mA	
Standby Current ($\overline{RAS}$ = V_{IH}, Dout = Enable)	I_{CC5}	–	10	–	10	–	10	mA	1
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ refresh, t_{RC} = min.)	I_{CC6}	–	69	–	58	–	45	mA	1
Operating Current (Page mode, t_{PC} = min.)	I_{CC7}	–	57	–	48	–	37	mA	1
Input Leakage Current (0 < *Vin* < 7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output Leakage Current (0 < *Vout* < 7V, Dout = Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output High Voltage (*Iout* = −5 mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage (*Iout* = 4.2 mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	typ.	max.	Unit	Note
Input Capacitance	Address	*CI1*	–	5	pF	1
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	*CI2*	–	10	pF	1
Output Capacitance	Data In/Data Out	*CI/O*	–	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{RAS}$	t_{RAC}	–	120	–	150	–	200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}	–	60	–	75	–	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{CAS}$	t_{OFF1}	–	30	–	40	–	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	–	260	–	330	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	90	–	100	–	120	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	

(to be continued)

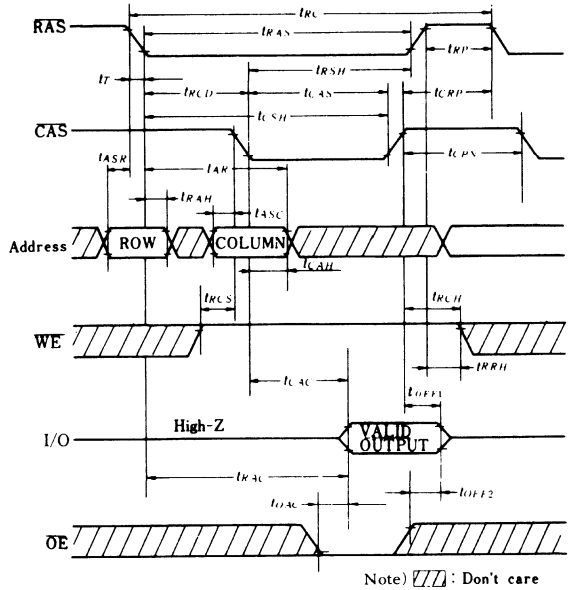
Parameter	Symbol	HM50464-12		HM50464-15		HM50464-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	25	–	30	–	ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80	–	100	–	130	–	ns	
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	40	–	45	–	55	–	ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100	–	120	–	155	–	ns	
Write Command Pulse Width	t_{WP}	40	–	45	–	55	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40	–	45	–	55	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40	–	45	–	55	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	40	–	45	–	55	–	ns	9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100	–	120	–	155	–	ns	
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	4	–	4	–	4	ms	
Read-Write Cycle Time	t_{RWC}	305	–	360	–	450	–	ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	100	–	125	–	160	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	160	–	200	–	260	–	ns	8
$\overline{CAS}$ Precharge Time	t_{CPN}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ refresh)	t_{CHR}	120	–	150	–	200	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0	–	0	–	0	–	ns	
Access Time from $\overline{OE}$	t_{OAC}	–	30	–	35	–	45	ns	
Output Buffer Turn-off Delay referenced to $\overline{OE}$	t_{OFF2}	–	30	–	40	–	50	ns	
$\overline{OE}$ to Data-in Delay Time	t_{ODD}	30	–	40	–	50	–	ns	
$\overline{OE}$ Hold Time referenced to $\overline{WE}$	t_{OEH}	25	–	30	–	40	–	ns	
Page Mode Cycle Time	t_{PC}	120	–	145	–	190	–	ns	
$\overline{CAS}$ Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	
$\overline{CAS}$ Read-modify-write Cycle Time (Page-mode)	t_{PCM}	205	–	245	–	310	–	ns	

Notes)

1. AC measurements assume t_T = 5ns.
2. Assume that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively be t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization of cycles.
11. Minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh is required before using internal refresh counter.
12. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

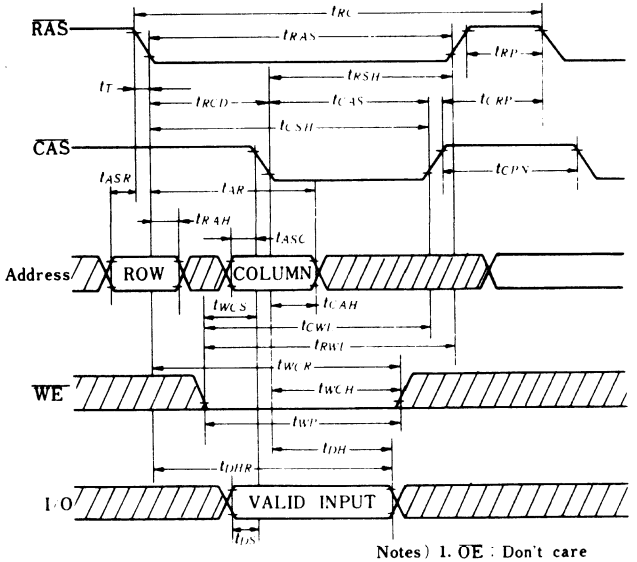
■ TIMING WAVEFORMS

• READ CYCLE



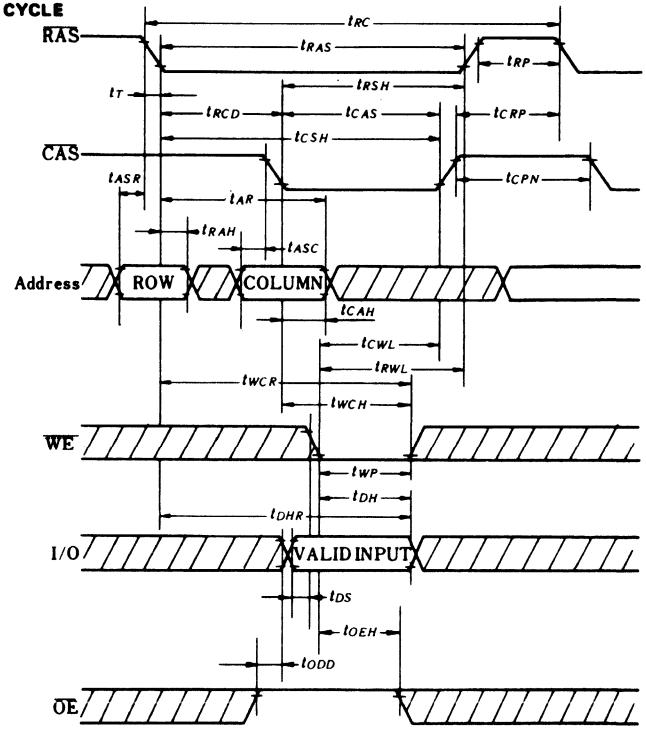
Note) ▨ : Don't care

• EARLY WRITE CYCLE



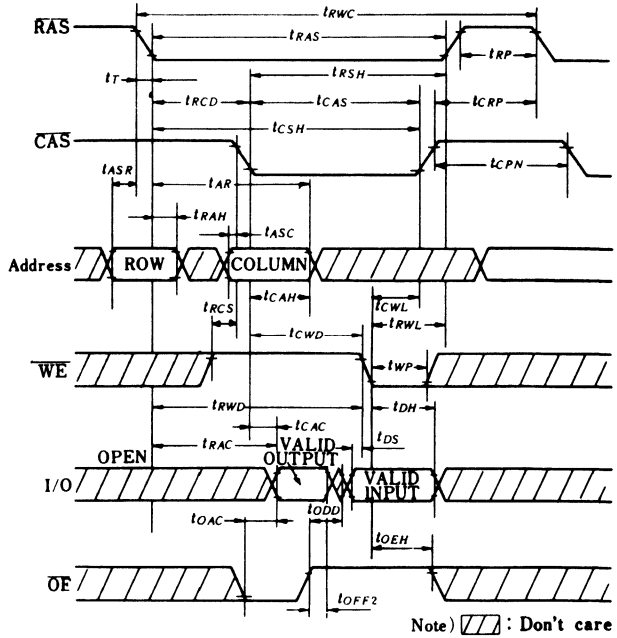
Notes) 1. $\overline{OE}$: Don't care
2. ▨ : Don't care

- **DELAYED WRITE CYCLE**



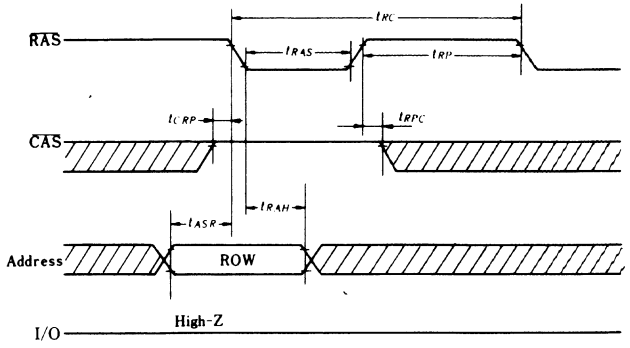
Note) ▨ : Don't care

- **READ MODIFY WRITE CYCLE**



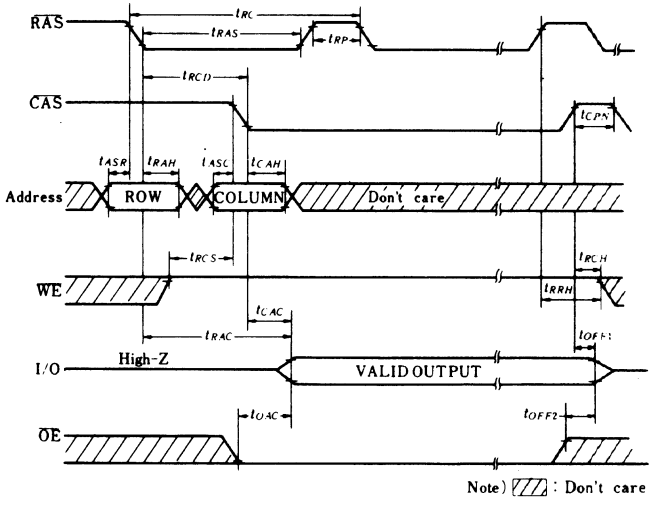
Note) ▨ : Don't care

- **$\overline{RAS}$ ONLY REFRESH CYCLE**



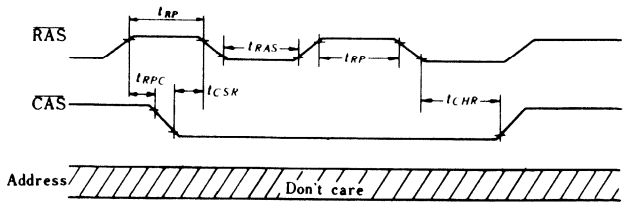
Notes) 1. $\overline{OE}$, $\overline{WE}$: Don't care
2. ▨ : Don't care

- **HIDDEN REFRESH CYCLE**

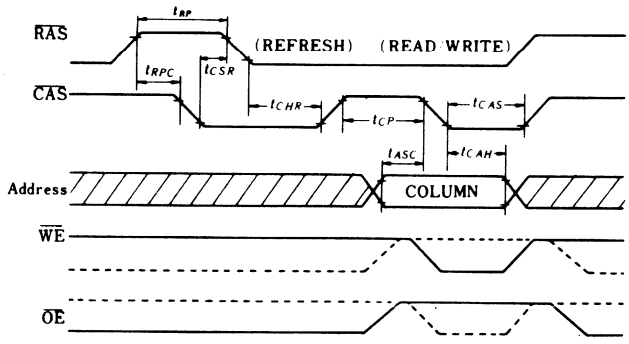


Note) ▨ : Don't care

- **$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE**

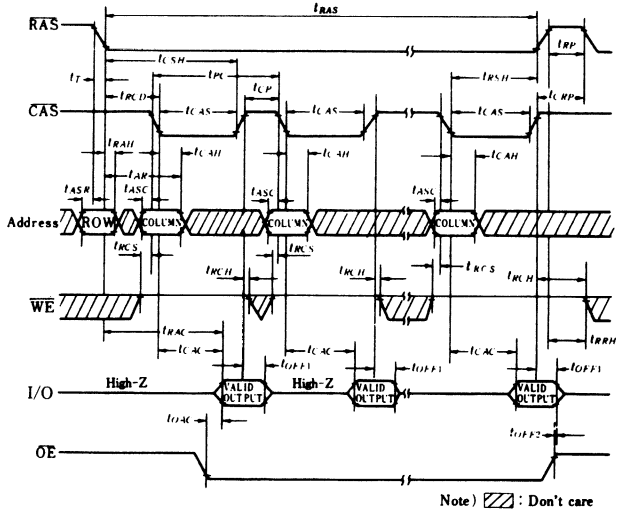


- **COUNTER TEST**



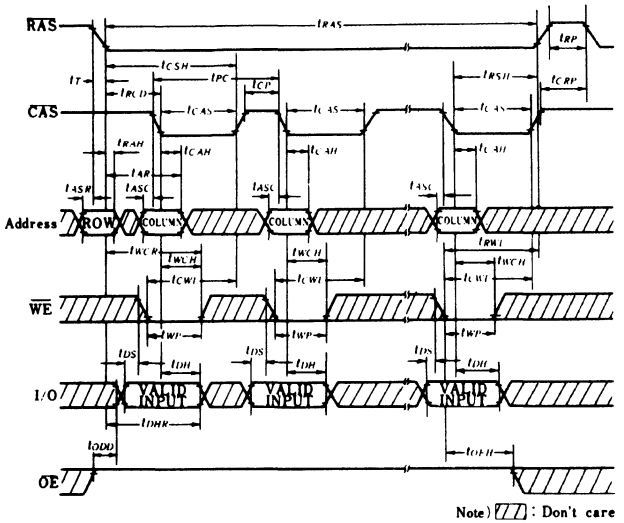
Notes) 1. Dotted-line Means Read Cycle. 2. ▨ : Don't care

- **PAGE MODE READ CYCLE**



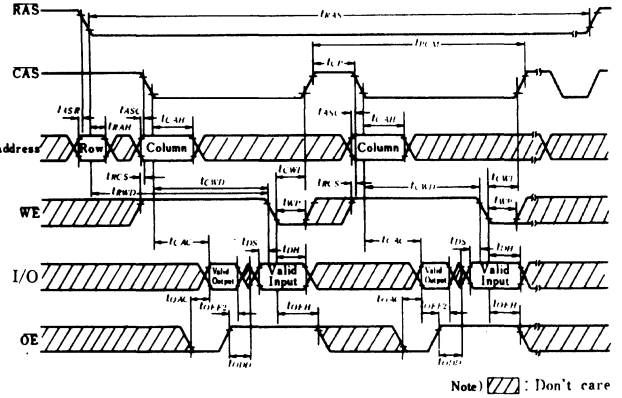
Note) ▨ : Don't care

- **PAGE MODE WRITE CYCLE**



Note) ▨ : Don't care

- **PAGE MODE READ MODIFY WRITE CYCLE**



Note) ▨ : Don't care

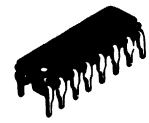
HM50256 Series

262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

- Industry Standard 16-Pin DIP, 18-Pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles · · · (4ms)
- 3 variations of refresh · · · $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh

HM50256P Series



(DP-16B)

HM50256CP Series

(CP-18)

HM50256ZP Series

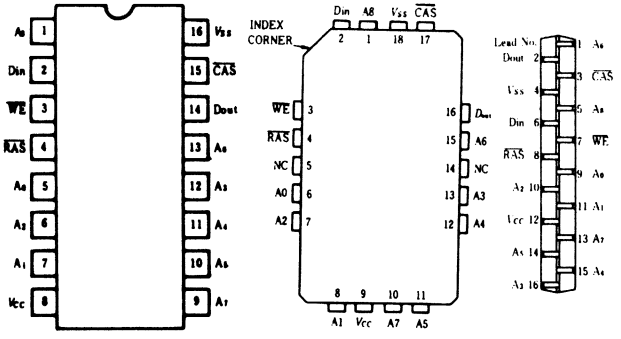
(ZP-16)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM50256P-12 HM50256P-15 HM50256P-20	120ns 150ns 200ns	300 mil 16 pin Plastic DIP
HM50256ZP-12 HM50256ZP-15 HM50256ZP-20	120ns 150ns 200ns	16 pin Plastic ZIP
HM50256CP-12 HM50256CP-15 HM50256CP-20	120ns 150ns 200ns	18 pin PLCC

■ PIN ARRANGEMENT

● HM50256P Series ● HM50256CP Series ● HM50256ZP Series

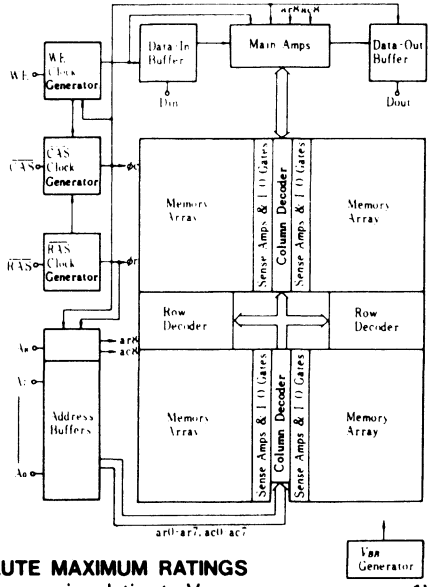


(Top View) (Top View) (Bottom View)

■ PIN DESCRIPTION

A_0~A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0~A_7	Refresh Address Inputs

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . −55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current($\overline{RAS}$, $\overline{CAS}$ =Cycling : t_{RC} =min)	I_{CC1}	—	83	—	70	—	55	mA	1
Standby Current($\overline{RAS}$=V_{IH}, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current($\overline{RAS}$ only Refresh, t_{RC}=min)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current($\overline{RAS}$=V_{IH}, Dout =Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current($\overline{CAS}$ before $\overline{RAS}$ Refresh, t_{RC}=min)	I_{CC6}	—	69	—	58	—	45	mA	
Page Mode Supply Current($\overline{RAS}$=V_{IL}, $\overline{CAS}$ =Cycling, t_{PC}=min)	I_{CC7}	—	57	—	48	—	37	mA	
Input leakage(0<V_{in}<7V)	I_{LI}	−10	10	−10	10	−10	10	μA	
Output leakage(0<V_{out}<7V, Dout=Disable)	I_{LO}	−10	10	−10	10	−10	10	μA	
Output levels High(I_{out}=−5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low(I_{out}=4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7		1, 2
Output Capacitance	Data-out	C_O		7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable Dout.

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V) [1], [10], [11]

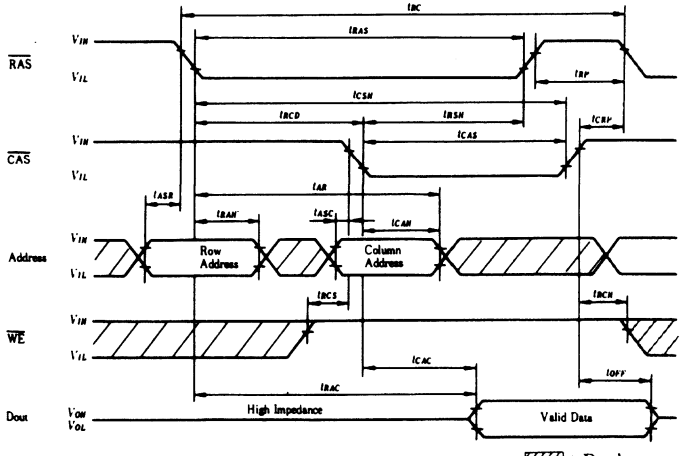
Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	220		260		330		ns	
Read-Write Cycle Time	t_{RWC}	265		310		390		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
Access Time from $\overline{RAS}$	t_{RAC}		120		150		200	ns	2, 3
Access Time from $\overline{CAS}$	t_{CAC}		60		75		100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}		30		40		50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{RAS}$ Precharge Time	t_{RP}	90		100		120		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	60		75		100		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	120		150		200		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		10		ns	
Row Address Set-up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	15		15		20		ns	
Column Address Set-up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	20		25		30		ns	
Column Address Hold Time referenced to $\overline{RAS}$	t_{AR}	80		100		130		ns	
Read Command Set-up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	
Write Command Set-up Time	t_{WCS}	0		0		0		ns	8
Write Command Hold Time	t_{WCH}	40		45		55		ns	
Write Command Hold Time referenced to $\overline{RAS}$	t_{WCR}	100		120		155		ns	
Write Command Pulse Width	t_{WP}	40		45		55		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	40		45		55		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	40		45		55		ns	
Data-in Set-up Time	t_{DS}	0		0		0		ns	9
Data-in Hold Time	t_{DH}	40		45		55		ns	8, 9
Data-in Hold Time referenced to $\overline{RAS}$	t_{DHR}	100		120		155		ns	
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	120		150		200		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	60		75		100		ns	8
Page Mode Read or Write Cycle	t_{PC}	120		145		190		ns	
Page Mode Read Modify Write Cycle	t_{PCM}	165		195		250		ns	
$\overline{CAS}$ Precharge Time, Page Cycle	t_{CP}	50		60		80		ns	
Read Command Hold Time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	
Refresh Period	t_{REF}		4		4		4	ms	
$\overline{CAS}$ Set-up Time	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	120		150		200		ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	t_{RPC}	0		0		0		ns	

Notes

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
8. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters.
   They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
11. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refesh cycles are required before using internal refresh counter.

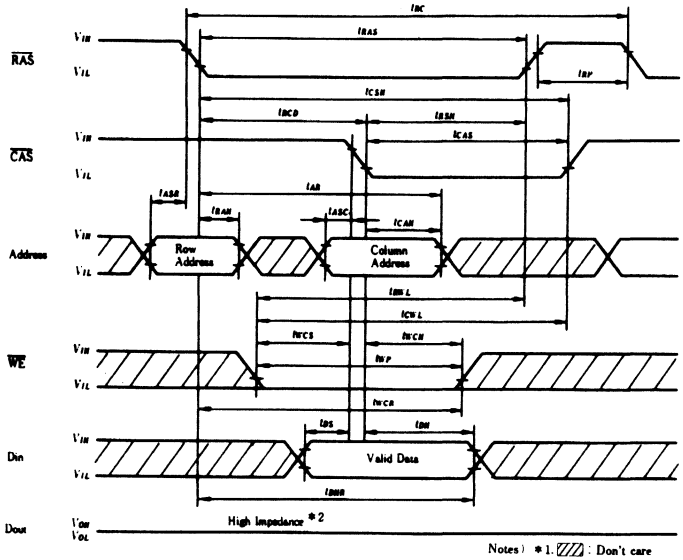
■ TIMING WAVEFORMS

● READ CYCLE



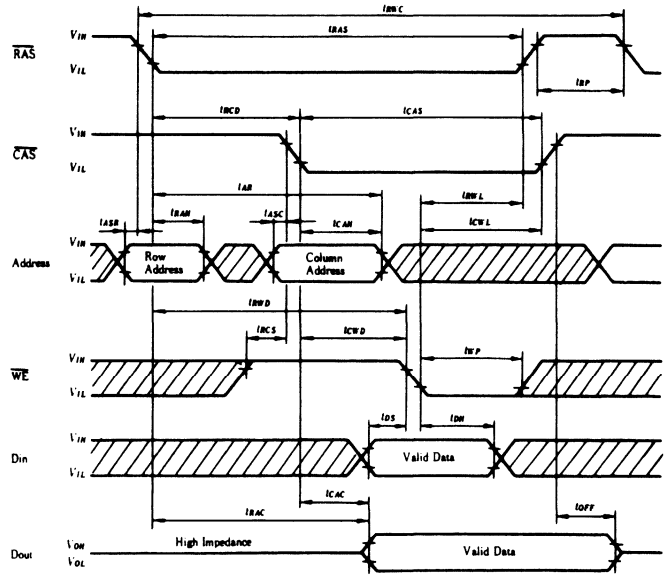
Note) ▨ : Don't care

● WRITE CYCLE



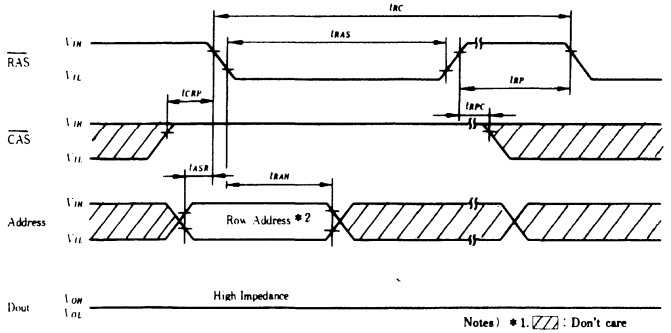
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$(min)

● READ MODIFY WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geq t_{RWD}$(min)
$t_{CWD} \geq t_{CWD}$(min)

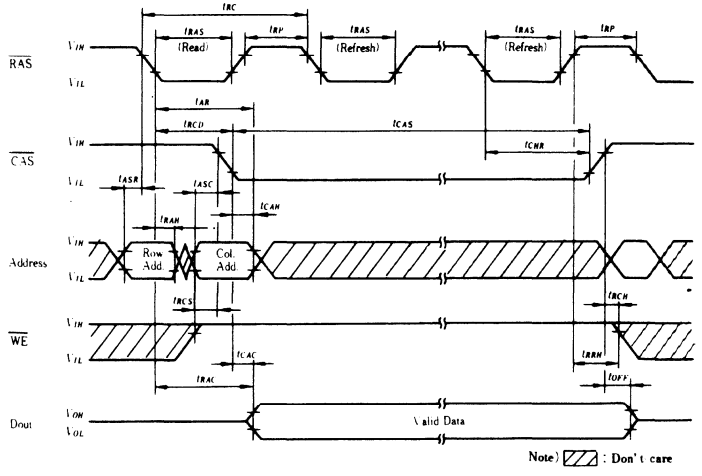
● $\overline{RAS}$ ONLY REFRESH CYCLE



Notes) *1. ▨ : Don't care

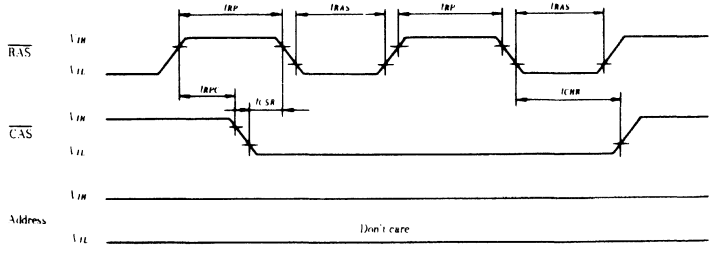
*2. Refresh Address A0-A7(AX0-AX7)

● HIDDEN REFRESH CYCLE

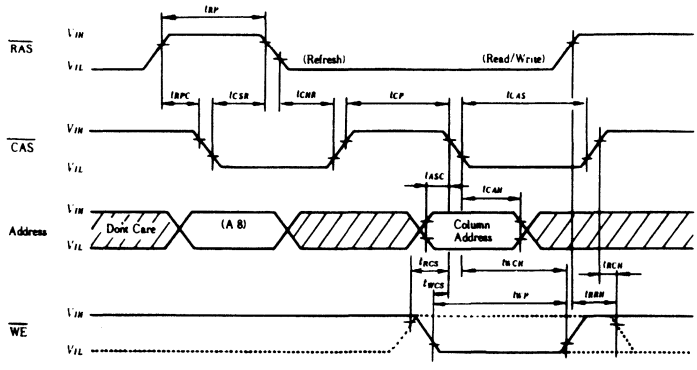


Note) ▨ : Don't care

● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

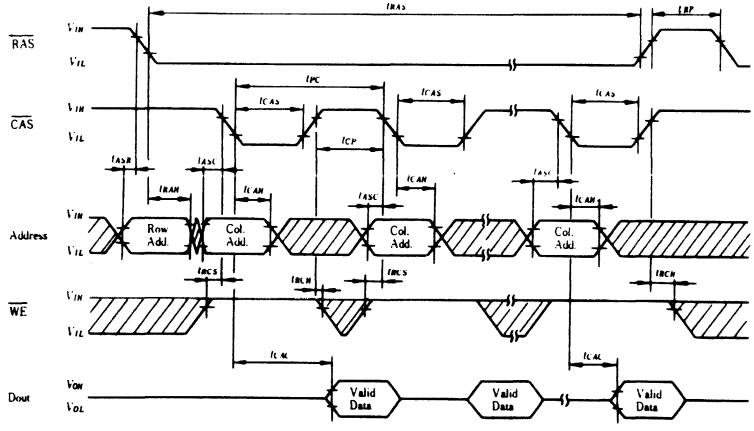


●COUNTER TEST



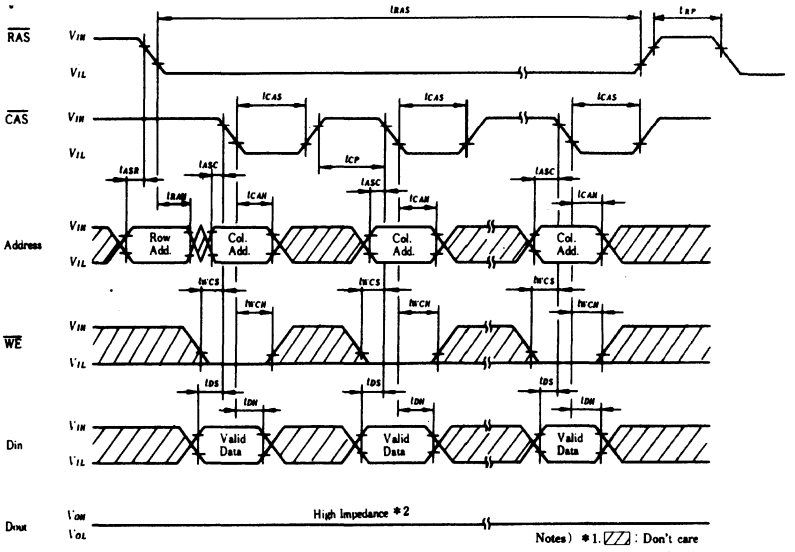
Notes) *1. ▨ : Don't care
*2. Dotted Line Means Read Cycle.

●PAGE MODE READ CYCLE



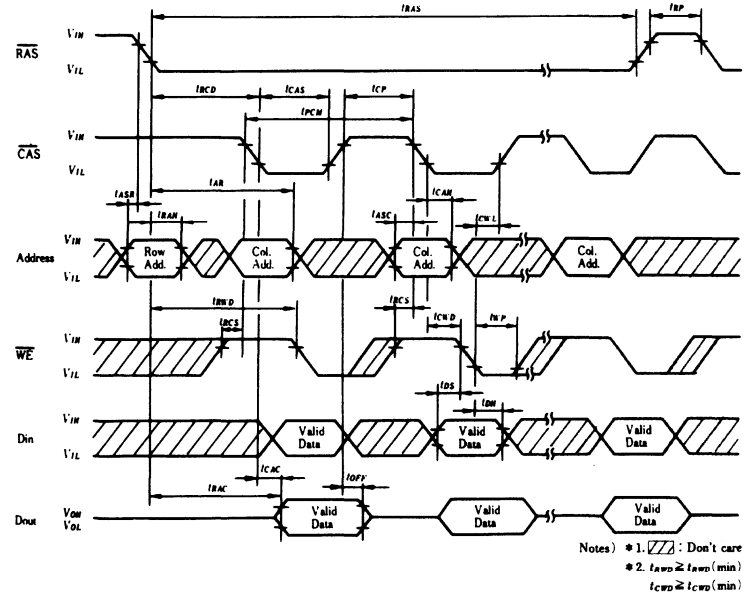
Note) ▨ : Don't care

● PAGE MODE WRITE CYCLE



Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

● PAGE MODE READ MODIFY WRITE CYCLE

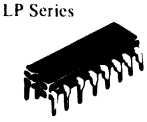


Notes) *1. ▨ : Don't care
*2. $t_{AWD} \geq t_{AWD}$ (min)
$t_{CWD} \geq t_{CWD}$ (min)

HM51256 Series

262144-word × 1-bit CMOS Dynamic Random Access Memory

HM51256P Series
HM51256LP Series



(DP-16B)

HM51256CP Series
HM51256LCP Series

(CP-18)

HM51256ZP Series
HM51256LZP Series

(ZP-16)

■FEATURE

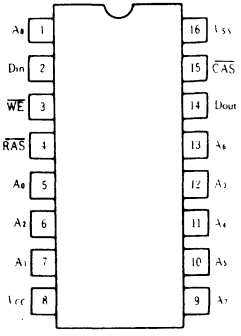
- 262, 144 word x 1 bit DRAM
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage: 5V ± 10%
- Access time
  - Row access time: 85/100/120/150ns
  - Address access time: 40/45/55/70ns
- Cycle time
  - Random read/write cycle time: 155/180/210/250ns
  - High speed page mode cycle time: 50/55/65/80ns
- Lower power
  - Standby: 11mW (TTL Level)
    1.1mW (CMOS Level: L-version)
  - Active: 385/330/275/220mW
- Refresh: 256 cycles/4ms
  256 cycles/32ms (L-version)
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast $\overline{CAS}$ output control

■ ORDERING INFORMATION

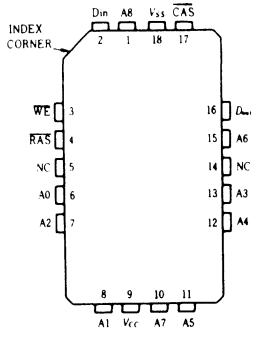
Type No.	Access Time	Package
HM51256P-8	85ns	300 mil 16 pin Plastic DIP
HM51256P-10	100ns	
HM51256P-12	120ns	
HM51256P-15	150ns	
HM51256CP-8	85ns	18 Pin PLCC
HM51256CP-10	100ns	
HM51256CP-12	120ns	
HM51256CP-15	150ns	
HM51256LP-8	85ns	300 mil 16 pin Plastic DIP
HM51256LP-10	100ns	
HM51256LP-12	120ns	
HM51256LP-15	150ns	
HM51256LCP-8	85ns	18 pin PLCC
HM51256LCP-10	100ns	
HM51256LCP-12	120ns	
HM51256LCP-15	150ns	
HM51256ZP-8	85ns	16 pin Plastic ZIP
HM51256ZP-10	100ns	
HM51256ZP-12	120ns	
HM51256ZP-15	150ns	
HM51256LZP-8	85ns	
HM51256LZP-10	100ns	
HM51256LZP-12	120ns	
HM51256LZP-15	150ns	

■ PIN ARRANGEMENT

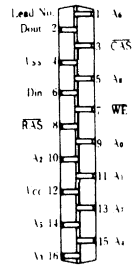
- HM51256P Series
  HM51256LP Series
- HM51256CP Series
  HM51256LCP Series
- HM51256ZP Series
  HM51256LZP Series



(Top View)



(Top View)



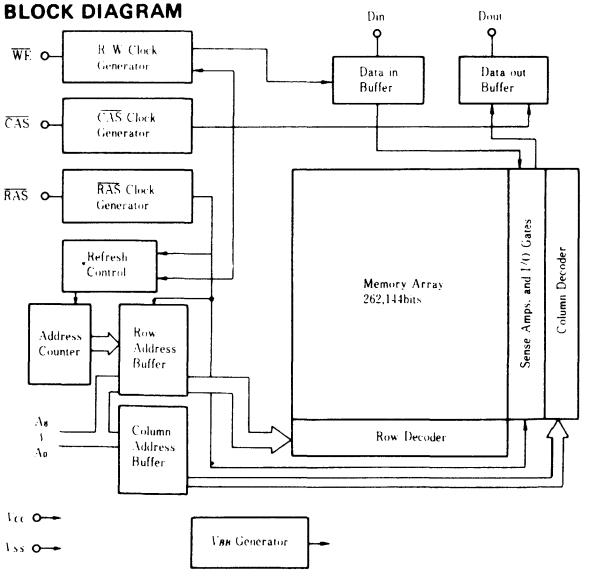
(Bottom View)

A_0-A_8	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A_0-A_7	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . -1V to +7V
Operating temperature, Ta (Ambient) . . . . . 0°C to +70°C
Storage temperature . . . . . -55°C to +125°C
Short circuit output current 50mA
Power dissipation 1W

■ BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS ($Ta=0$ to $+70$°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Operating Current (RAS, CAS Cycling: t_{RC} = min)	I_{CC1}	–	70	–	60	–	50	–	40	mA	1
Standby Current (RAS = V_{IH}, Dout = High Impedance)	I_{CC2}	–	2	–	2	–	2	–	2	mA	
Refresh Current (RAS only Refresh, t_{RC} = min)	I_{CC3}	–	70	–	60	–	50	–	40	mA	
Standby Current (RAS = V_{IH}, Dout Enable)	I_{CC4}	–	6	–	6	–	6	–	6	mA	1
Refresh Current (CAS before RAS Refresh, t_{RC} = min)	I_{CC5}	–	60	–	55	–	45	–	35	mA	
High Speed Page Mode Supply Current (RAS = V_{IL}, CAS Cycling, t_{PC} = min)	I_{CC6}	–	70	–	60	–	50	–	40	mA	1
Standby Current (RAS, CAS = V_{CC} – 0.2V)	I_{CC7}	–	200	–	200	–	200	–	200	μA	2
Input leakage (0≤ V_{in} ≤7V)	I_{LI}	–10	10	–10	10	–10	10	–10	10	μA	
Output leakage (0≤ V_{out} ≤7V, Dout = Disable)	I_{LO}	–10	10	–10	10	–10	10	–10	10	μA	
Output levels High (I_{out} = –5mA)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low (I_{out} = 4.2mA)	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	V	

Notes: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
2. This specification is guaranteed only for L version.

■CAPACITANCE (V_{CC}=5V±10%, Ta=25°C)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1
Output Capacitance	Data out	C_O	–	7		1, 2

Notes) 1 Capacitance measured with Boonton Meter or effective capacitance measuring method.
2 CAS = V_{IH} to disable Dout

■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Ta=0 to +70°C, V_{CC}=5V±10%, V_{SS}=0V)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
RAS Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
RAS Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
CAS Pulse Width	t_{CAS}	25	–	25	–	30	–	35	–	ns	
Column Address Set-up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to RAS	t_{AR}	60	–	75	–	90	–	110	–	ns	
RAS to CAS Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
RAS to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
RAS Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
CAS Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
CAS to RAS Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms	
		–	32	–	32	–	32	–	32	ms	21

● Read Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Access Time from RAS	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from CAS	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to CAS	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to RAS	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to RAS Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
Output Buffer Turn off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6

● Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Write Command Set-up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

● Read-Modify-Write Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10

● Refresh Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
$\overline{CAS}$ Set-up Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Prechange to $\overline{CAS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

● High Speed Page Mode Cycle

Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time	t_{PC}	50	–	55	–	65	–	80	–	ns	18, 20
High Speed Page Mode $\overline{RAS}$ Pulse Width	t_{RAPC}	55	75000	65	75000	75	75000	95	75000	ns	19
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	10	–	15	–	20	–	20	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	
Access Time from Column Precharge Time	t_{CAP}	–	45	–	50	–	60	–	75	ns	20

● High Speed Page Mode Read-Modify-Write Cycle

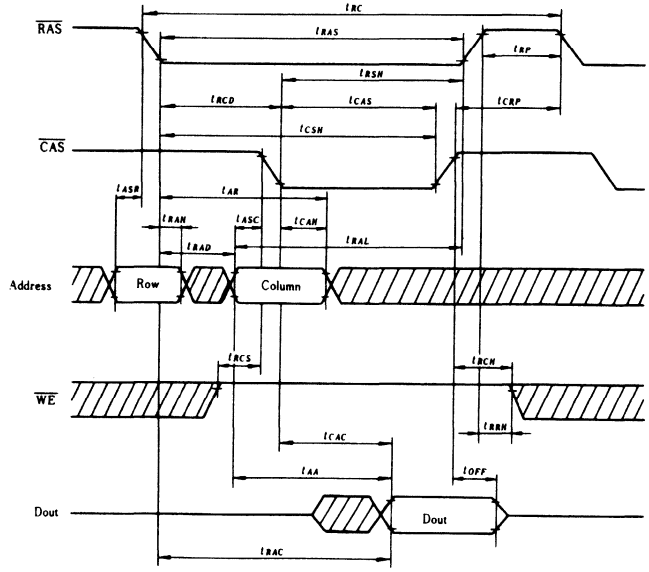
Parameter	Symbol	HM51256-8		HM51256-10		HM51256-12		HM51256-15		Unit	Notes
		min	max	min	max	min	max	min	max		
High Speed Page Mode Cycle Time on Read-Write	t_{RWPC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15

Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a Reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWPC} (min) = t_{AWD} (min) + t_{WAD} (max) + t_T.
13. Assumes that $t_{WAD} \leqq t_{WAD}$ (max). If t_{WAD} is greater than the maximum recommended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$ (max).
15. Operation with the t_{WAD} (max) limit insures that t_{PWA} (max) can be met, t_{WAD} (max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. An intial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
17. At least, 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required before using internal refresh counter.
18. Assumes that $t_{ASC} = t_{CP} - 5$ ns.
19. t_{RAPC} is determined by $\overline{RAS}$ pulse width in High Speed Page mode cycle.
20. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
21. This specification is guaranteed only for L-version.

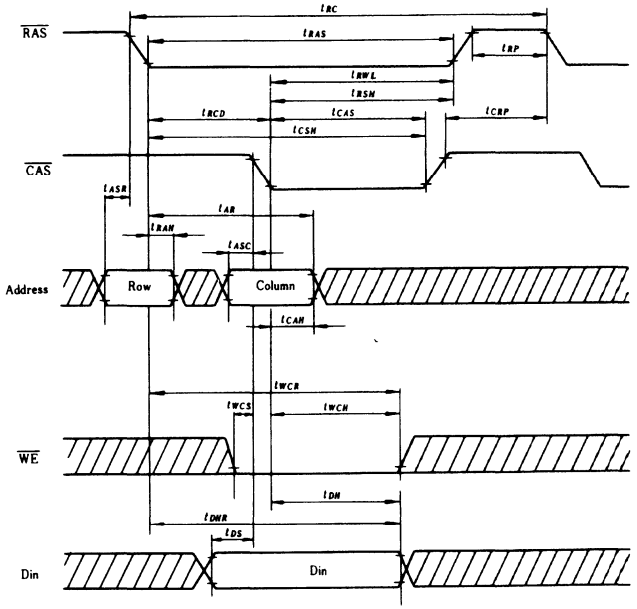
■TIMING WAVEFORMS

●Read Cycle



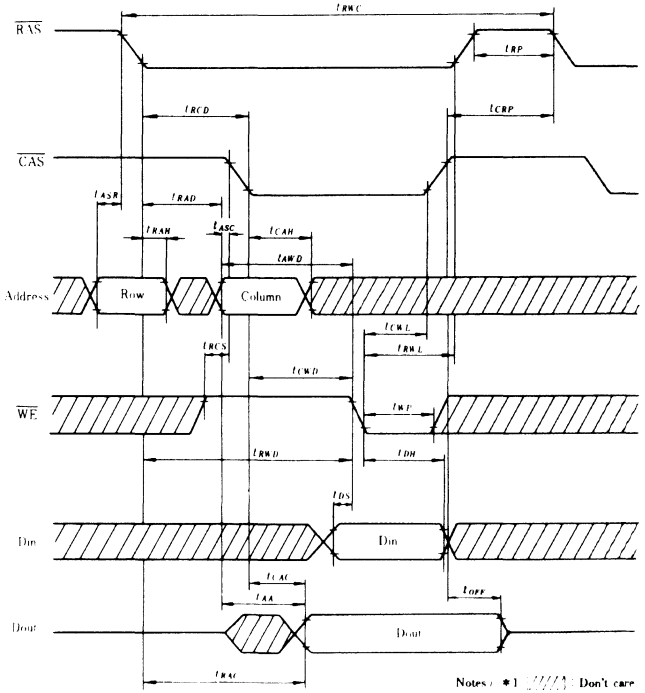
Note) ▨ : Don't care

● Write Cycle



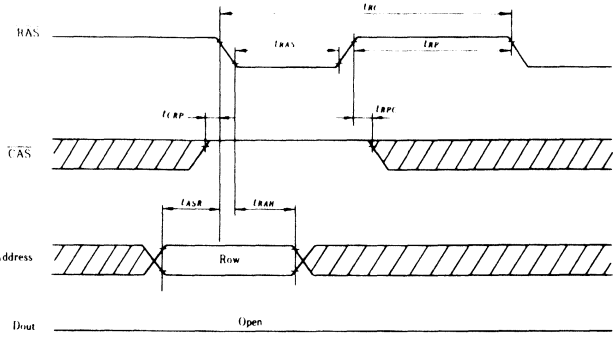
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

● Read Modify Write Cycle



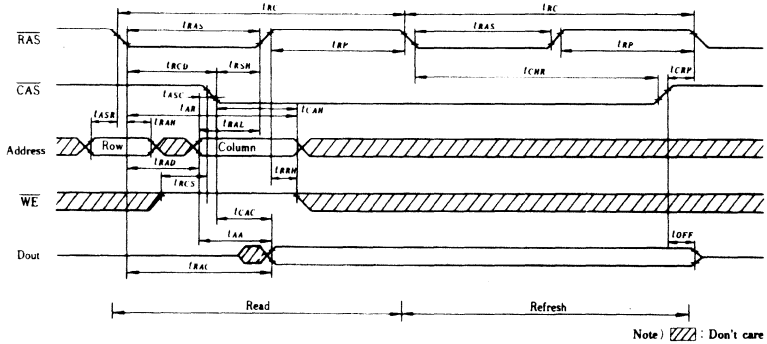
Notes) *1 ▨ : Don't care
*2 $t_{RWD} \geq t_{RWD}$ (min)
$t_{CWD} \geq t_{CWD}$ (min)
$t_{AWD} \geq t_{AWD}$ (min)

● RAS Only Refresh Cycle



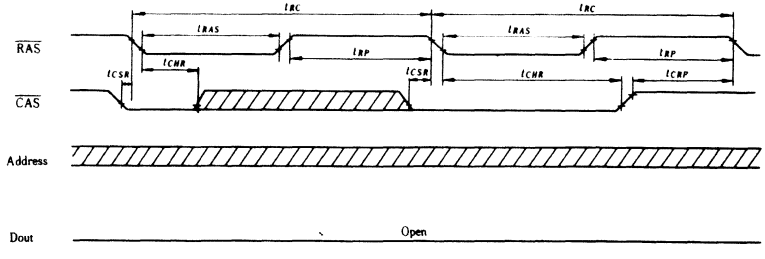
Note) ▨ : Don't care

● Hidden Refresh Cycle



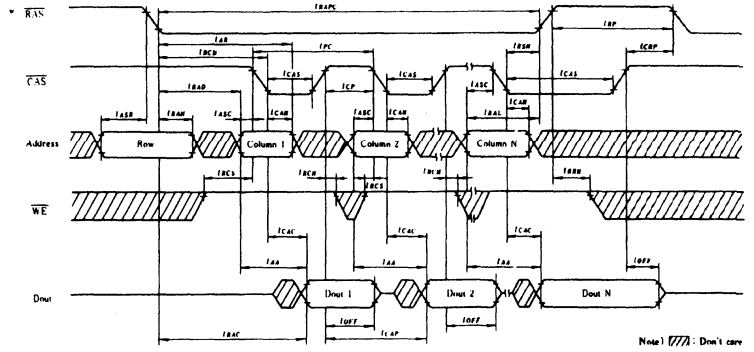
Note) ▨ : Don't care

● $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

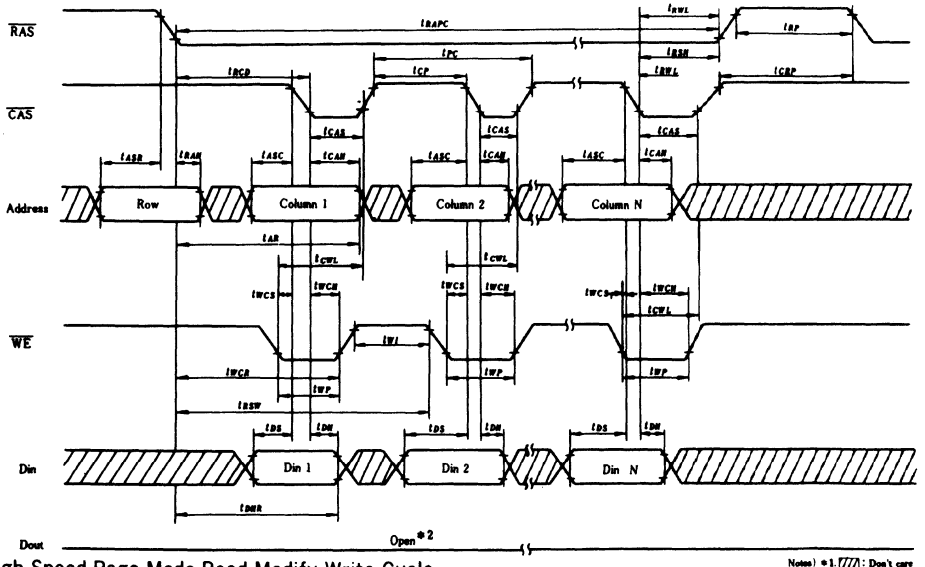


Note) ▨ : Don't care

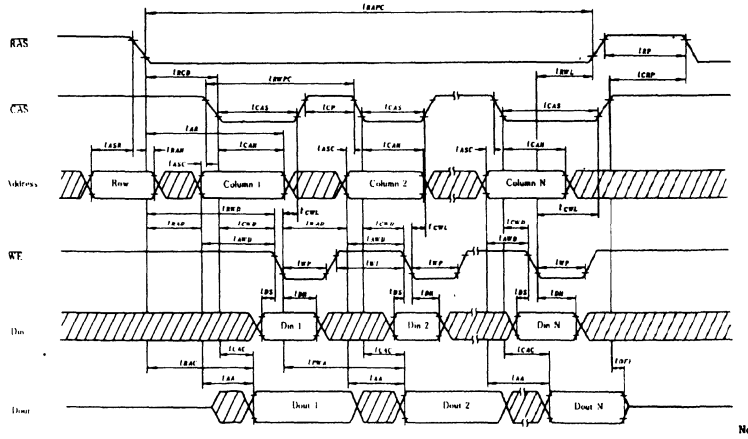
● High Speed Page Mode Read Cycle



● High Speed Page Mode Write Cycle



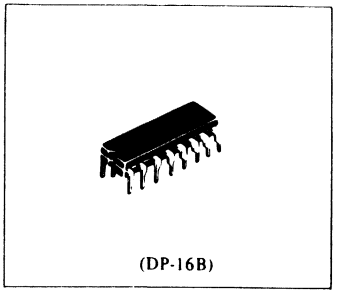
● High Speed Page Mode Read Modify Write Cycle



HM51258 Series

262144-word x 1-bit Static Column CMOS Dynamic RAM

The HM51258 is the 262,144 word by 1 bit static column dynamic random access memory utilizing the Hitachi 2μm CMOS process.
This device has static column circuit and it is good for high performance main storage or for page access applications.
While the row circuitry is still dynamic, and it controls the power consumed in the static circuitry. It realizes very low power dissipation.
Multiplexed address and the 16 pin pinout are compatible with the fully dynamic 256K DRAM HM50256.



(DP-16B)

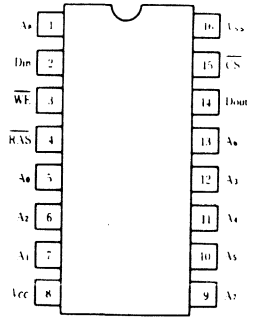
■ FEATURES

- 262,144 word x 1 bit SCRAM
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage 5V ± 10%
- Access time
  Row access time: 85/100/120/150ns
  Address access time: 40/45/55/70ns
- Cycle time
  Random Read&Write cycle time: 155/180/210/250ns
  Static Column cycle time: 45/50/60/75ns
- Lower power
  Standby: 11mW
  Active: 385/330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: $\overline{RAS}$ only refresh, $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh
- Static column mode capability
- Edge triggered write capability
- Fast $\overline{CS}$ output control

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM51258P-8	85ns	300 mil 16 pin Plastic DIP
HM51258P-10	100ns	
HM51258P-12	120ns	
HM51258P-15	150ns	

■PIN ARRANGEMENT

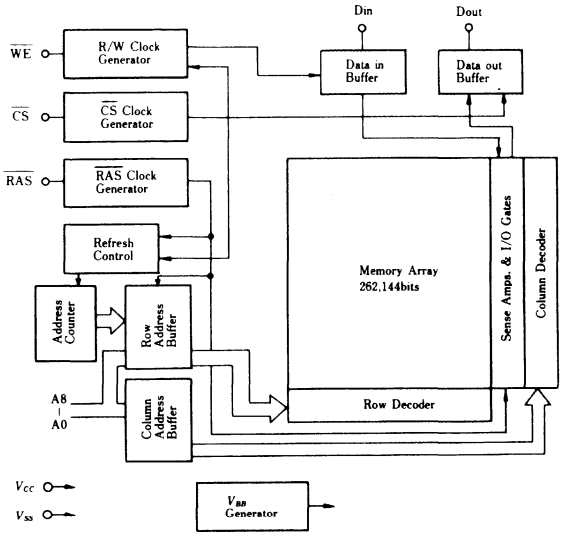


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A8	Address inputs
$\overline{CS}$	Chip select
Din	Data in
Dout	Data out
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Read/Write input
Vcc	Power (+5V)
Vss	Ground
A0–A7	Refresh address inputs

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply Voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	−1.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

■ DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=0 to +70°C)

Parameter	Sybmol	Test conditions	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Note
			min	max	min	max	min	max	min	max		
Operating current	I_{CC1}	RAS, CS Cycling; t_{RC}=min.		70		60		50		40	mA	1
Standby current	I_{CC2}	RAS=V_{IH}, Dout=High Impedance		2		2		2		2	mA	
Refresh current	I_{CC3}	RAS only Refresh, t_{RC}=min		70		60		50		40	mA	
Standby current	I_{CC4}	RAS=V_{IH}, Dout Enable		6		6		6		6	mA	1
Refresh current	I_{CC5}	CS before RAS Refresh, t_{RC}=min		60		55		45		35	mA	
Operating current	I_{CC6}	Static Column Mode, t_{RSC}, t_{WSC}=min		70		60		50		40	mA	1
Input leakage	I_{LI}	V_{in}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage	I_{LO}	V_{out}=0 to 7V	−10	10	−10	10	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{out}=−5mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{out}=4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.

■ CAPACITANCE (V_{CC}=5V±10%, T_a=25°C)

Parameter		Symbol	typ	max	Unit	Note
Input capacitance	Address, Data-In	C_{I1}	–	5	pF	1
	Clock	C_{I2}	–	7	pF	1
Output capacitance	Data-Out	C_O	–	7	pF	1, 2

Note) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (T_a=0 to +70°C, V_{CC}=5V±10%, V_{SS} = 0V)

• Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	–	180	–	210	–	250	–	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	60	–	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
$\overline{CS}$ Pulse Width	t_{CS}	25	–	25	–	30	–	35	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
$\overline{RAS}$ Hold Time	t_{RSH}	20	–	25	–	30	–	35	–	ns	
$\overline{CS}$ Hold Time	t_{CSH}	85	–	100	–	120	–	150	–	ns	
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10	–	10	–	10	–	10	–	ns	
Row Address Set-Up Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	10	–	15	–	15	–	20	–	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	–	4	–	4		4	–	4	ms	
• Read Cycle											
Access Time from $\overline{RAS}$	t_{RAC}	–	85	–	100	–	120	–	150	ns	2, 3
Access Time from $\overline{CS}$	t_{CAC}	–	25	–	25	–	30	–	35	ns	3, 4
Access Time from Address	t_{AA}	–	40	–	45	–	55	–	70	ns	3,5,14
Column Address Hold Time to $\overline{RAS}$ on Read	t_{AR}	85	–	100	–	120	–	150	–	ns	
Read Command Set-Up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	40	–	45	–	55	–	70	–	ns	
$\overline{RAS}$ to Column Address Hold Time	t_{AH}	10	–	15	–	15	–	20	–	ns	16
Output Hold Time from Address	t_{OH}	5	–	5	–	5	–	5	–	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6
• Write Cycle											
Column Address Set-Up Time	t_{ASC}	0	–	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	15	–	20	–	25	–	30	–	ns	
Column Address Hold Time to $\overline{RAS}$ on Write	t_{AWR}	60	–	75	–	90	–	110	–	ns	
Write Command Set-Up Time	t_{WCS}	0	–	0	–	0	–	0	–	ns	10
Write Command Hold Time	t_{WCH}	20	–	25	–	30	–	35	–	ns	
Write Command Hold Time to $\overline{RAS}$	t_{WCR}	65	–	80	–	95	–	115	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	30	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20	–	25	–	30	–	35	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{CWL}	20	–	25	–	30	–	35	–	ns	
Data-in Set-up Time	t_{DS}	0	–	0	–	0	–	0	–	ns	11
Data-in Hold Time	t_{DH}	15	–	20	–	25	–	30	–	ns	10, 11
Data-in Hold Time to $\overline{RAS}$	t_{DHR}	60	–	75	–	90	–	110	–	ns	

(to be continued)

- **Read-Modify-Write Cycle**

Parameter	Symbol	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
$\overline{CS}$ to $\overline{WE}$ Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10
Output Hold Time from $\overline{WE}$	t_{OHW}	25	–	25	–	25	–	25	–	ns	

- **Refresh Cycle**

$\overline{CS}$ Set-up Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

- **SC Mode Cycle**

SC Mode Cycle Time on Read	t_{RSC}	45	–	50	–	60	–	75	–	ns	
SC Mode Cycle Time on Write	t_{WSC}	45	–	50	–	60	–	75	–	ns	
$\overline{RAS}$ to Second $\overline{WE}$ Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
SC Mode $\overline{RAS}$ Pulse Width	t_{RASC}	55	75000	65	75000	75	75000	95	75000	ns	
$\overline{CS}$ Precharge Time	t_{CP}	10	–	10	–	15	–	15	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	

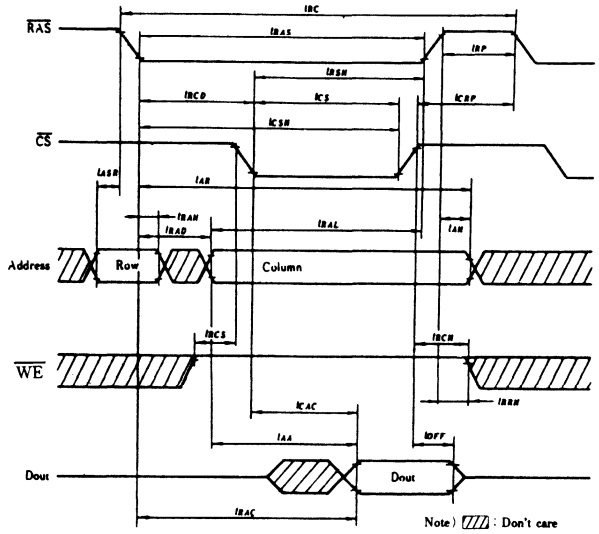
- **SC Mode Read-Modify-Write and Mixed Cycle**

SC Mode Cycle Time on Read-Write	t_{RWSC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous $\overline{WE}$	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous $\overline{WE}$ to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15
Column Address Hold Time to Previous $\overline{WE}$	t_{PWH}	80	–	90	–	110	–	140	–	ns	

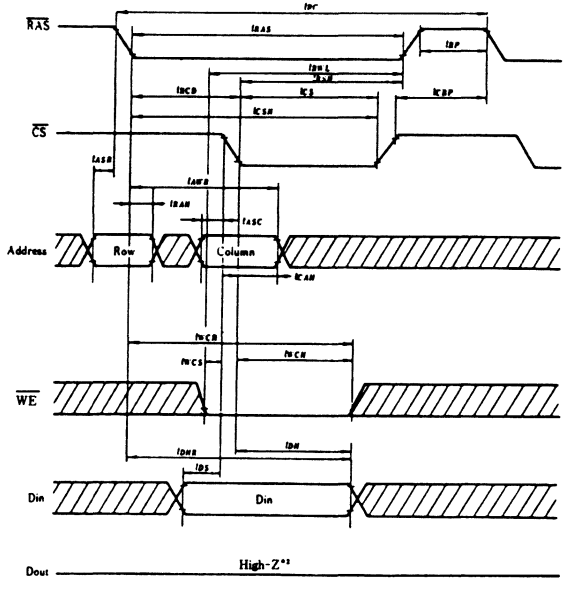
Notes:
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \leqq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $tRAD \leqq tRAD$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \geqq t_{RAD}$(max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$(min), $t_{CWD} \geqq t_{CWD}$(min) and $t_{AWD} \geqq t_{AWD}$(min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RWSC}(min) = t_{AWD}(min) + t_{WAD}(max) + t_T
13. Assumes that $tWAD \leqq tWAD$(max). If $tWAD$ is greater than the maximum recommended value shown in this table, t_{PWA} exceeds the value shown.
14. Assumes that $t_{WAD} \geqq t_{WAD}$(max).
15. Operation with the t_{WAD}(max) limit insures that t_{PWA}(max) can be met, t_{WAD}(max) is specified as a reference point only, if t_{WAD} is greater than the specified t_{WAD}(max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is defined as the time at which the column address hold.
17. An initial pause of 100μs is required after power-up then execute at least 8 initialization cycles.
18. At least, 8 $\overline{CS}$ before $\overline{RAS}$ refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

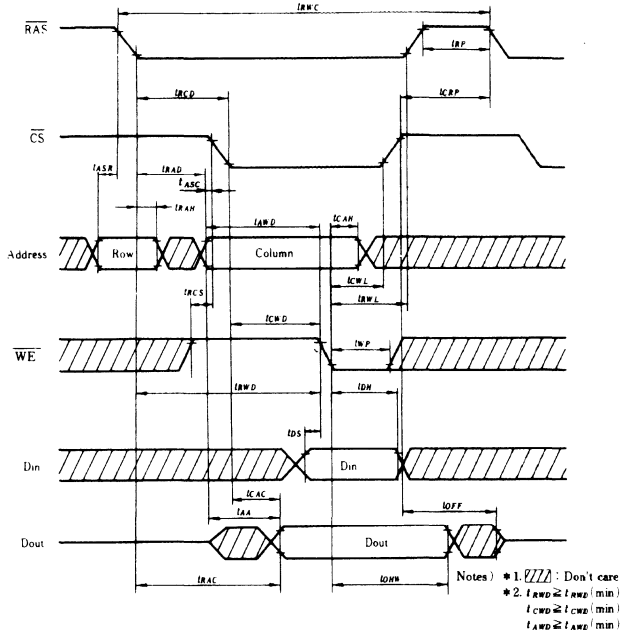
● Read Cycle



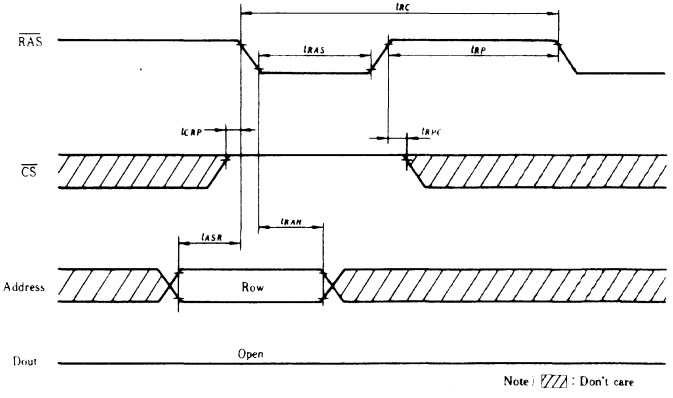
● Write Cycle



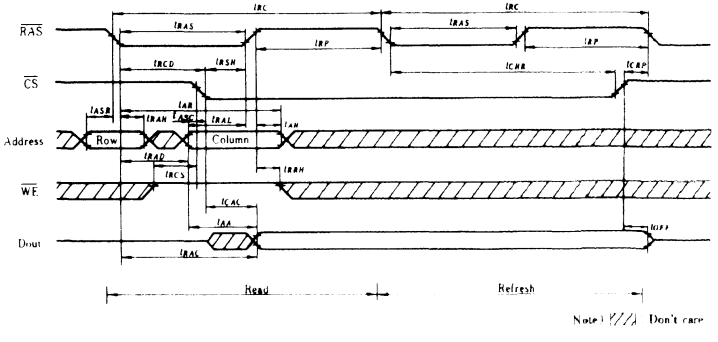
- **Read-Modify-Write Cycle**



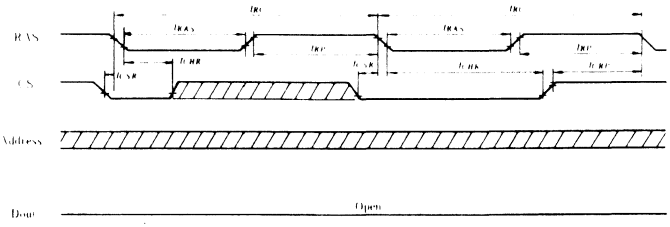
- **$\overline{RAS}$ Only Refresh Cycle**



- **Hidden Refresh Cycle**

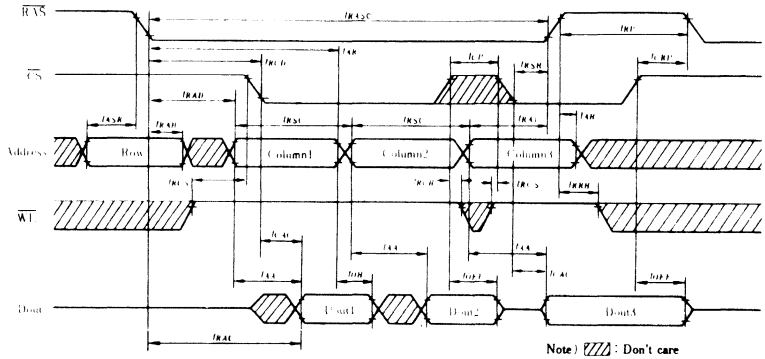


- **$\overline{CS}$ before $\overline{RAS}$ Refresh Cycle**



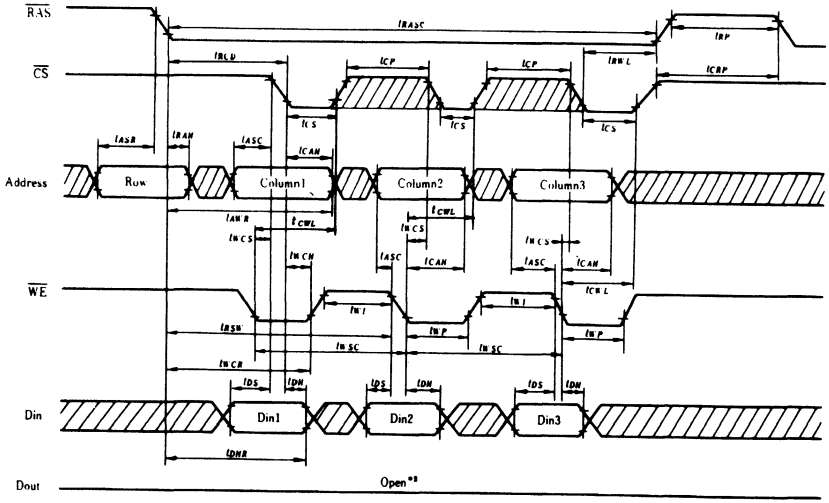
Note) ▨: Don't care

- **Static Column Mode Read Cycle**



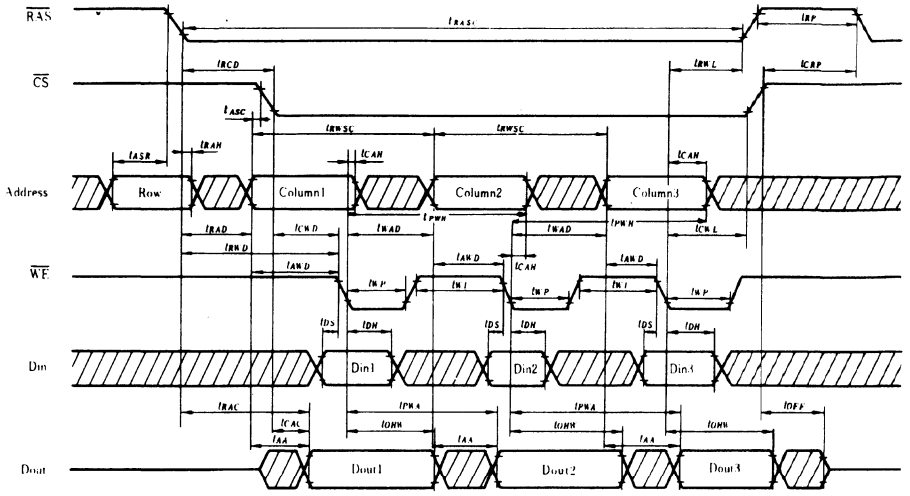
Note) ▨: Don't care

- **Static Column Mode Write Cycle**



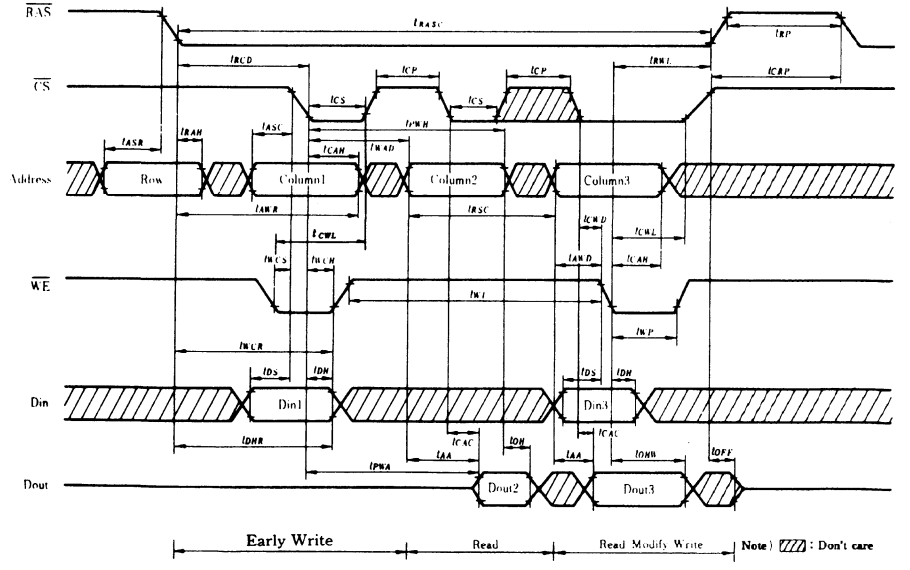
Notes) *1. ▨: Don't care
*2. $t_{WCS} \geqq t_{WCS}$ (min)

- **Static Column Mode Read-Modify-Write Cycle**

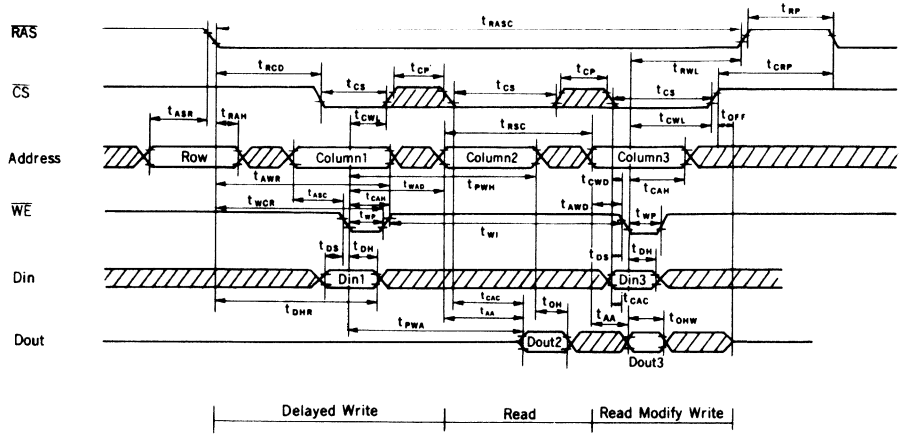


Notes) *1. ▨ : Don't care
*2. $t_{RWD} \geq t_{RWD}(\min)$
$t_{CWD} \geq t_{CWD}(\min)$
$t_{AWD} \geq t_{AWD}(\min)$

- **Static Column Mode Mixed Cycle-1**



- **Static Column Mode Mixed Cycle-2**



Note) ▨ : Don't care.

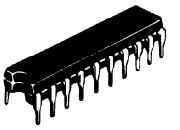
HM514256A Series
HM514256AL Series

262144-Word × 4-Bit CMOS Dynamic RAM

The Hitachi HM514256A/AL is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514256A/AL has realized higher density, higher performance and various functions by employing 1.3 µm CMOS technology and some new CMOS circuit design technologies. The HM514256A/AL offers Fast Page Mode as a high speed access mode.

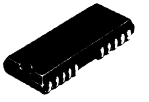
Multiplexed address input permits the HM514256A/AL to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM514256A/ALP Series



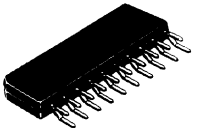
(DP-20NA)

HM514256A/ALJP Series



(CP-20D)

HM514256A/ALZP Series

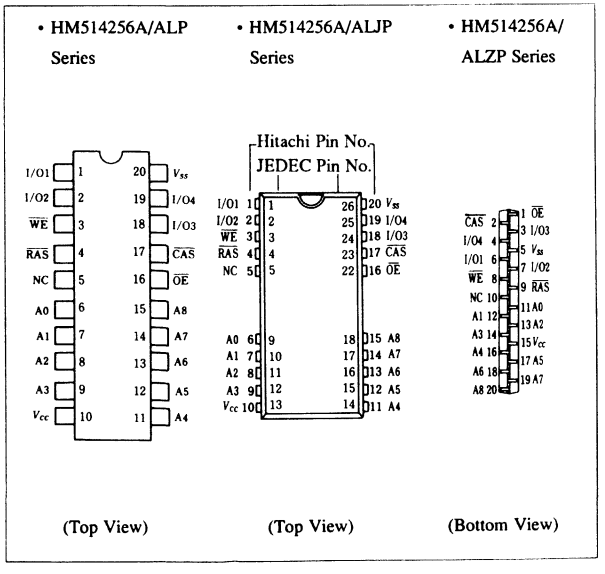


(ZP-20)

Features

- Single 5 V (±10%)
- High speed: Access Time 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power: Standby 11 mW (max), 1.7 mW (max)(L version)
  Active 495 mW/440 mW/363 mW/302.5 mW/258.5 mW (max)
- Fast page mode capability
- 512 refresh cycles: (8 ms), (64 ms) (L version)
- 2 variations of refresh: $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

Pin Arrangement



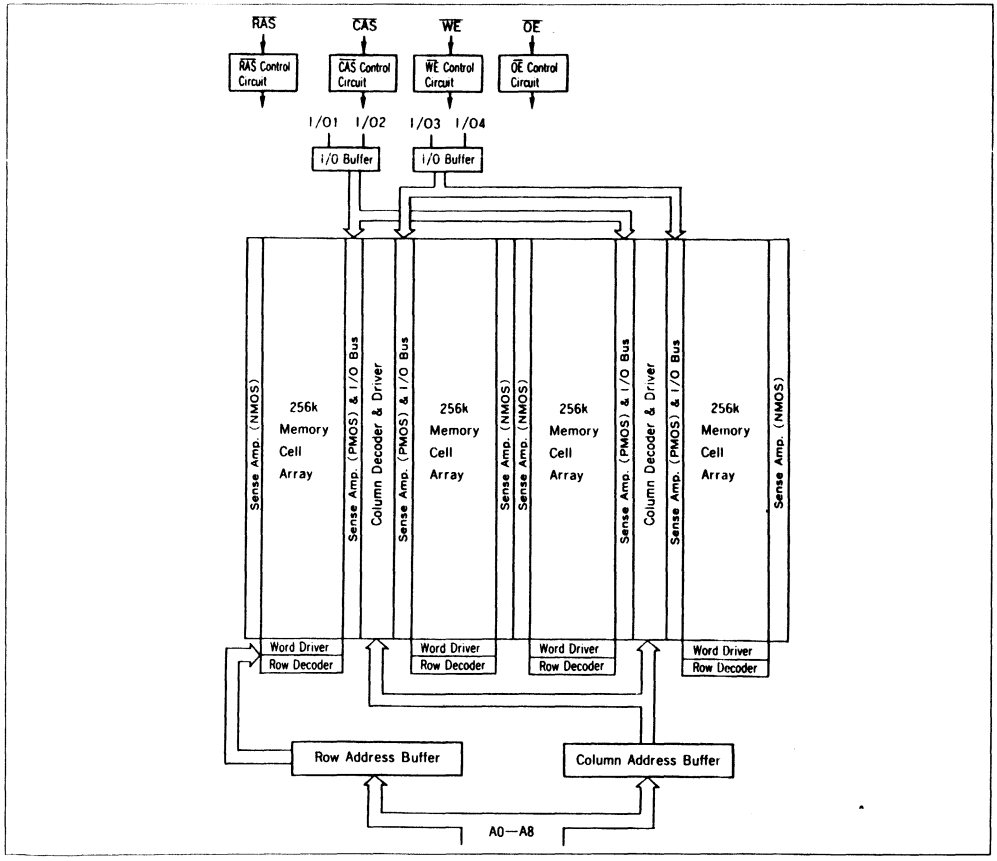
Pin Description

Pin Name	Function
A0–A8	Address input
A0–A8	Refresh address input
I/O1–I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power supply (+5 V)
Vss	Ground

Ordering Information

Type No.	Access Time	Package	Type No.	Access Time	Package
HM514256AP-6	60 ns		HM514256ALP-6	60 ns	
HM514256AP-7	70 ns	300-mil 20-pin	HM514256ALP-7	70 ns	300-mil 20-pin
HM514256AP-8	80 ns	plastic DIP	HM514256ALP-8	80 ns	plastic DIP
HM514256AP-10	100 ns	(DP-20NA)	HM514256ALP-10	100 ns	(DP-20NA)
HM514256AP-12	120 ns		HM514256ALP-12	120 ns	
HM514256AJP-6	60 ns		HM514256ALJP-6	60 ns	
HM514256AJP-7	70 ns	300-mil 20-pin	HM514256ALJP-7	70 ns	300-mil 20-pin
HM514256AJP-8	80 ns	plastic SOJ	HM514256ALJP-8	80 ns	plastic SOJ
HM514256AJP-10	100 ns	(CP-20D)	HM514256ALJP-10	100 ns	(CP-20D)
HM514256AJP-12	120 ns		HM514256ALJP-12	120 ns	
HM514256AZP-6	60 ns		HM514256ALZP-6	60 ns	
HM514256AZP-7	70 ns	400-mil 20-pin	HM514256ALZP-7	70 ns	400-mil 20-pin
HM514256AZP-8	80 ns	plastic ZIP	HM514256ALZP-8	80 ns	plastic ZIP
HM514256AZP-10	100 ns	(ZP-20)	HM514256ALZP-10	100 ns	(ZP-20)
HM514256AZP-12	120 ns		HM514256ALZP-12	120 ns	

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−1.0 to +7.0	V
Supply voltage relative to Vss	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	*1
Input high voltage		V_{IH}	2.4	—	6.5	V	*1
Input low voltage	I/O pin	V_{IL}	−1.0	—	0.8	V	*1
	Others	V_{IL}	−2.0	—	0.8	V	*1

Note: *1. All voltage referenced to Vss.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0 V)

Item	Symbol	HM514256A /AL-6 Min	HM514256A /AL-6 Max	HM514256A /AL-7 Min	HM514256A /AL-7 Max	HM514256 A/AL-8 Min	HM514256 A/AL-8 Max	HM514256 A/AL-10 Min	HM514256 A/AL-10 Max	HM514256 A/AL-12 Min	HM514256 A/AL-12 Max	Unit	Test Conditions	Note
Operating current	I_{CC1}	—	90	—	80	—	66	—	55	—	47	mA	$\overline{RAS}$,$\overline{CAS}$ cycling, t_{RC}=Min	*1,*2
Standby current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	$\overline{RAS}$,$\overline{CAS}$ =V_{IH} Dout =High-Z	TTL interface
		—	1	—	1	—	1	—	1	—	1		$\overline{RAS}$,$\overline{CAS}$ ≥ V_{CC} -0.2V	CMOS interface
		—	300	—	300	—	300	—	300	—	300	µA	Dout =High-Z	CMOS interface L-version
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	66	—	55	—	47	mA	t_{RC} = Min	*2
Battery backup current (only for L-version)	I_{CC4}	—	300	—	300	—	300	—	300	—	300	µA	t_{RC} = 125µs $\overline{CAS}$ before $\overline{RAS}$ cycling	*4
Standby current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ =V_{IH} $\overline{CAS}$ =V_{IL} Dout =enable	*1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	80	—	70	—	66	—	55	—	47	mA	t_{RC} =Min	
Fast page mode current	I_{CC7}	—	80	—	70	—	55	—	55	—	47	mA	t_{PC} = Min	*1 ,*3
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	-10	10	-10	10	µA	0V ≤ Vin ≤ 7V	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	-10	10	-10	10	µA	0V ≤ Vout ≤ 7V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: *1. I_{CC} depends on output loading condition when the device is selected.
I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
*4. $t_{RAS} = t_{RAS}$ (min) to 1 µs
Input voltage: I/O pins : $V_{IH} \geq V_{CC}$-0.2V, $V_{IL} \leq$ 0.2V or High-Z
the other pins: $V_{IH} \geq V_{CC}$-0.2V or $V_{IL} \leq$ 0.2V

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Item		Symbol	Typ	Max	Unit	Note
Input capacitance	Address	C_{I1}	—	5	pF	*1
	Clock	C_{I2}	—	7	pF	*1
Input/Output capacitance	Data input/Data output	$C_{I/O}$	—	10	pF	*1, *2

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, VCC = 5 V ± 10%, VSS = 0 V)*14

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514256A /AL -6		HM514256A /AL -7		HM514256A /AL-8		HM514256A /AL-10		HM514256A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row addres hold time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	*9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	*1,*7
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	
Refresh period (only for L-version)	t_{REF}	—	64	—	64	—	64	—	64	—	64	ms	

Read Cycle

Item	Symbol	HM514256A /AL -6		HM514256A /AL -7		HM514256A /AL-8		HM514256A /AL-10		HM514256A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	*3,*4
Access time from Address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	*3,*5
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	*6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	*6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

Write Cycle

Item	Symbol	HM514256A /AL -6		HM514256A /AL -7		HM514256A /AL-8		HM514256A /AL-10		HM514256A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	*10
Write command hold time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	*11
Data-in hold time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	*11

Read-Modify-Write Cycle

Item	Symbol	HM514256A /AL -6		HM514256A /AL -7		HM514256A /AL-8		HM514256A /AL-10		HM514256A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	—	95	—	110	—	135	—	160	—	ns	*10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	55	—	60	—	70	—	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	55	—	60	—	70	—	80	—	95	—	ns	*10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

Refresh Cycle

Item	Symbol	HM514256A /AL -6		HM514256A /AL -7		HM514256A /AL-8		HM514256A /AL-10		HM514256A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Item	Symbol	HM514256A /AL -6		HM514256A /AL -7		HM514256A /AL-8		HM514256A /AL-10		HM514256A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	—	1000000	—	100000	ns	*12
Access time from CAS precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	*13
$\overline{RAS}$ hold time from CAS precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast page mode read-write cycle time	t_{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

Notes: *1. AC measurements assume tT = 5ns.

*2. Assumes that tRCD ≤ tRCD (max) and tRAD ≤ tRAD (max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that tRCD ≥ tRCD (max) and tRAD ≤ tRAD (max).

*5. Assumes that tRCD ≤ tRCD (max) and tRAD ≥ tRAD (max).

*6. tOFF (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between VIH and VIL.

*8. Operation with the tRCD (max) limit insures that tRAC (max) can be met, tRCD (max) is specified as a reference point only, if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.

*9. Operation with the tRAD (max) limit insures that tRAC (max) can be met, tRAD (max) is specified as a reference point only, if tRAD is greater than the specified tRAD (max) limit, then access time is controlled exclusively by tAA.

*10. tWCS, tRWD, tCWD and tAWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if tWCS ≥ tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tRWD ≥ tRWD (min), tCWD≥tCWD (min) and tAWD ≥ tAWD (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

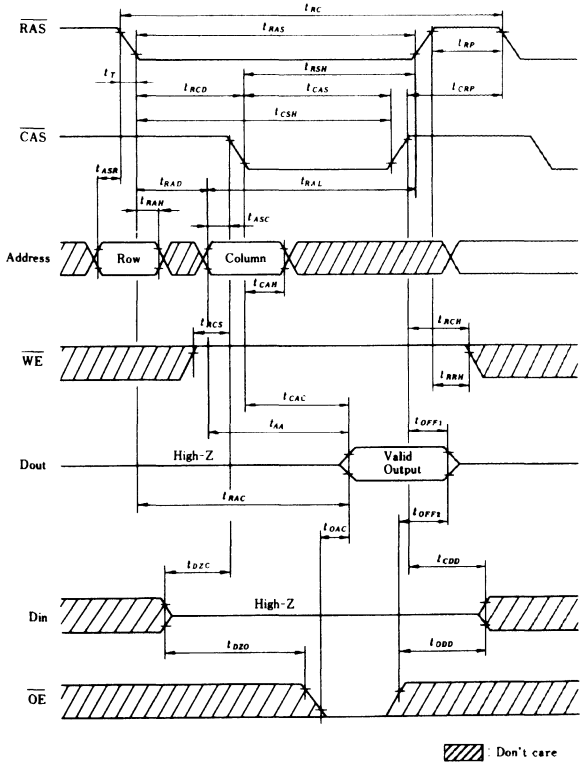
*12. tRASC is determined by $\overline{RAS}$ pulse width in fast page mode cycles.

*13. Access time is determined by the longer of tAA, tCAC or tACP.

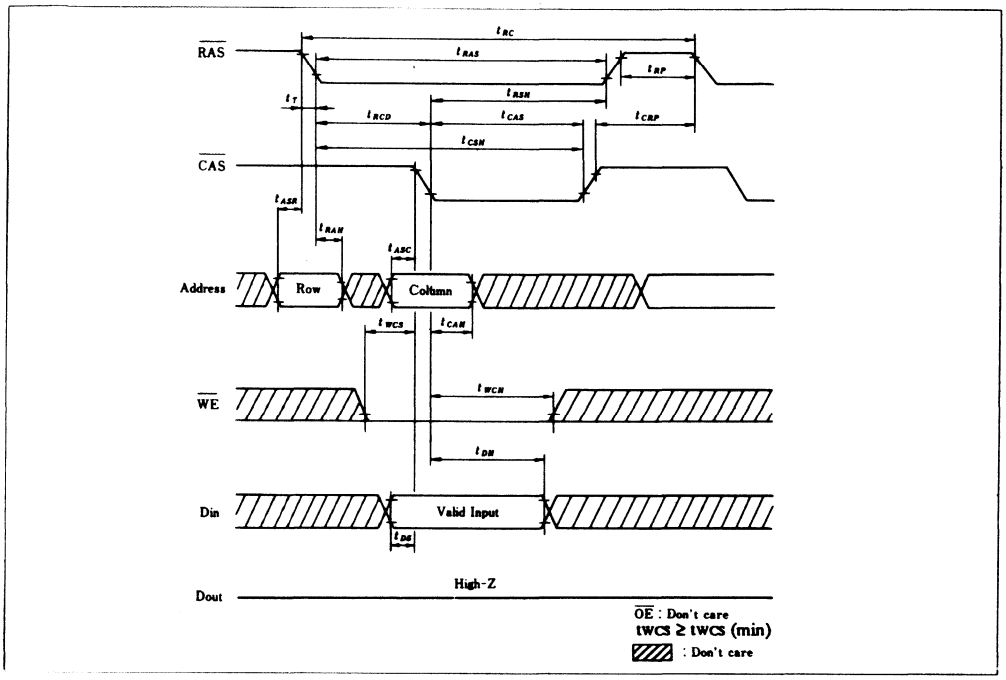
*14. An initial pause of 100 µs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Timing Waveforms

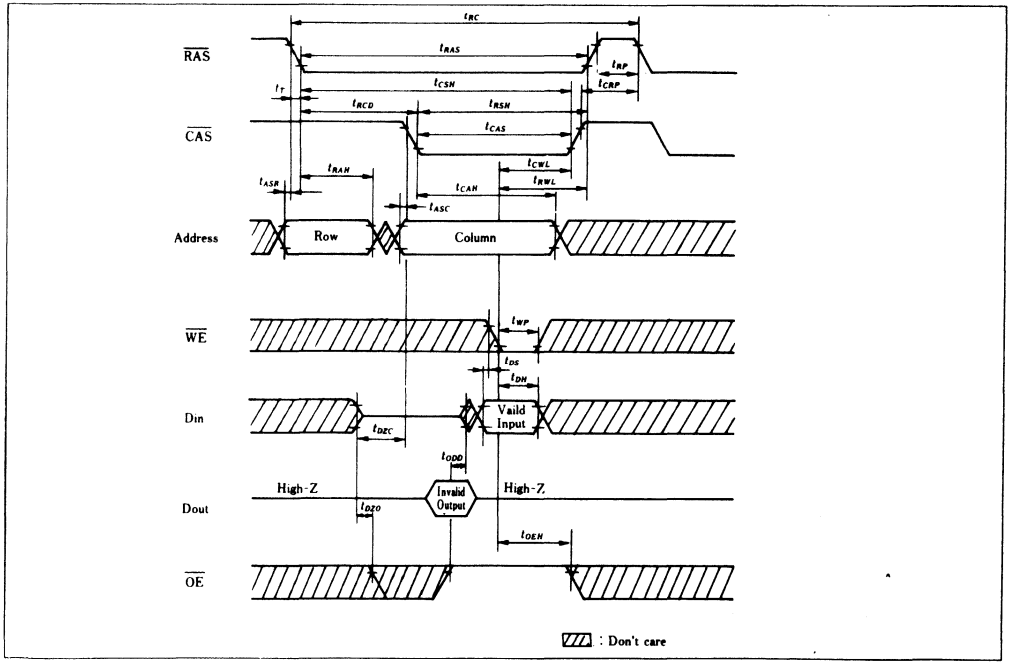
Read Cycle



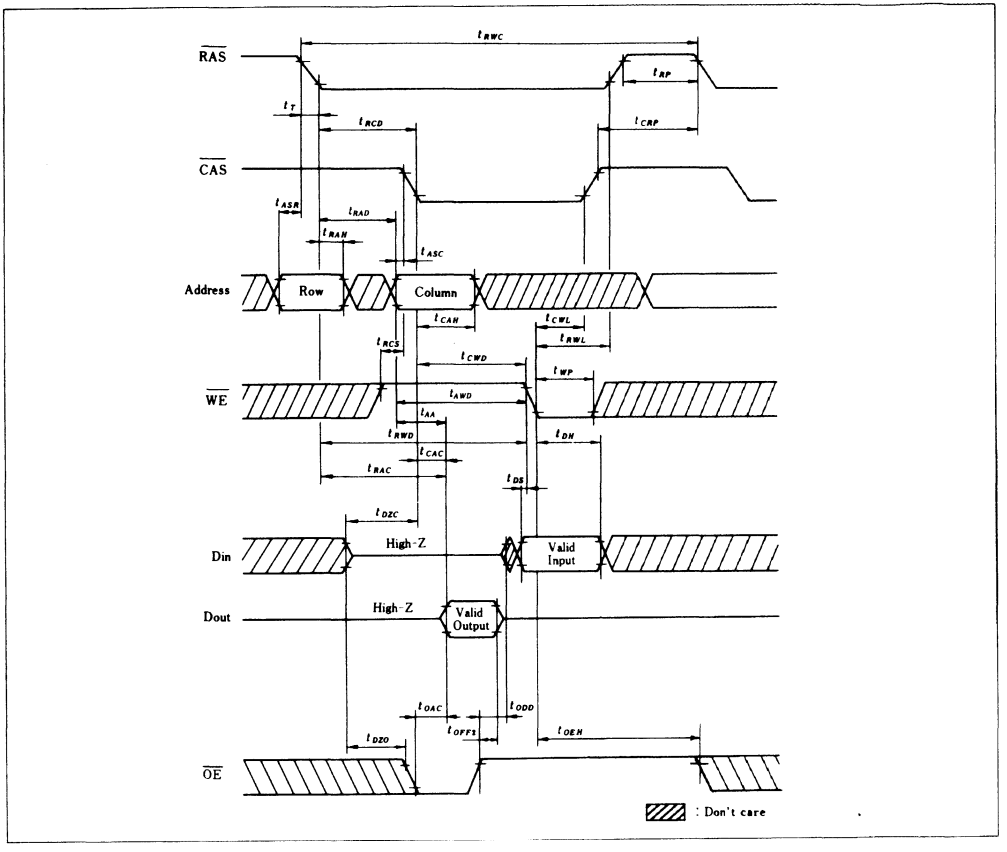
Early Write Cycle



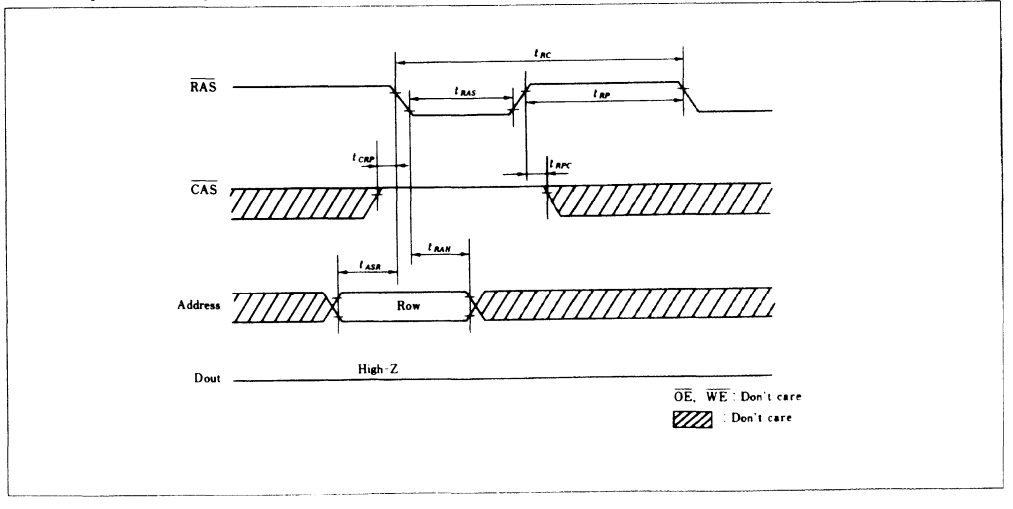
Delayed Write Cycle



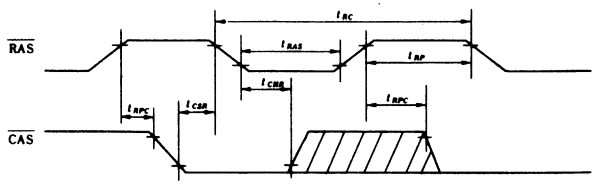
Read-Modify-Write Cycle



RAS-Only Refresh Cycle

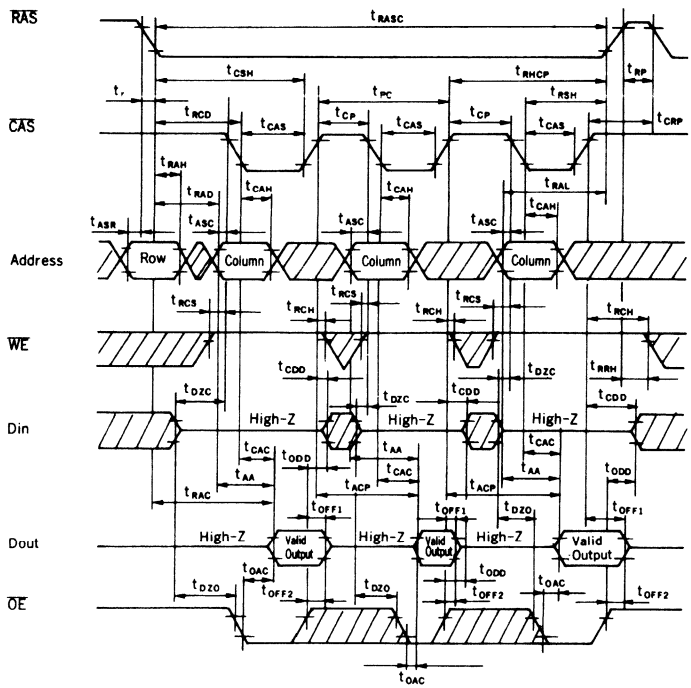


CAS-before-RAS Refresh Cycle



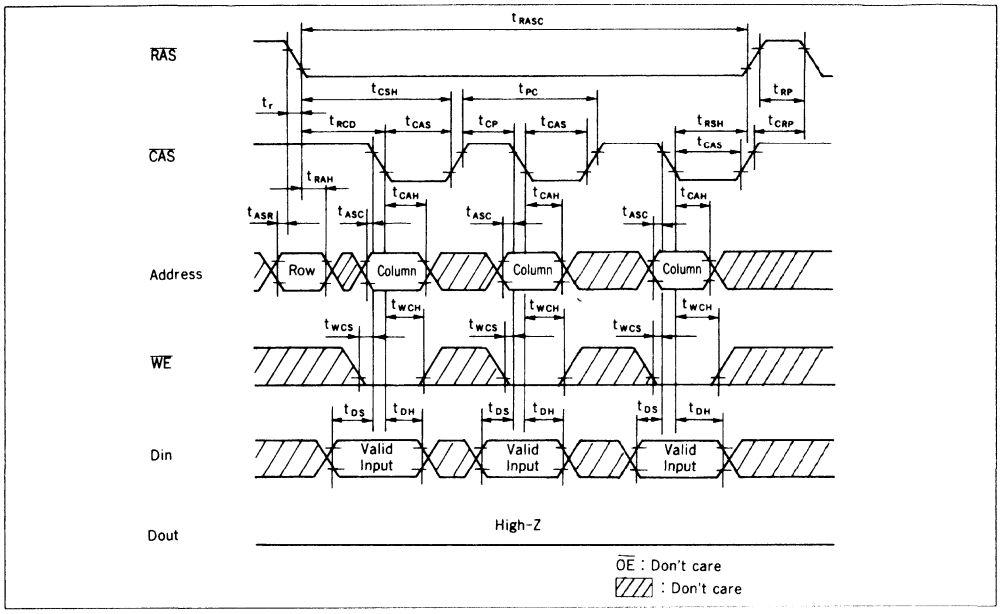
Address, Din, $\overline{WE}$: Don't care
Dout : High-Z
▨ : Don't care

Fast Page Mode Read Cycle

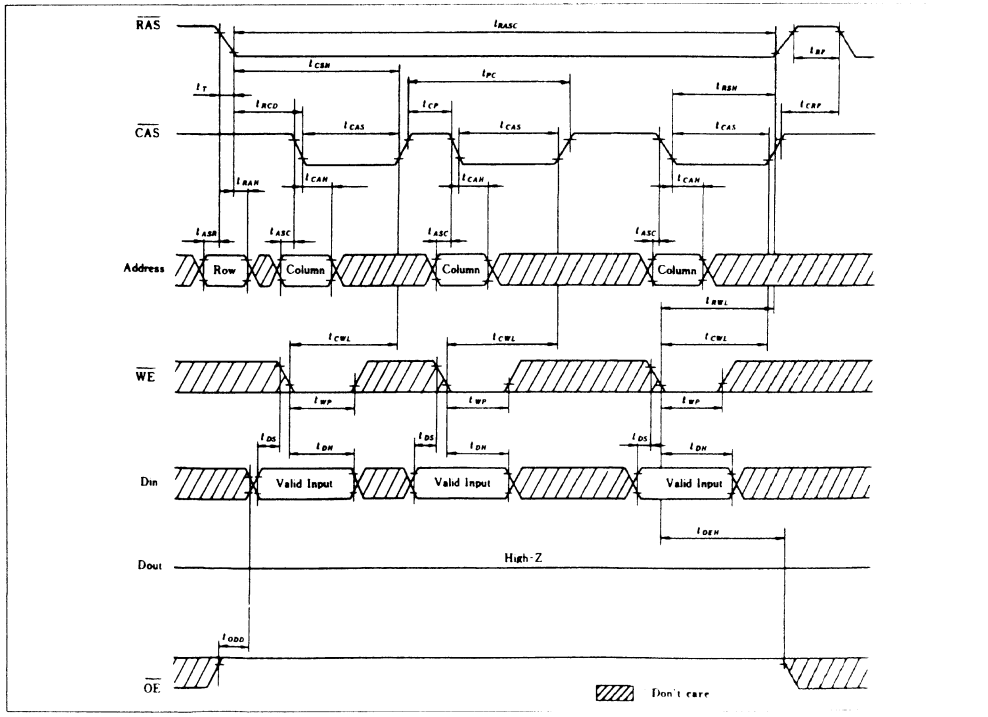


▨ : Don't care

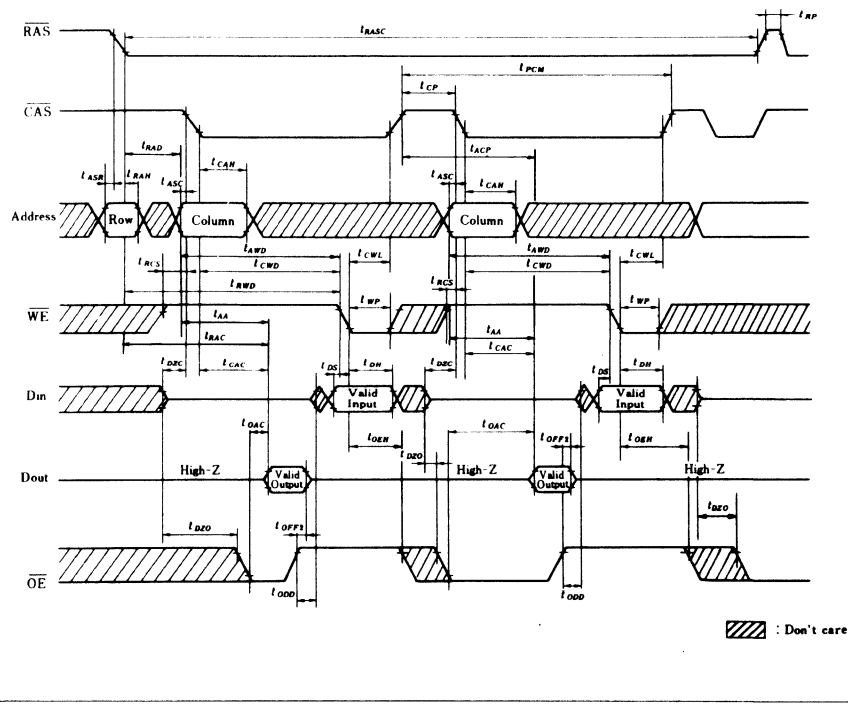
Fast Page Mode Early Write Cycle



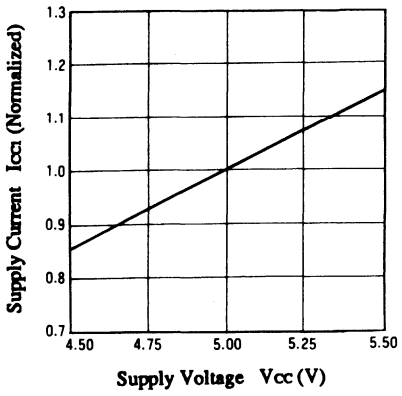
Fast Page Delayed Write Cycle



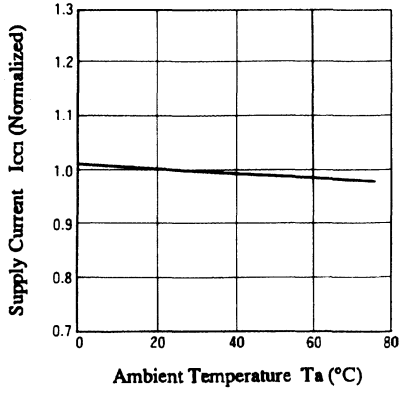
Fast Page Mode Read-Modify-Write Cycle



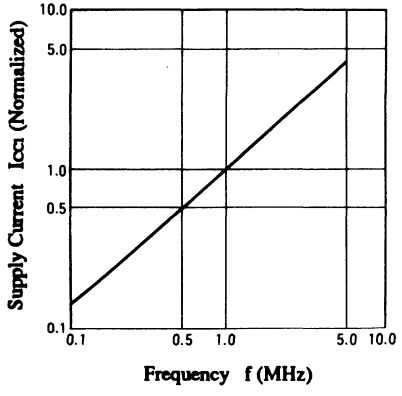
Supply Current (Active) vs. Supply Voltage



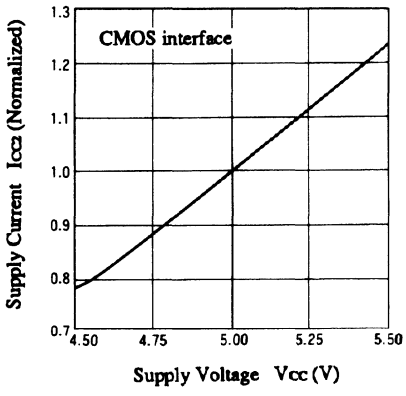
Supply Current (Active) vs. Ambient Temperature



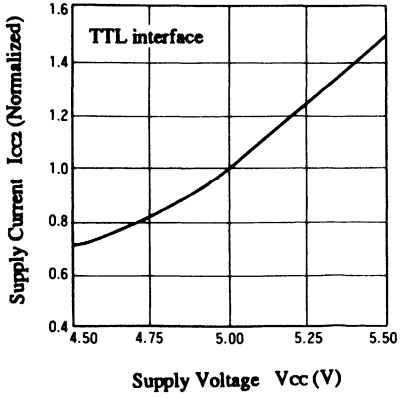
Supply Current (Active) vs. Frequency



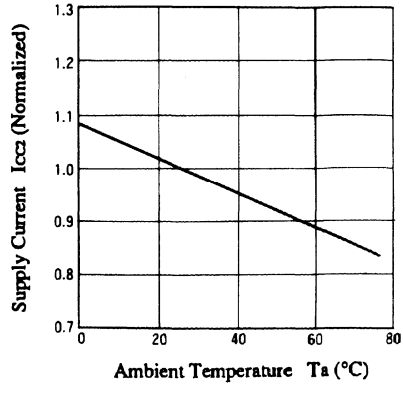
Supply Current (Standby) vs. Supply Voltage



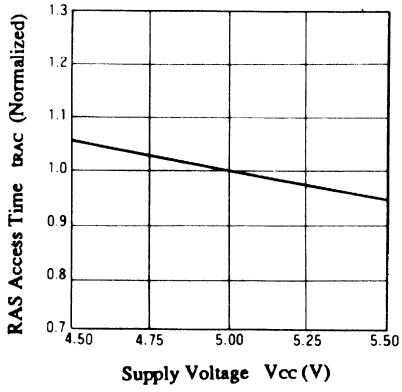
Supply Current (Standby) vs. Supply Voltage



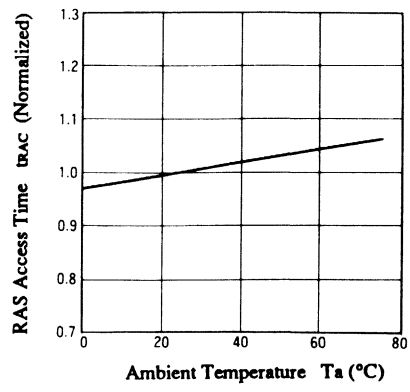
Supply Current (Standby) vs. Ambient Temperature



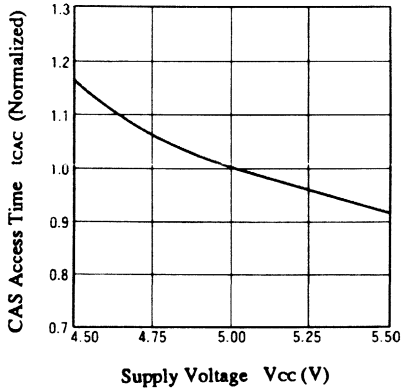
$\overline{RAS}$ Access Time vs. Supply Voltage



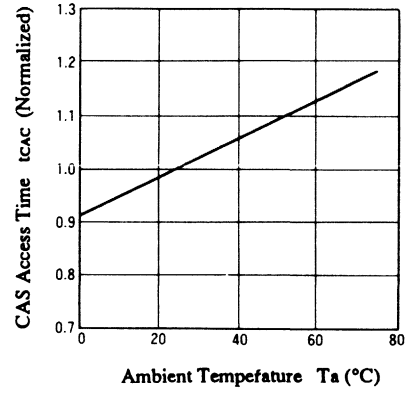
$\overline{RAS}$ Access Time vs. Ambient Temperature



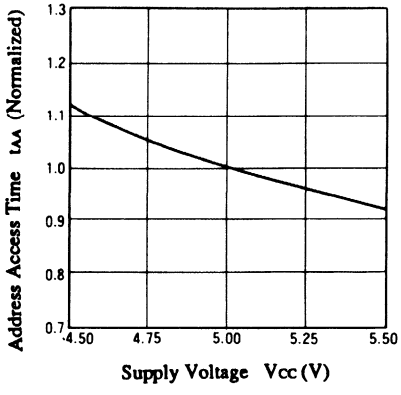
$\overline{CAS}$ Access Time vs. Supply Voltage



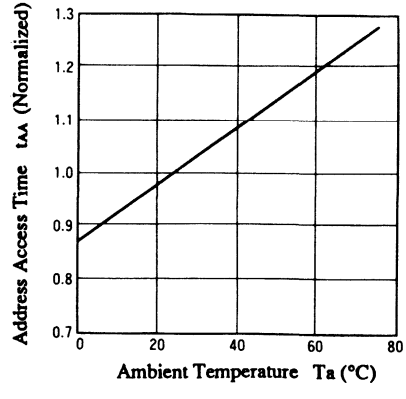
$\overline{CAS}$ Access Time vs. Ambient Temperature



Address Access Time vs. Supply Voltage



Address Access Time vs. Ambient Temperature



HM514256H Series

262144-Word × 4-Bit CMOS Dynamic RAM

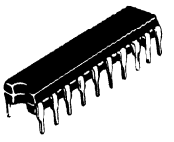
The Hitachi HM514256H is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514256H has realized higher density, higher performance and various functions by employing 1.3 µm CMOS technology and some new CMOS circuit design technologies. The HM514256H offers Fast Page Mode as a high speed access mode.

Multiplexed address input permits the HM514256H to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

Features

- Single 5 V (±10%)
- High speed: Access Time 60 ns/70 ns (max)
- Low power: Standby 11 mW (max)
  Active 495 mW/440 mW (max)
- Fast page mode capability
- 512 refresh cycles: (8 ms)
- 2 variations of refresh: $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

HM514256HP Series

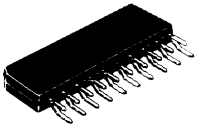


(DP-20NA)

HM514256HJP Series

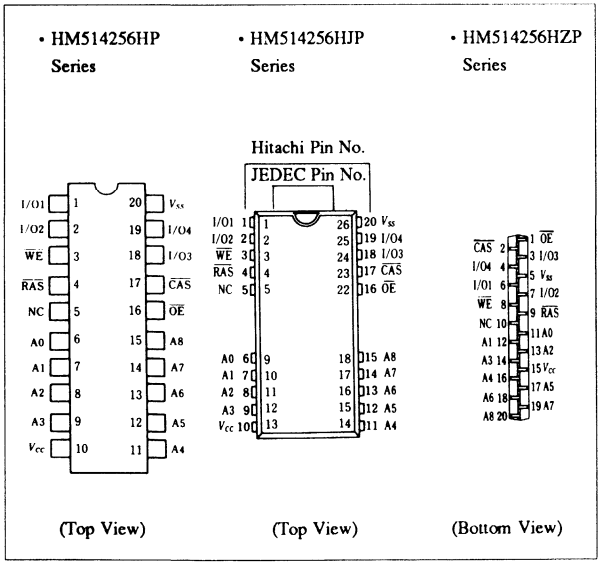
(CP-20D)

HM514256HZP Series



(ZP-20)

Pin Arrangement



Pin Description

Pin Name	Function
A0–A8	Address input
A0–A8	Refresh address input
I/O1–I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power supply (+5 V)
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM514256HP-6	60 ns	300-mil 20-pin plastic DIP (DP-20NA)
HM514256HP-7	70 ns	
HM514256HJP-6	60 ns	300-mil 20-pin plastic SOJ (CP-20D)
HM514256HJP-7	70 ns	
HM514256HZP-6	60 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514256HZP-7	70 ns	

HM514258A Series

262144-Word × 4-Bit CMOS Dynamic RAM

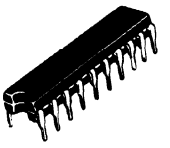
The Hitachi HM514258A is a CMOS dynamic RAM organized 262144-word x 4-bit. HM514258A has realized higher density, higher performance and various functions by employing 1.3 µm CMOS technology and some new CMOS circuit design technologies. The HM514258A offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM514258A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

Features

- Single 5 V (±10%)
- High speed: Access Time 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power: Standby 11 mW (max)
  Active 495 mW/440 mW/413 mW/358 mW/303 mW (max)
- Static column mode capability
- 512 refresh cycles: (8 ms)
- 2 variations of refresh: $\overline{RAS}$-only refresh
  $\overline{CS}$-before-$\overline{RAS}$ refresh

HM514258AP Series

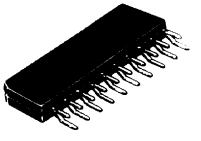


(DP-20NA)

HM514258AJP Series

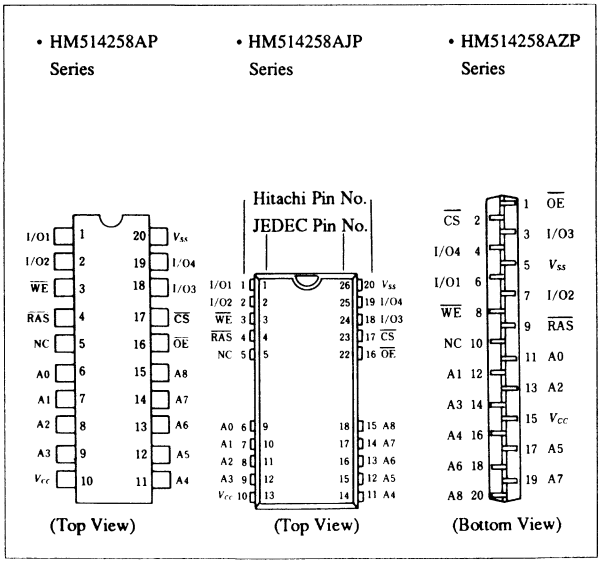
(CP-20D)

HM514258AZP Series



(ZP-20)

Pin Arrangement



Pin Description

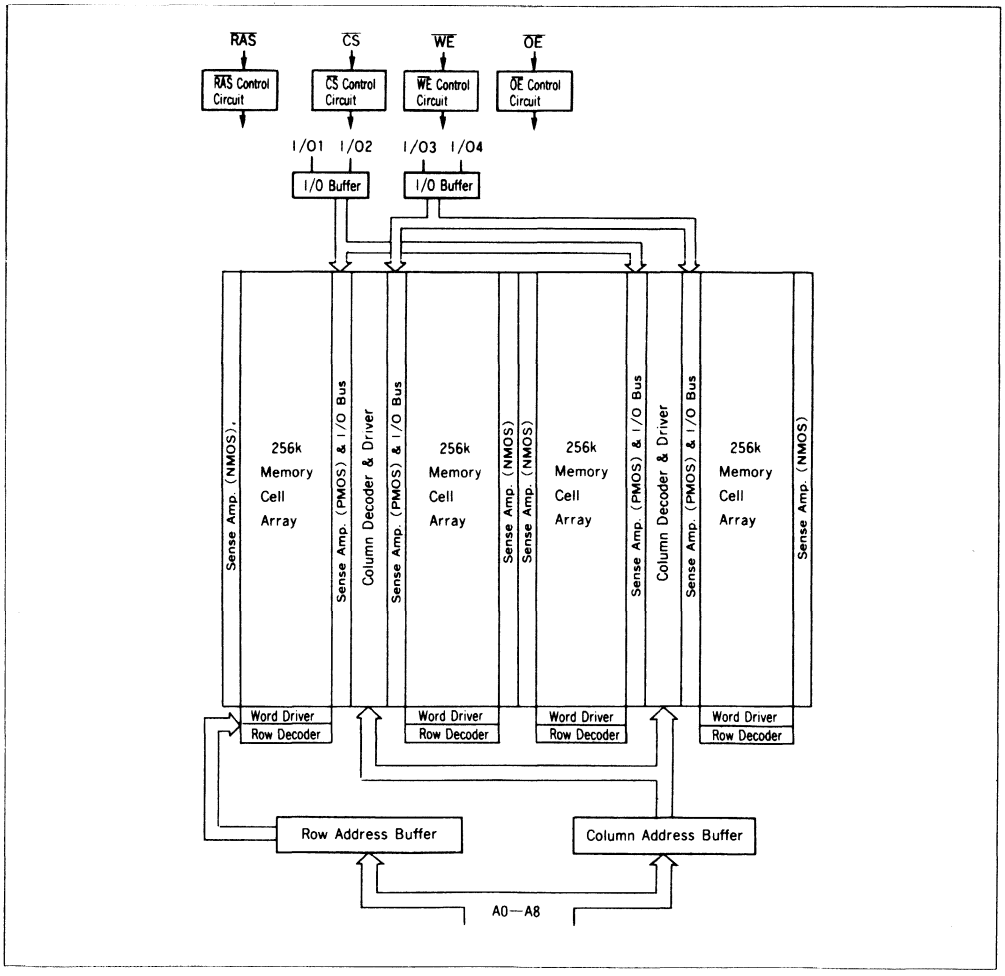
Pin Name	Function
A0–A8	Address input
A0–A8	Refresh address input
I/O1–I/O4	Data input/Data output
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
Vcc	Power supply (+5 V)
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM514258AP-6	60ns	
HM514258AP-7	70ns	300-mil 20-pin
HM514258AP-8	80 ns	plastic DIP
HM514258AP-10	100 ns	(DP-20NA)
HM514258AP-12	120 ns	
HM514258AJP-6	60ns	
HM514258AJP-7	70ns	300-mil 20-pin
HM514258AJP-8	80 ns	plastic SOJ
HM514258AJP-10	100 ns	(CP-20D)
HM514258AJP-12	120 ns	

Type No.	Access Time	Package
HM514258AZP-6	60ns	
HM514258AZP-7	70ns	400-mil 20-pin
HM514258AZP-8	80 ns	plastic ZIP
HM514258AZP-10	100 ns	(ZP-20)
HM514258AZP-12	120 ns	

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−1.0 to +7.0	V
Supply voltage relative to Vss	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item		Symbol	Min	Typ	Max	Unit	Note
Supply voltage		Vss	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	*1
Input high voltage		V_{IH}	2.4	—	6.5	V	*1
Input low voltage	I/O pin	V_{IL}	−1.0	—	0.8	V	*1
	Others	V_{IL}	−2.0	—	0.8	V	*1

Note: *1. All voltage referenced to Vss.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, Vss = 0V)

Item	Symbol	HM514258A-6 Min	HM514258A-6 Max	HM514258A-7 Min	HM514258A-7 Max	HM514258A-8 Min	HM514258A-8 Max	HM514258A-10 Min	HM514258A-10 Max	HM514258A-12 Min	HM514258A-12 Max	Unit	Test Conditions	Note
Operating current	I_{CC1}	—	90	—	80	—	75	—	65	—	55	mA	$\overline{RAS}$, $\overline{CS}$ cycling tRC = Min	*1, *2
Standby current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	$\overline{RAS}$, $\overline{CS}$ = V_{IH} TTL Dout = High-Z interface	
		—	1	—	1	—	1	—	1	—	1		$\overline{RAS}$, $\overline{CS}$ ≥ Vcc-0.2V CMOS Dout = High-Z interface	
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	75	—	65	—	55	mA	tRC = Min	*2
Standby current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IL} Dout = enable	*1
$\overline{CS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	80	—	70	—	65	—	55	—	45	mA	tRC = Min	
Static column mode current	I_{CC9}	—	80	—	70	—	65	—	55	—	45	mA	tSC = Min	*1, *3
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	μA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	Vcc	2.4	Vcc	2.4	Vcc	2.4	Vcc	2.4	Vcc	V	High Iout = −5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: *1. Icc depends on output load condition when the device is selected.
Icc max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Item		Symbol	Typ	Max	Unit	Note
Input capacitance	Address	C_{I1}	—	5	pF	*1
	Clock	C_{I2}	—	7	pF	*1
Input/Output capacitance	Data input/Data output	$C_{I/O}$	—	10	pF	*1, *2

Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*17, *18

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Item	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ pulse width	t_{SP}	20	10000	20	10000	25	10000	30	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column address setup time	t_{ASW}	0	—	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{AHW}	15	—	15	—	20	—	25	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	22	55	25	70	25	90	ns	*8
$\overline{RAS}$ hold time	t_{RSL}	20	—	20	—	25	—	30	—	30	—	ns	
$\overline{CS}$ hold time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{SRS}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	*1, *7
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Item	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	tRAC	—	60	—	70	—	80	—	100	—	120	ns	*2, *3
Access time from $\overline{CS}$	tACS	—	20	—	20	—	25	—	30	—	30	ns	*3, *4
Access time from address	tAA	—	30	—	35	—	40	—	50	—	55	ns	*3, *5, *14
Access time from $\overline{OE}$	tOAC	—	20	—	20	—	25	—	25	—	30	ns	
Read command setup time	tRCS	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CS}$	tRCH	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	tRRH	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to column address hold time	tAHR	15	—	15	—	15	—	15	—	15	—	ns	*16
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	17	40	20	50	20	65	ns	*9
Column address to $\overline{RAS}$ lead time	tRAL	30	—	35	—	40	—	50	—	55	—	ns	
Column address hold time from $\overline{RAS}$	tAR	60	—	70	—	80	—	100	—	120	—	ns	
Output buffer turn-off time	tOFF	—	20	—	20	—	20	—	25	—	30	ns	*6
Output buffer turn-off to $\overline{OE}$	tOFF2	—	20	—	20	—	20	—	25	—	30	ns	*6
Output hold time from address	tAOH	5	—	5	—	5	—	5	—	5	—	ns	
$\overline{CS}$ to Din delay time	tCDD	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{CS}$ hold time from $\overline{OE}$	tOCH	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{OE}$ hold time from $\overline{RAS}$	tROH	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{OE}$ hold time from $\overline{CS}$	tCOH	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{OE}$ pulse width	tOEP	20	—	20	—	25	—	25	—	30	—	ns	

Write Cycle

Item	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	tWCS	0	—	0	—	0	—	0	—	0	—	ns	*10
Write command hold time	tWCH	15	—	15	—	20	—	25	—	25	—	ns	
Write command hold time to $\overline{RAS}$	tWCR	55	—	65	—	75	—	95	—	115	—	ns	
Write command pulse width	tWP	10	—	10	—	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	tRWL	20	—	20	—	25	—	25	—	30	—	ns	
Write command to $\overline{CS}$ lead time	tCWL	20	—	20	—	25	—	25	—	30	—	ns	
Din setup time	tDS	0	—	0	—	0	—	0	—	0	—	ns	*11
Din hold time	tDH	15	—	15	—	20	—	25	—	25	—	ns	*11
Din hold time to $\overline{RAS}$	tDHR	55	—	65	—	75	—	95	—	115	—	ns	
Column address hold time from $\overline{RAS}$	tAWR	55	—	65	—	75	—	95	—	115	—	ns	

Read-Modify-Write Cycle

Item	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	tRWC	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	85	—	93	—	110	—	135	—	160	—	ns	*10
$\overline{CS}$ to $\overline{WE}$ delay time	tCWD	45	—	45	—	55	—	65	—	70	—	ns	*10
Column address to $\overline{WE}$ delay time	tAWD	55	—	60	—	70	—	85	—	95	—	ns	*10

Refresh Cycle

Item	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	tCSR	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	tCHR	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	tZRH	10	—	10	—	10	—	10	—	10	—	ns	

Static Column Mode Cycle

Item	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Static column mode cycle time	tSC	35	—	40	—	45	—	55	—	60	—	ns	
Static column mode $\overline{RAS}$ pulse width	tRASC	—	100000	—	100000	—	100000	—	100000	—	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	tRSWD	70	—	80	—	90	—	110	—	135	—	ns	
Static column mode $\overline{CS}$ precharge time	tSI	10	—	10	—	10	—	10	—	15	—	ns	
Static column mode $\overline{WE}$ precharge time	tWI	10	—	10	—	10	—	10	—	15	—	ns	

Static Column Mode Read-Modify-Write Cycle and Mixed Cycle

Item	Symbol	HM514258A -6		HM514258A -7		HM514258A -8		HM514258A -10		HM514258A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Static column mode cycle time on read-modify-write	tSRW	90	—	100	—	120	—	140	—	160	—	ns	*12
Access time from first $\overline{WE}$	tALW	—	65	—	75	—	85	—	100	—	115	ns	*3, *13
Last $\overline{WE}$ to column address delay time	tLWAD	20	35	20	40	25	45	25	50	30	60	ns	*15
Last $\overline{WE}$ to column address hold time	tAHLW	65	—	75	—	85	—	100	—	115	—	ns	

Notes: *1. AC measurements assume tT = 5ns.

*2. Assumes that tRCD ≤ tRCD (max) and tRAD ≤ tRAD (max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that tRCD ≥ tRCD (max) and tRAD ≤ tRAD (max).

*5. Assumes that tRCD ≤ tRCD (max) and tRAD ≥ tRAD (max).

*6. tOFF (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between VIH and VIL.

*8. Operation with the tRCD (max) limit insures that tRAC (max) can be met, tRCD (max) is specified as a reference point only, if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tACS.

*9. Operation with the tRAD (max) limit insures that tRAC (max) can be met, tRAD (max) is specified as a reference point only, if tRAD is greater than the specified tRAD (max) limit, then access time is controlled exclusively by tAA.

*10. tWCS, tRWD, tCWD and tAWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if tWCS ≥ tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tRWD ≥ tRWD (min), tCWD≥tCWD (min) and tAWD ≥ tAWD (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

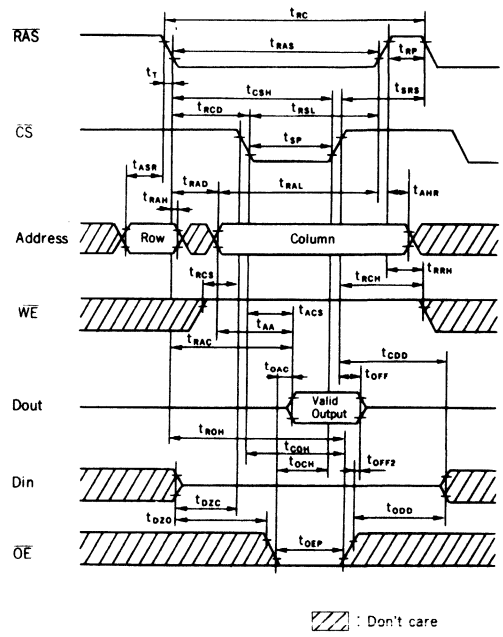
*11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-wirte cycles.

*12. tSRW (min) = tAWD (min) + tLWAD (max) + tT

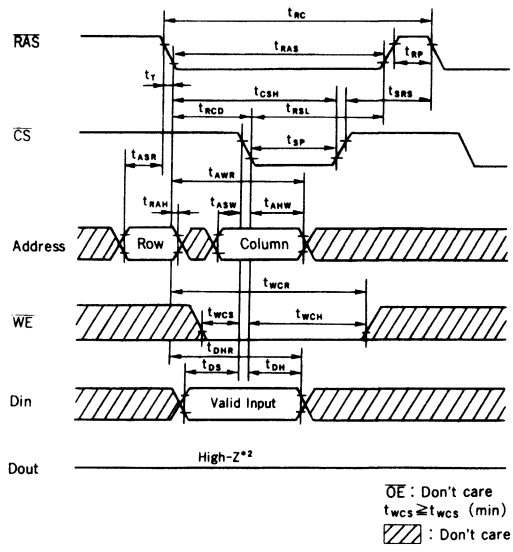
*13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recomended value shown in this table, t_{ALW} exceeds the value shown.
*14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
*15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
*16. t_{AHR} is defined as the time at which the column address hold.
*17. An initial pause of 100 µs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CS}$-before-$\overline{RAS}$ refresh cycles are required.
*18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.

Timing Waveforms

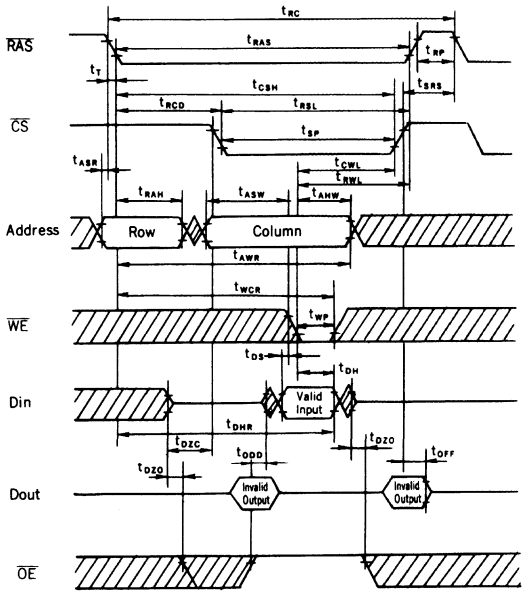
Read Cycle



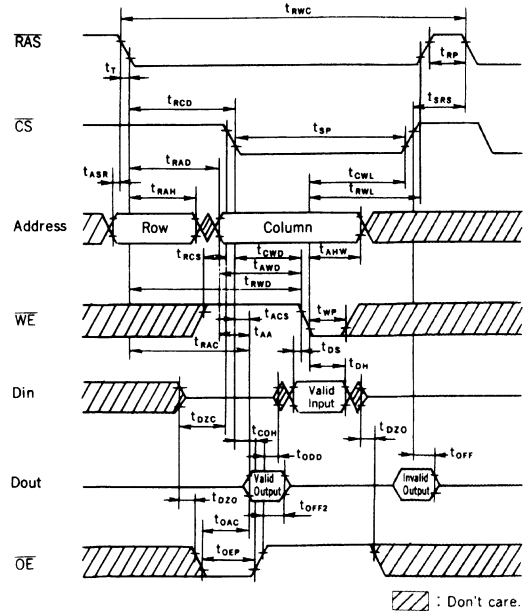
Early Write Cycle



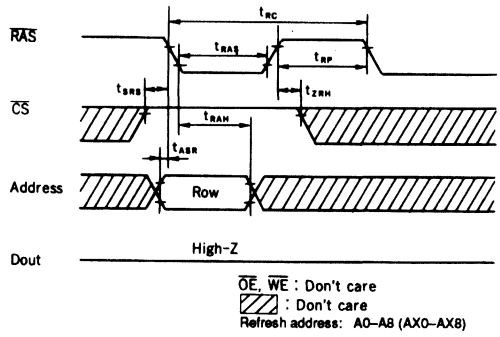
Delayed Write Cycle



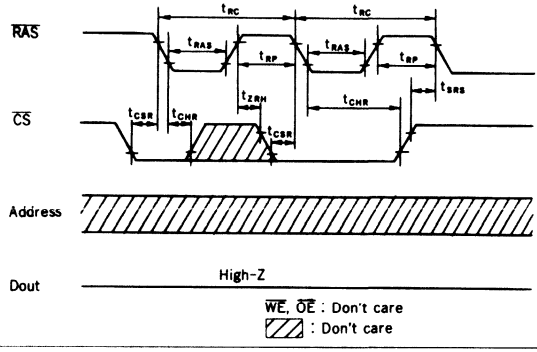
Read-Modify-Write Cycle



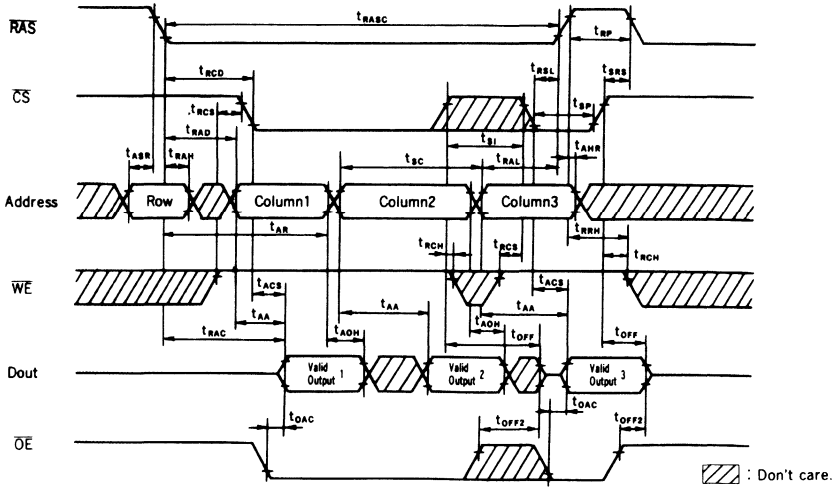
RAS-Only Refresh Cycle



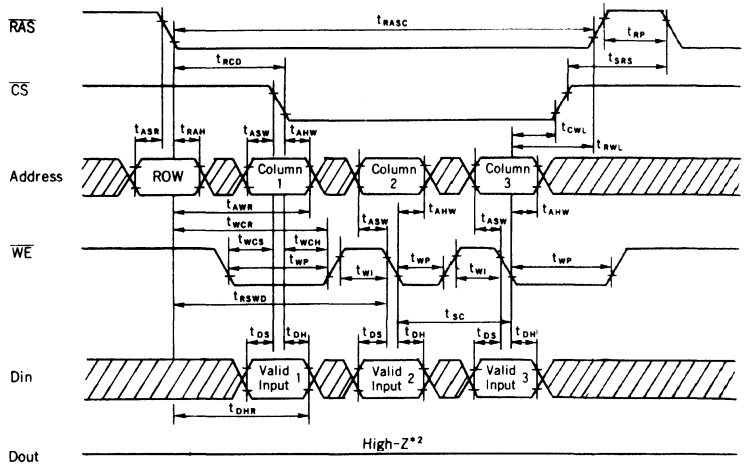
CS-before-RAS Refresh Cycle



Static Column Mode Read Cycle

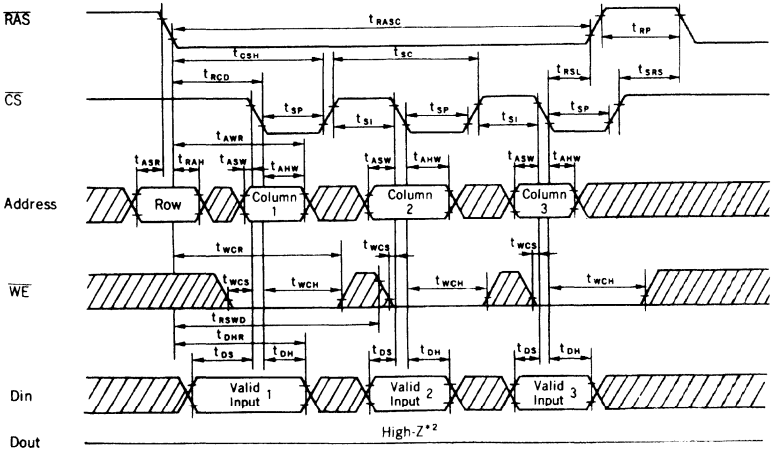


Static Column Mode Write Cycle (1)



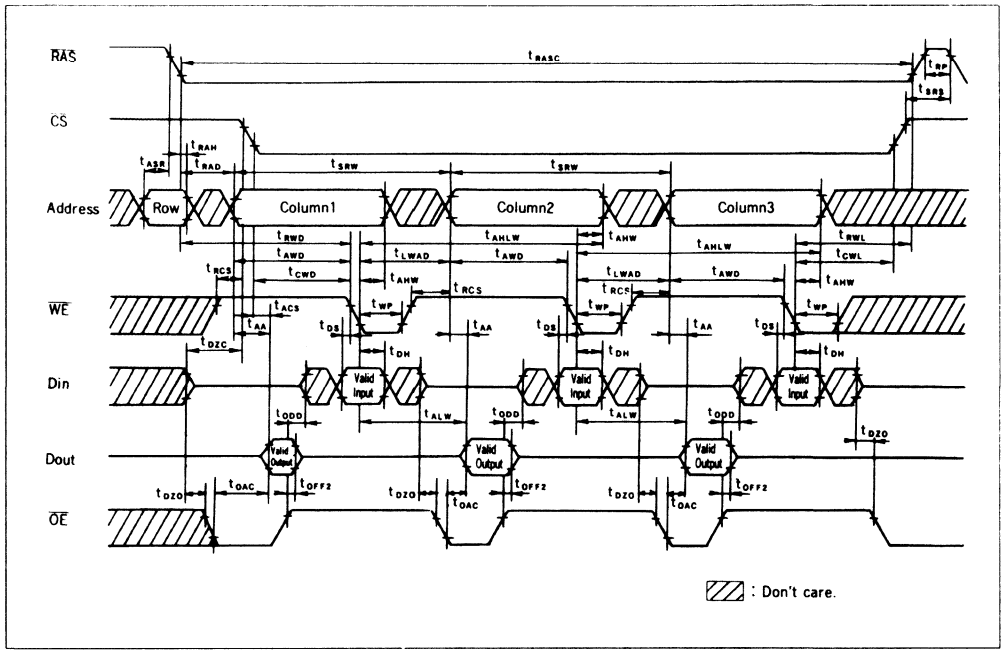
1. ▨ : Don't care
2. $t_{WCS} \geqq t_{WCS}(min)$
3. $\overline{OE}$: Don't care

Static Column Mode Write Cycle (2)

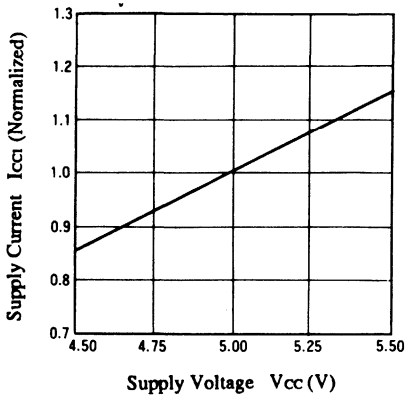


1. ▨ : Don't care.
2. $t_{WCS} \geqq t_{WCS}(min)$
3. OE : Don't care.

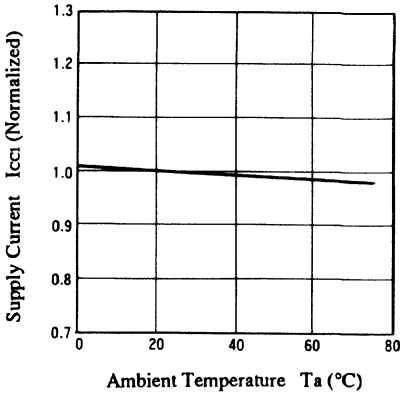
Static Column Mode Read-Modify-Write Cycle



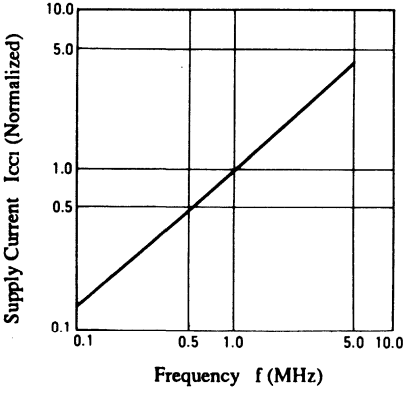
Supply Current (Active) vs. Supply Voltage



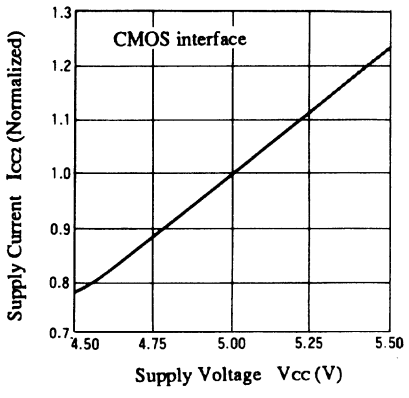
Supply Current (Active) vs. Ambient Temperature



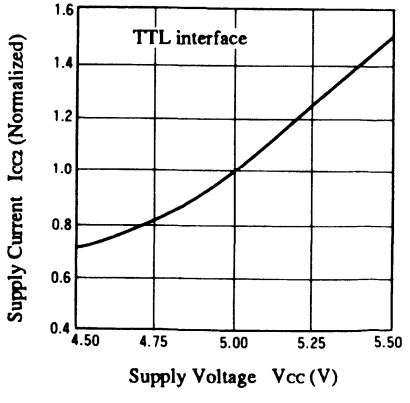
Supply Current (Active) vs. Frequency



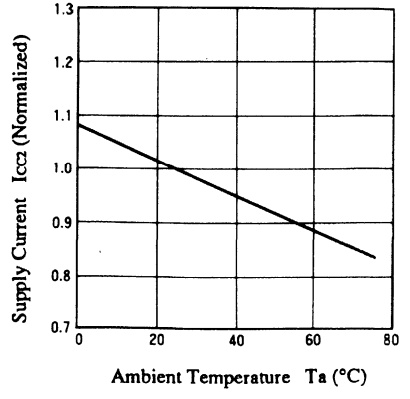
Supply Current (Standby) vs. Supply Voltage



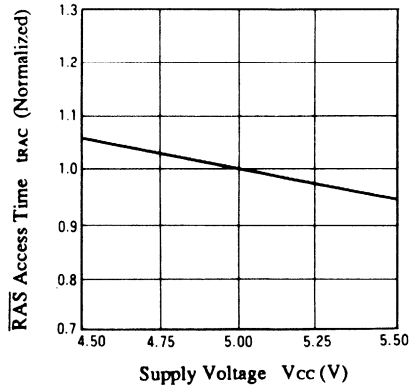
Supply Current (Standby) vs. Supply Voltage



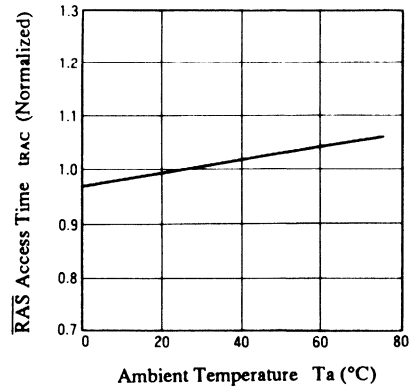
Supply Current (Standby) vs. Ambient Temperature



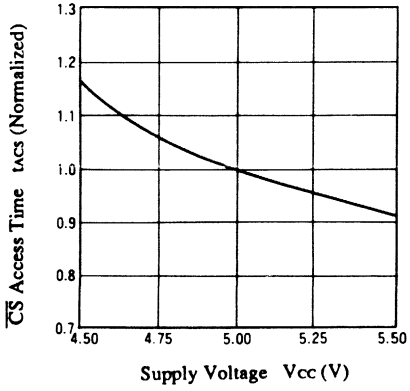
$\overline{RAS}$ Access Time vs. Supply Voltage



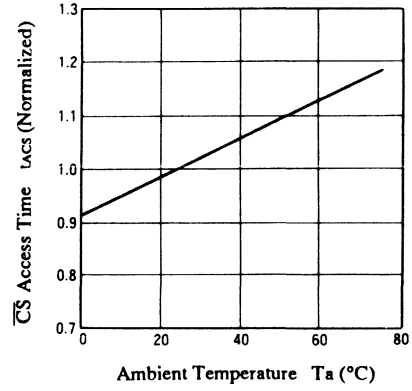
$\overline{RAS}$ Access Time vs. Ambient Temperature



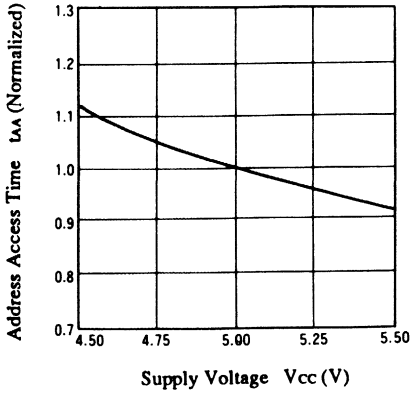
$\overline{CS}$ Access Time vs. Supply Voltage



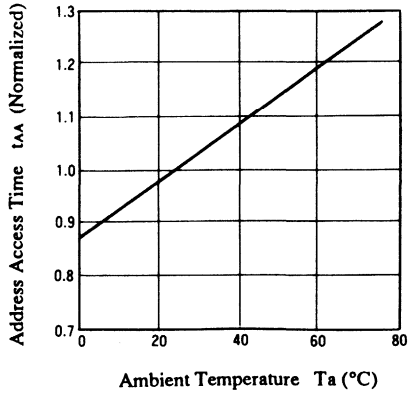
$\overline{CS}$ Access Time vs. Ambient Temperature



Address Access Time vs. Supply Voltage



Address Access Time vs. Ambient Temperature



HM514266A Series — Preliminary

262,144-Word × 4-Bit Dynamic RAM

The Hitachi HM514266A is a CMOS dynamic RAM organized 262,144-word × 4-bit. HM514266A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies. The HM514266A offers fast page mode as a high speed access mode.

Multiplexed address input permits HM514266A to be packaged in standard 20-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

Features

- Single 5 V (± 10%)
- High speed
  - Access time: 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 495 mW/440 mW/363 mW 303 mW/259 mW (max)
  - Standby mode: 11 mW (max)
- Fast page mode capability
- 512 refresh cycles: 8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- Write per bit capability

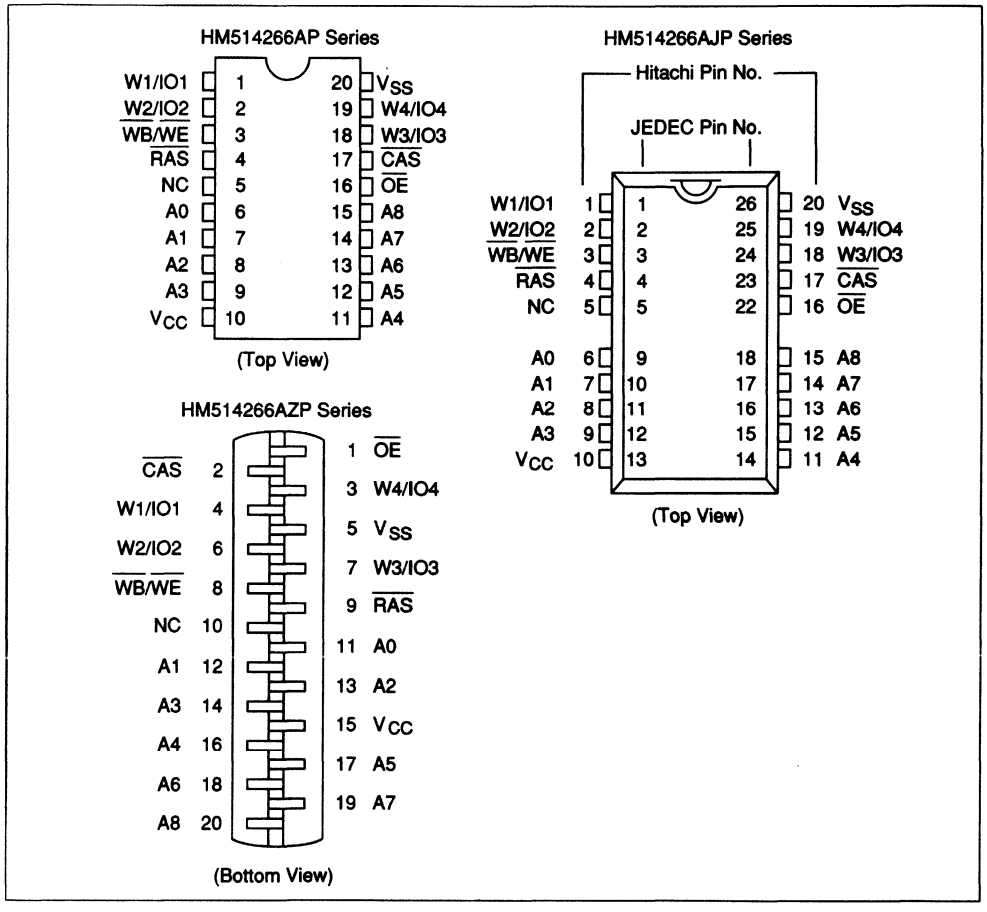
Ordering Information

Type No.	Access time	Package
HM514266AP-6	60 ns	300-mil 20-pin plastic DIP (DP-20NA)
HM514266AP-7	70 ns	
HM514266AP-8	80 ns	
HM514266AP-10	100 ns	
HM514266AP-12	120 ns	
HM514266AJP-6	60 ns	300-mil 20-pin plastic SOJ (CP-20D)
HM514266AJP-7	70 ns	
HM514266AJP-8	80 ns	
HM514266AJP-10	100 ns	
HM514266AJP-12	120 ns	

Type No.	Access time	Package
HM514266AZP-6	60 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514266AZP-7	70 ns	
HM514266AZP-8	80 ns	
HM514266AZP-10	100 ns	
HM514266AZP-12	120 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Arrangement

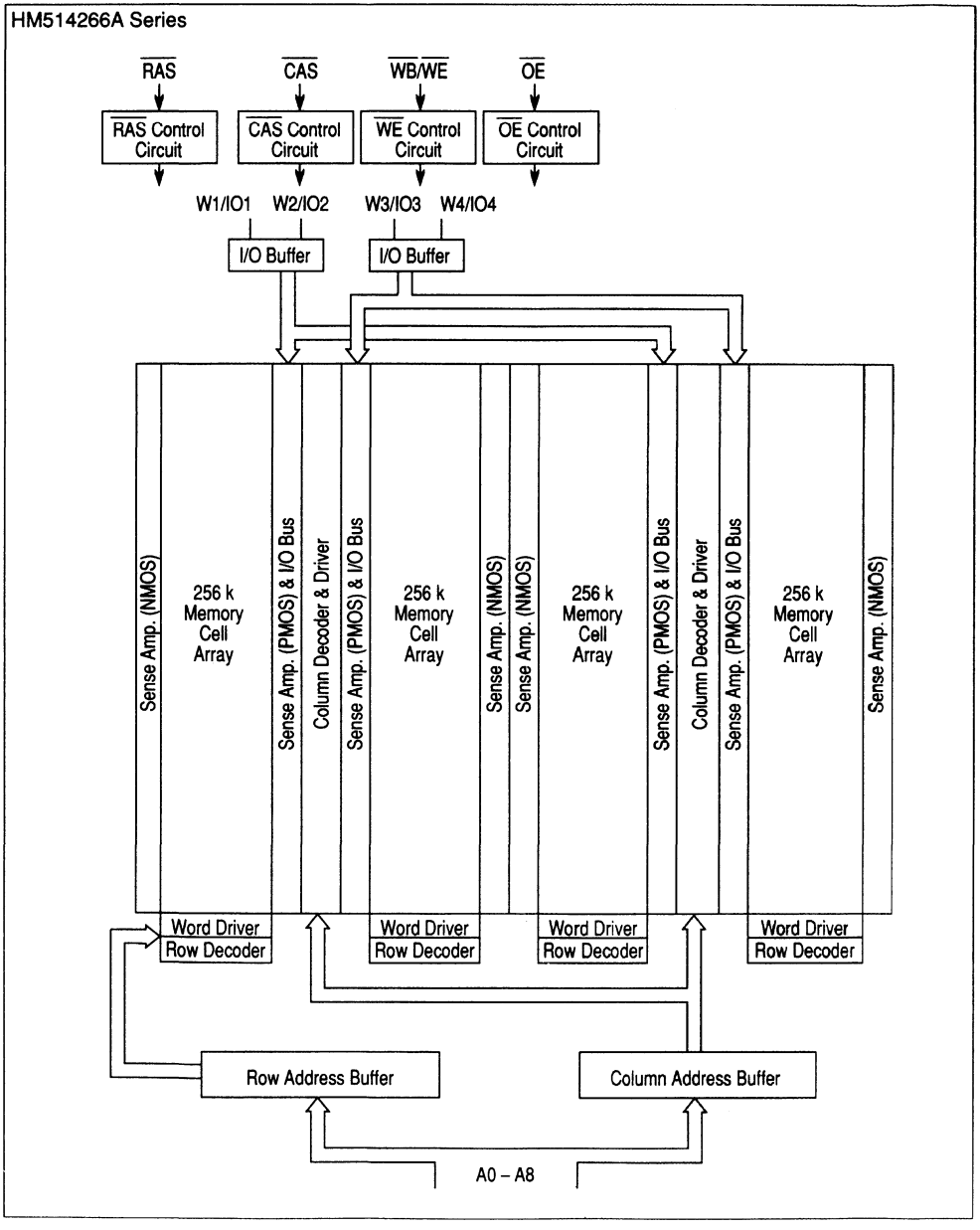


Pin Description

Pin name	Function
A0 – A8	Address input
A0 – A8	Refresh address input
W1/IO1 – W1/IO4	Write select/data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe

Pin name	Function
$\overline{WB/WE}$	Write per bit/write enable
$\overline{OE}$	Output enable
V_{CC}	Power supply (+5.0 V)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input high voltage		V_{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin)	V_{IL}	–1.0	—	0.8	V	1
	(Others)	V_{IL}	–2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514266A										
		-6		-7		-8		-10		-12		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	90	—	80	—	66	—	55	—	47	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High – Z	

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514266A														
		-6		-7		-8		-10		-12						
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions			Notes
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	66	—	55	—	47	mA	t_{RC} = min			2
Standby current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable			1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	80	—	70	—	66	—	55	—	47	mA	t_{RC} = min			
Fast page mode current	I_{CC7}	—	80	—	70	—	55	—	55	—	47	mA	t_{PC} = min			1, 3
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V			
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable			
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = −5 mA			
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA			

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *14

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters) (cont)

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	20	—	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	0	—	0	—	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access time from address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Access time from $\overline{OE}$	t_{OAC}	—	20	—	20	—	25	—	25	—	30	ns	

Read Cycle (cont)

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF1}	—	20	—	20	—	20	—	25	—	30	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	—	20	—	20	—	20	—	25	—	30	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	20	—	20	—	25	—	30	—	ns	

Write Cycle

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	

Write Cycle (cont)

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-write cycle time	t_{RWC}	170	—	180	—	220	—	255	—	295	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	85	—	95	—	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	45	—	45	—	55	—	60	—	70	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	55	—	60	—	70	—	80	—	95	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	20	—	20	—	25	—	25	—	30	—	ns	

Refresh Cycle

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	13
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	
Fast page mode read-write cycle time	t_{PCM}	95	—	100	—	110	—	115	—	135	—	ns	

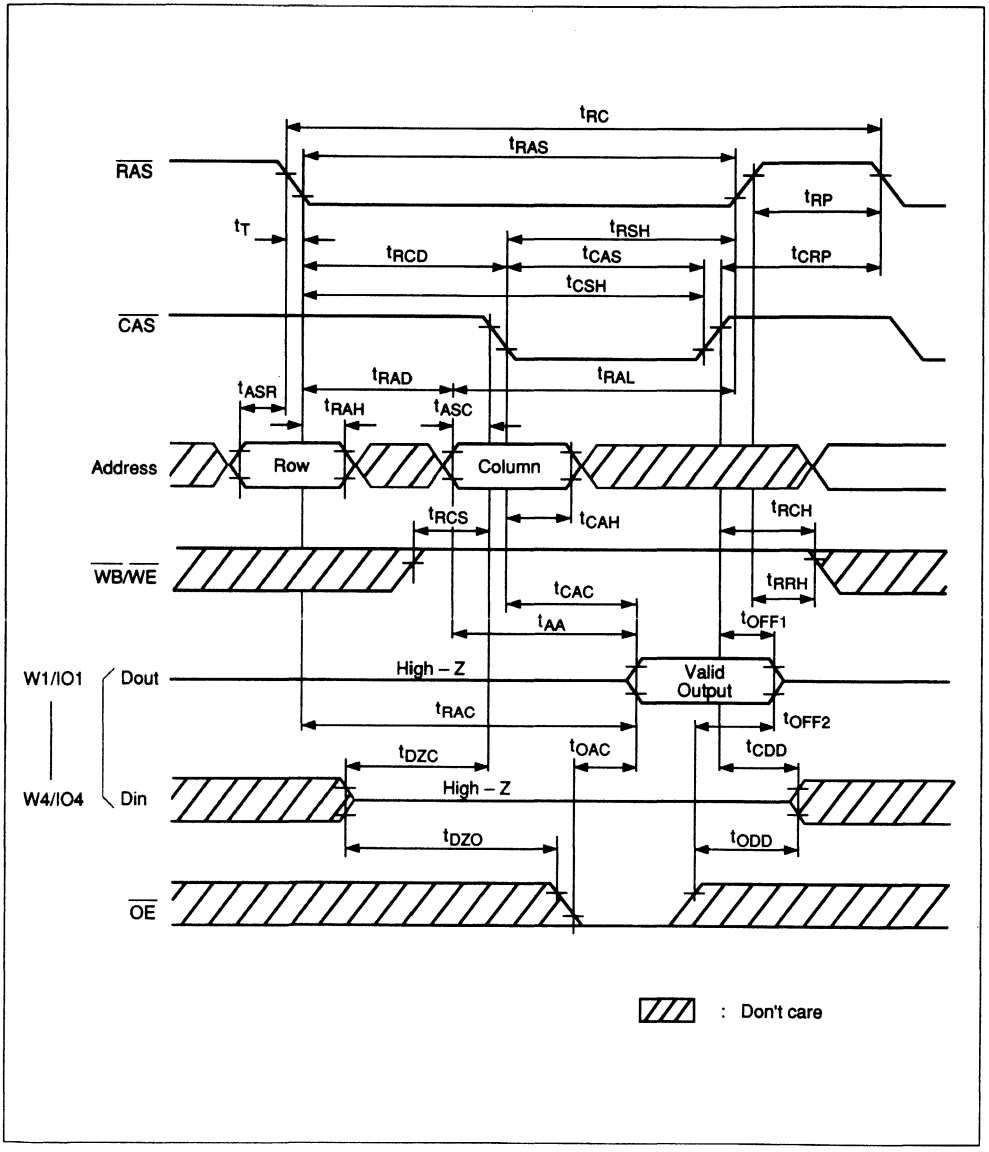
Write Per Bit *15, *16

		HM514266A											
		-6		-7		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write per bit setup time	t_{WBS}	0	—	0	—	0	—	0	—	0	—	ns	
Write per bit hold time	t_{WBH}	10	—	10	—	12	—	15	—	15	—	ns	
Write per bit selection setup time	t_{WDS}	0	—	0	—	0	—	0	—	0	—	ns	
Write per bit selection hold time	t_{WDH}	10	—	10	—	12	—	15	—	15	—	ns	

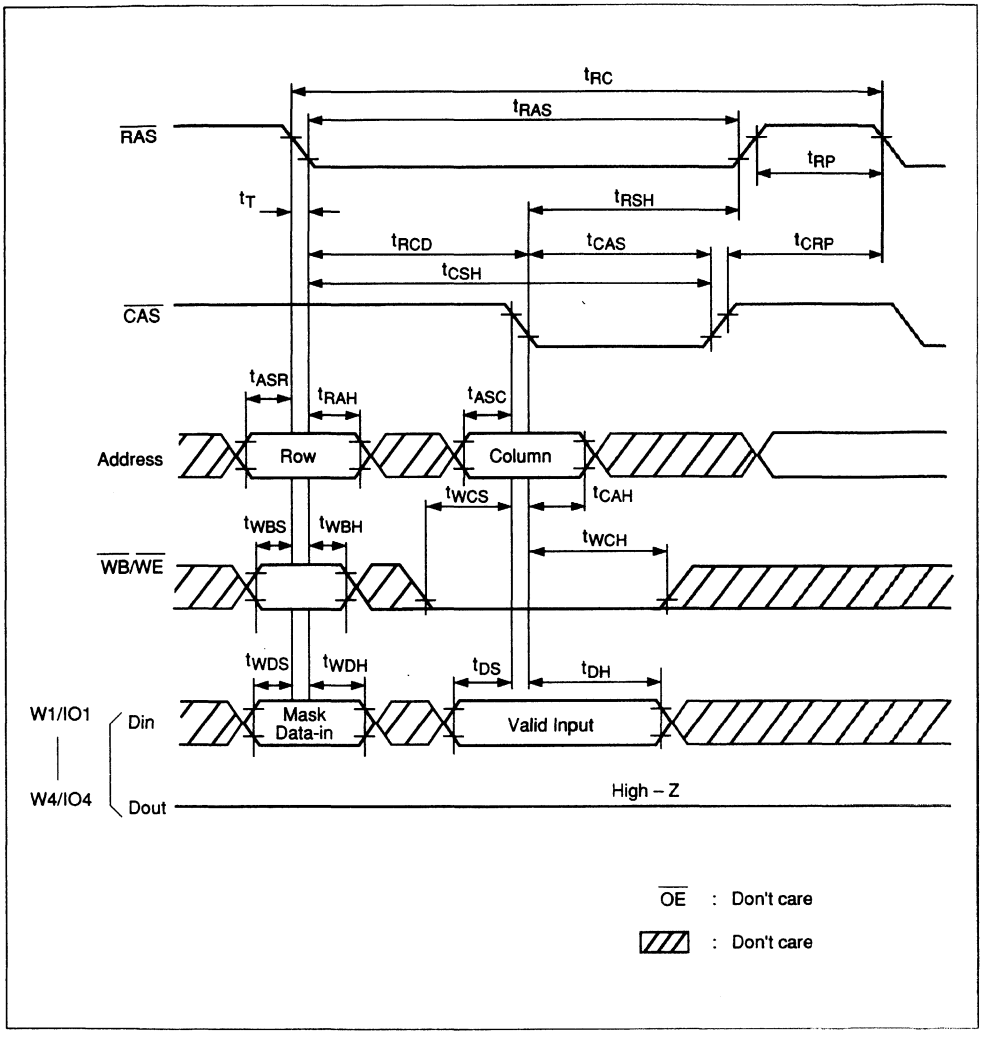
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical charactgeristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisified, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB/WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
15. When using the write-per-bit capability, $\overline{WB/WE}$ must be low as $\overline{RAS}$ falls.
16. The data bits to which the write operation is applied can be specified by keeping W1/IO1 high with setup and hold time referenced to $\overline{RAS}$ negative transition.

Timing Waveforms

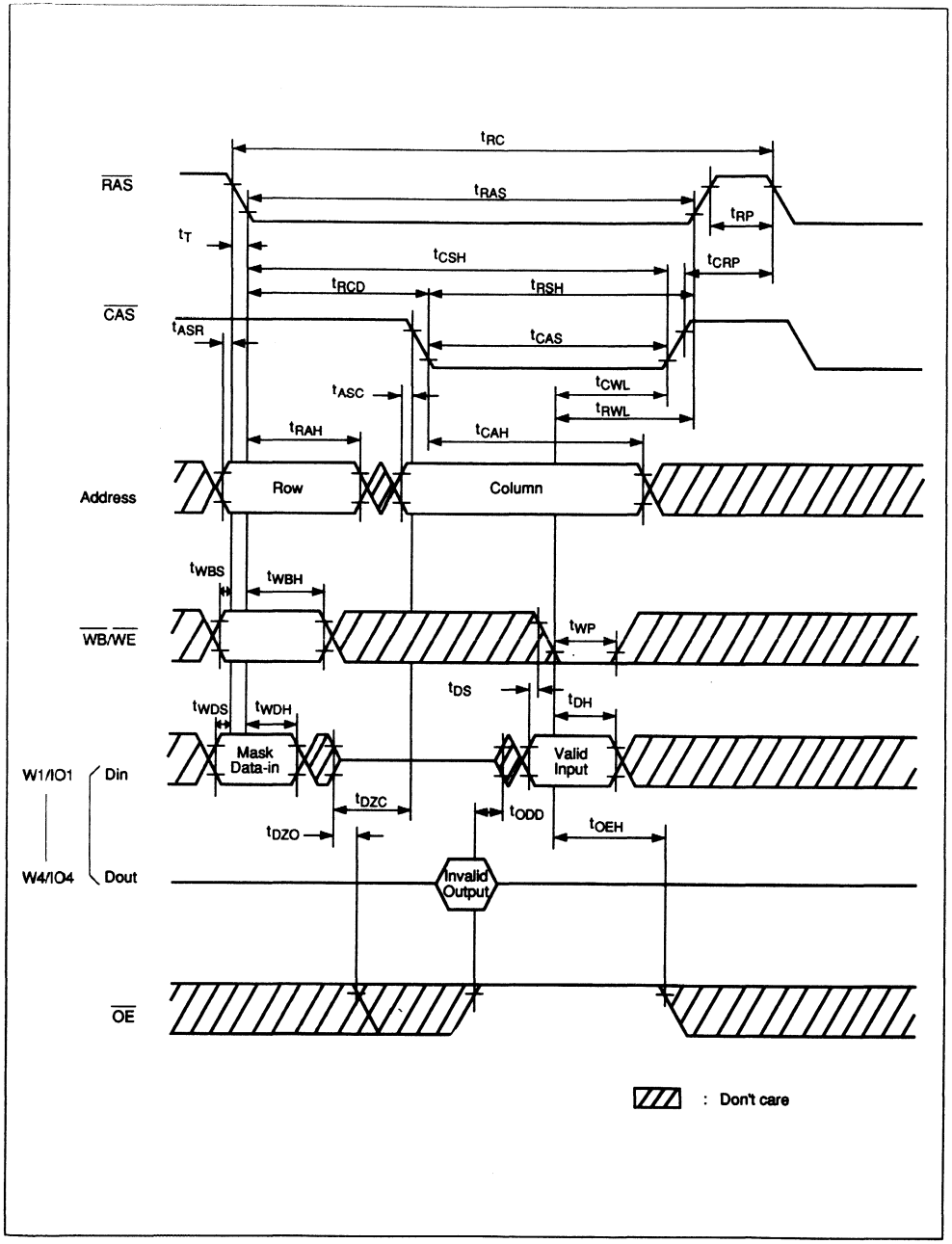
Read Cycle



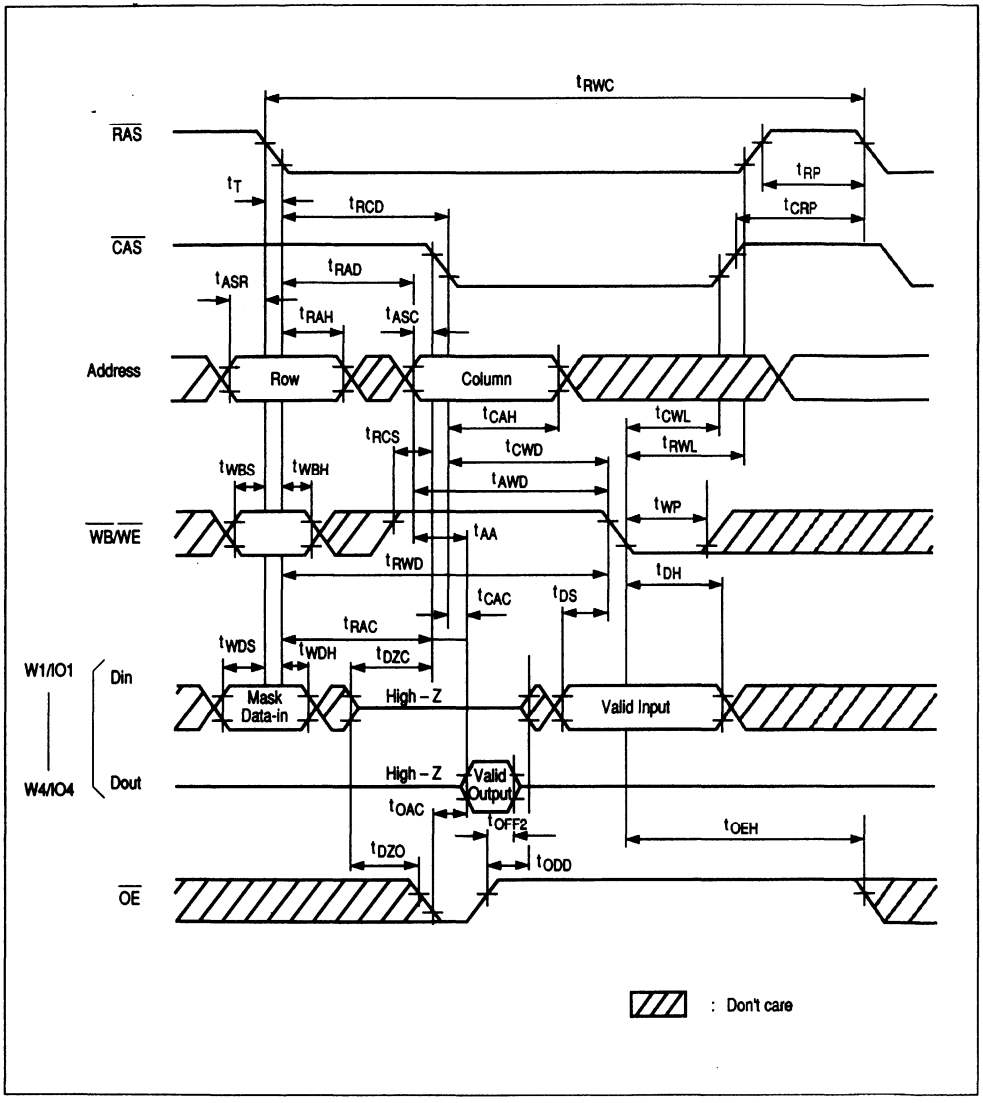
Early Write Cycle



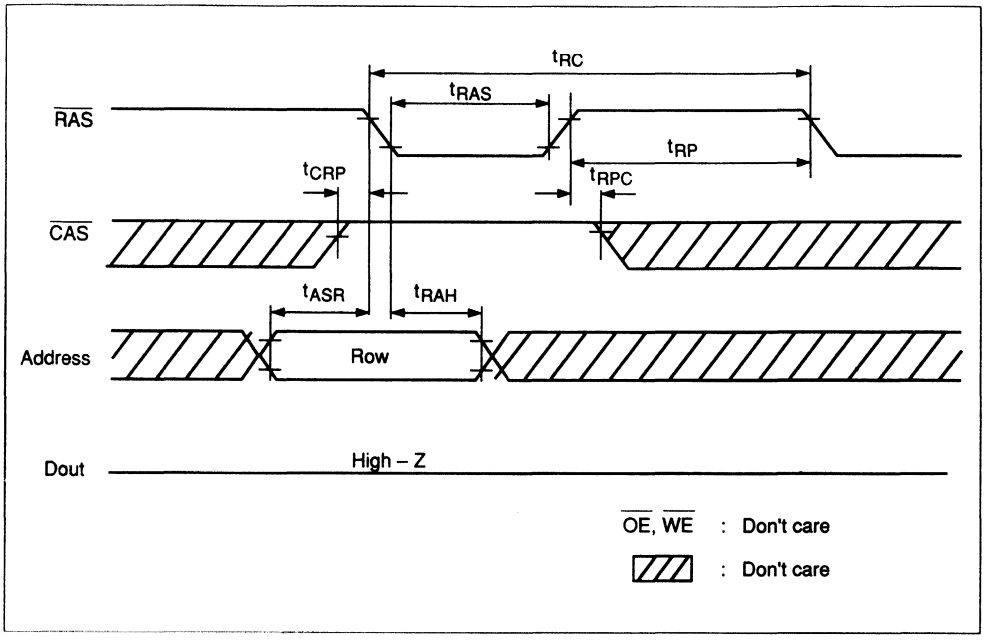
Delayed Write Cycle



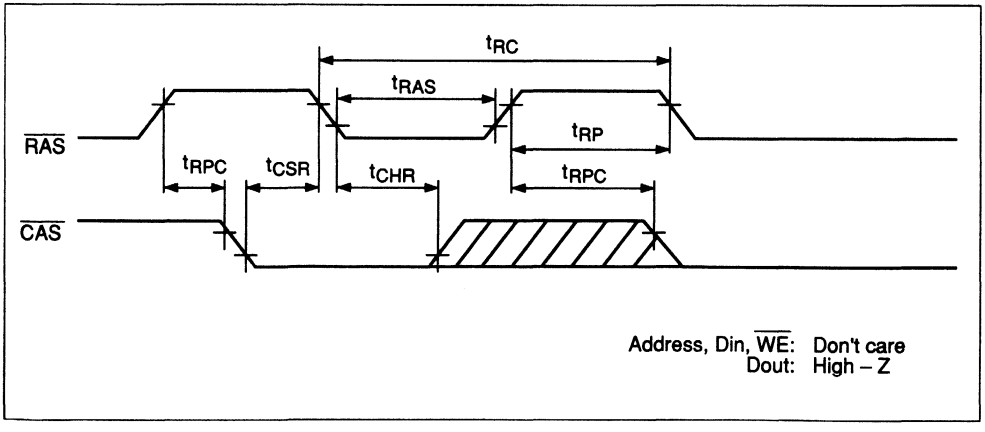
Read-Modify-Write Cycle



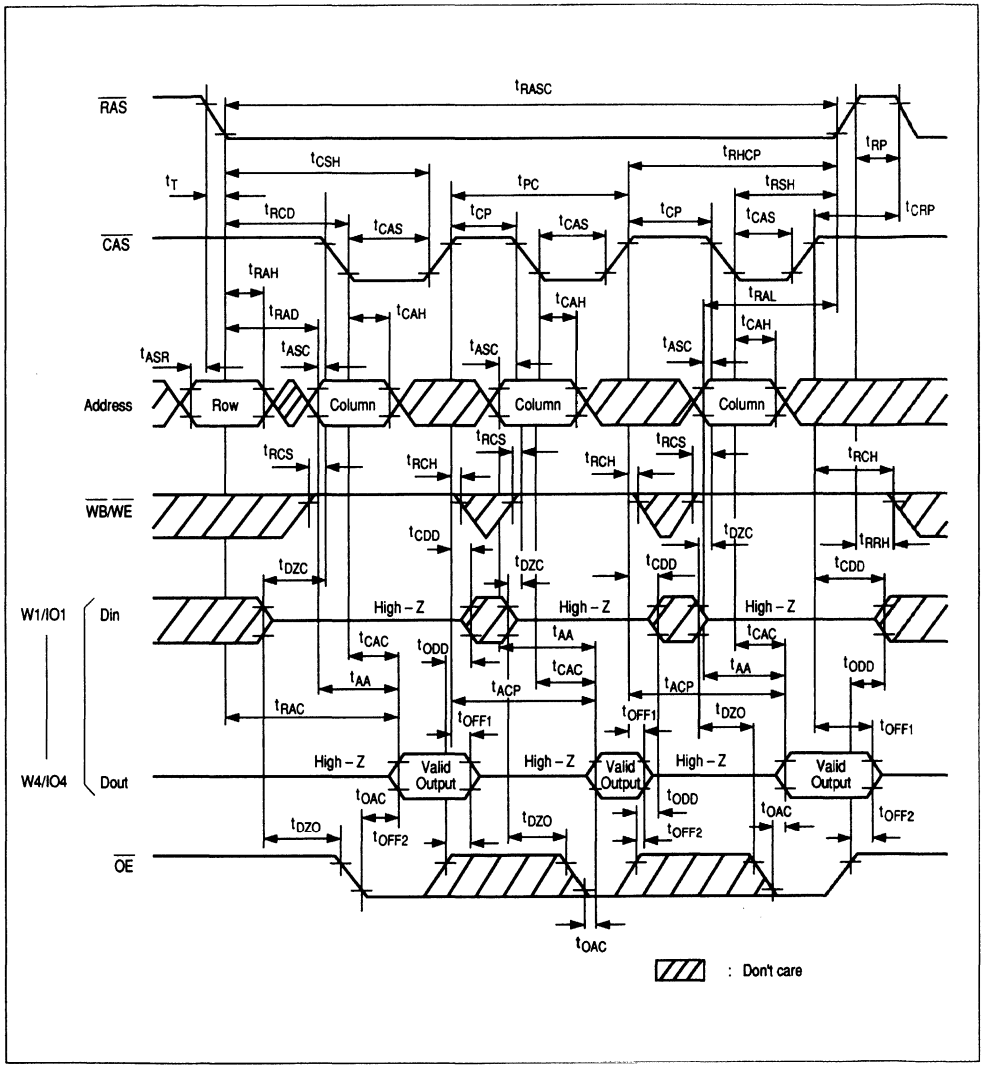
$\overline{RAS}$-Only Refresh Cycle



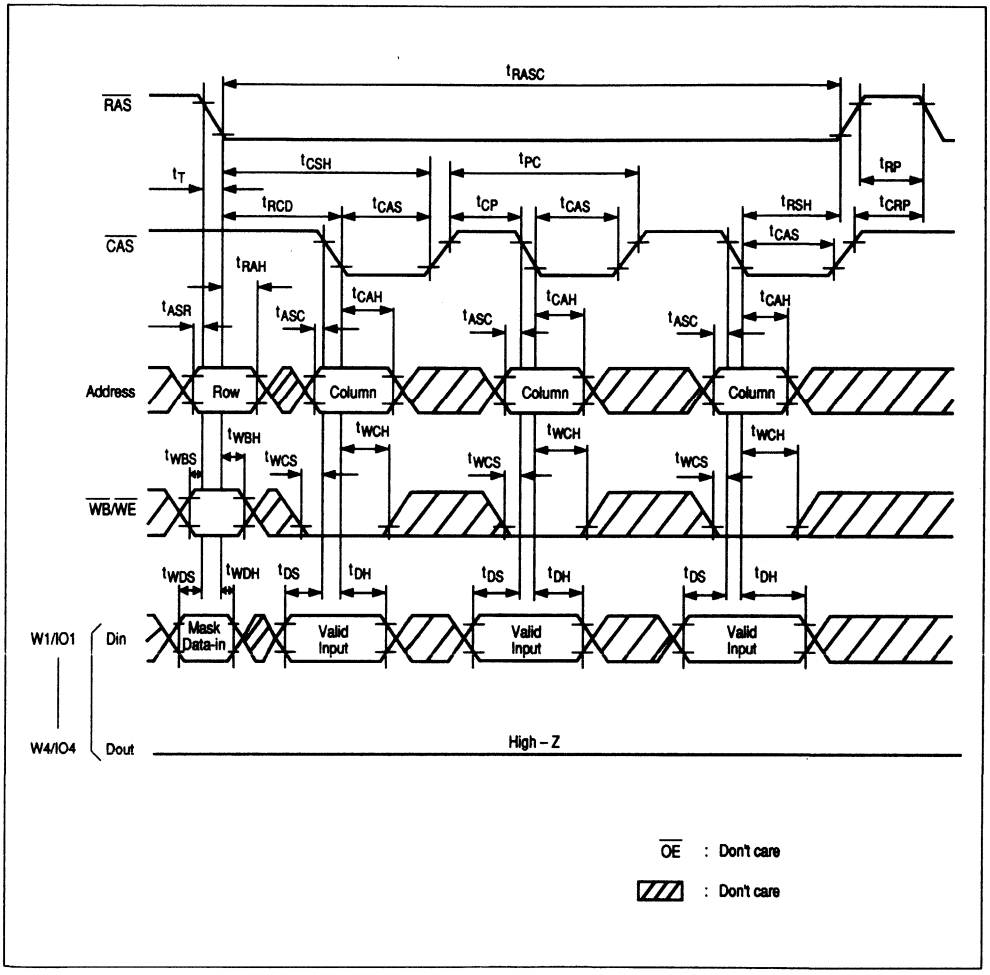
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



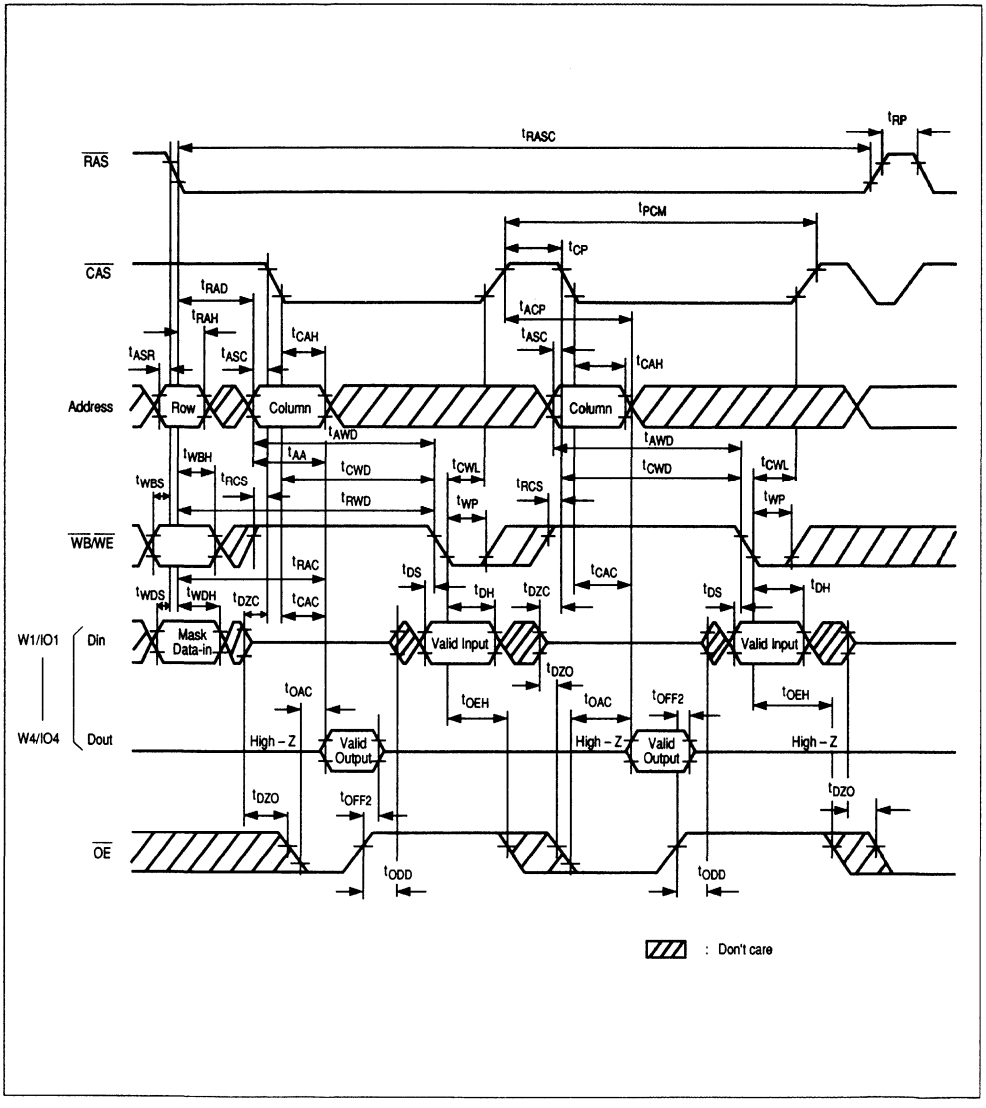
Fast Page Mode Read Cycle



Fast Page Mode Early Write Cycle



Fast Page Mode Read Modify-Write Cycle



HM511000A Series
HM511000AL Series

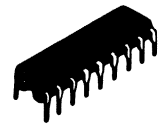
1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511000A/AL series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511000A/AL has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies.

The HM511000A/AL offers Fast Page Mode as a high speed access mode.

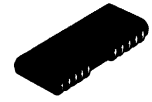
Multiplexed address input permits the HM511000A/AL to be packaged in standard 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511000A/ALP Series



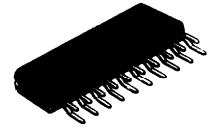
(DP-18C)

HM511000A/ALJP Series



(CP-20D)

HM511000A/ALZP Series



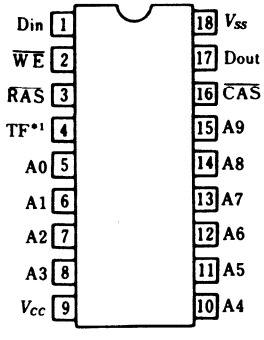
(ZP-20)

Features

- High speed; Access time 60/70/80/100/120 ns (max)
- Low power; 11 mW standby, 495/440/385/330/275 mW active
- Single 5V supply (±10%)
- Fast page mode capability
- 512 refresh cycle; (8ms)
- 2 variations of refresh; $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

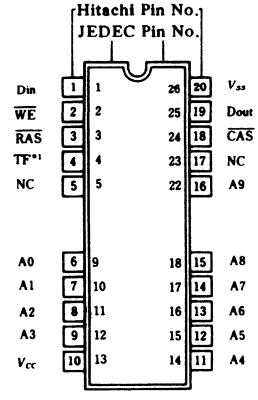
Pin Arrangement

HM511000A/ALP Series



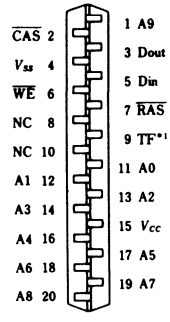
(Top View)

HM511000A/ALJP Series



(Top View)

HM511000A/ALZP Series



(Bottom View)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write input
TF*1	Test function
V_{CC}	Power (+5V)
V_{SS}	Ground

Note)

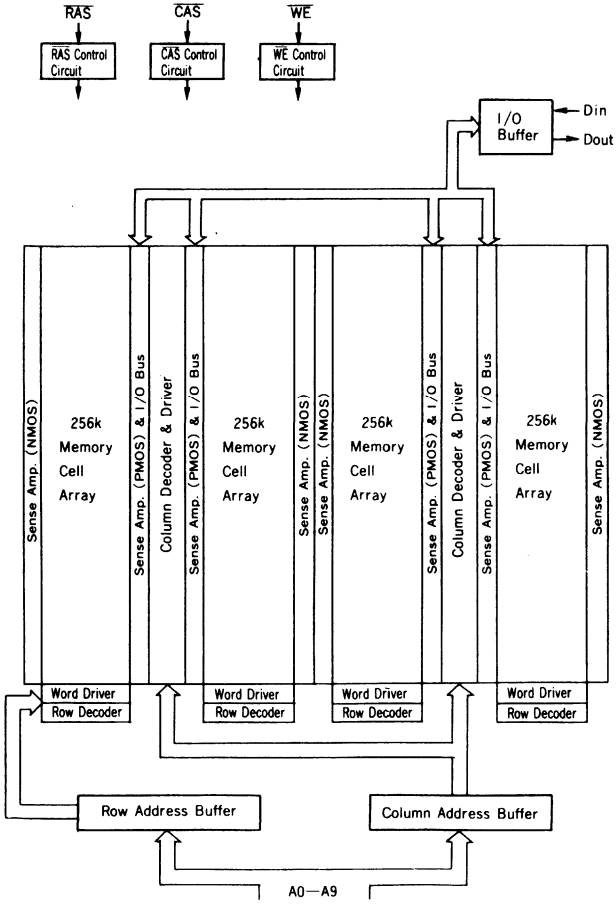
***1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.**

Ordering Information

Type No.	Access Time	Package
HM511000AP-6	60ns	300 mil 18-pin Plastic DIP
HM511000AP-7	70ns	
HM511000AP-8	80ns	
HM511000AP-10	100ns	
HM511000AP-12	120ns	
HM511000AJP-6	60ns	300 mil 20-pin Plastic SOJ
HM511000AJP-7	70ns	
HM511000AJP-8	80ns	
HM511000AJP-10	100ns	
HM511000AJP-12	120ns	
HM511000AZP-6	60ns	400 mil 20-pin Plastic ZIP
HM511000AZP-7	70ns	
HM511000AZP-8	80ns	
HM511000AZP-10	100ns	
HM511000AZP-12	120ns	

Type No.	Access Time	Package
HM511000ALP-6	60ns	300 mil 18- pin Plastic DIP
HM511000ALP-7	70ns	
HM511000ALP-8	80ns	
HM511000ALP-10	100ns	
HM511000ALP-12	120ns	
HM511000ALJP-6	60ns	300 mil 20-pin Plastic SOJ
HM511000ALJP-7	70ns	
HM511000ALJP-8	80ns	
HM511000ALJP-10	100ns	
HM511000ALJP-12	120ns	
HM511000ALZP-6	60ns	400 mil 20-pin Plastic ZIP
HM511000ALZP-7	70ns	
HM511000ALZP-8	80ns	
HM511000ALZP-10	100ns	
HM511000ALZP-12	120ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000 A-8		HM51100 A-10		HM51100 A-12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$,$\overline{CAS}$ cycling, t_{RC}=Min	*1,*2
		—	2	—	2	—	2	—	2	—	2	mA	$\overline{RAS}$,$\overline{CAS}$ =V_{IH} Dout =High-Z	TTL interface
Standby current	I_{CC2}	—	1	—	1	—	1	—	1	—	1	mA	$\overline{RAS}$,$\overline{CAS}$ ≥V_{CC} -0.2V Dout =High-Z	CMOS interface
		—	300	—	300	—	300	—	300	—	300	µA		CMOS interface L-version
Refresh current	I_{CC3}	—	90	—	80	—	60	—	50	—	45	mA	$\overline{RAS}$-only refresh, t_{RC}=Min	*2
Battery back up current (only for L-version)	I_{CC4}	—	300	—	300	—	300	—	300	—	300	µA	t_{RC}=125µs, $\overline{CAS}$ before $\overline{RAS}$ cycling	*4
Standby current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ =V_{IH},$\overline{CAS}$ =V_{IL}, Dout =enable	*1
Refresh current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	$\overline{CAS}$-before-$\overline{RAS}$ refresh, t_{RC} = Min	
Fast page mode current	I_{CC7}	—	80	—	70	—	50	—	50	—	40	mA	$\overline{RAS}$ =V_{IL},$\overline{CAS}$ cycling,t_{PC} = Min	*1,*3
Input leakage	I_{LI}	-10	10	-10	10	-10	10	-10	10	-10	10	µA	V_{IN} =0 to +7V	
Output leakage	I_{LO}	-10	10	-10	10	-10	10	-10	10	-10	10	µA	V_{OUT} =0 to +7V, D_{OUT} =disable	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OUT} =-5mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{OUT} =4.2mA	

Notes: *1. Icc depends on output loading condition when the device is selected.
Icc max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = VIL.
*3. Address can be changed once or less while $\overline{CAS}$ = VIH.
*4. t_{RAS}=t_{RAS}(min) to 1µs
Input voltage: All pins: $V_{IH} \geq V_{CC}$–0.2V or $V_{IL} \leq$ 0.2V.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{SS} = 0V, V_{CC} = 5V ± 10%)

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2 TTL Gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511000A /AL-6		HM511000A /AL-7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	*9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	*7
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	
Refresh period (only for L-version)	t_{REF}	—	64	—	64	—	64	—	64	—	64	ms	

Read Cycle

Parameter	Symbol	HM511000A /AL -6		HM511000A /AL -7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	*2,*3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	*3,*4
Access time from address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	*3,*5
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	*6

Write Cycle

Parameter	Symbol	HM511000A /AL -6		HM511000A /AL -7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	*10
Write command hold time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	*11
Data -in hold time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	*11

Read-Modify-Write Cycle

Parameter	Symbol	HM511000A /AL -6		HM511000A /AL -7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	145	—	155	—	190	—	220	—	255	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	60	—	70	—	80	—	100	—	120	—	ns	*10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20	—	20	—	25	—	25	—	30	—	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	30	—	35	—	40	—	45	—	55	—	ns	*10

Refresh Cycle

Parameter	Symbol	HM511000A /AL -6		HM511000A /AL -7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM511000A /AL -6		HM511000A /AL -7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	_	10	—	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	*13
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	*14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511000A /AL -6		HM511000A /AL -7		HM511000A /AL-8		HM511000A /AL-10		HM511000A /AL-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Fast page mode read-write cycle time	t_{PCM}	70	—	75	—	85	—	85	—	100	—	ns	

Notes) *1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).

*5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).

*6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*7. Transition times are measured between V_{IH} and V_{IL}.

*8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

*10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

*11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

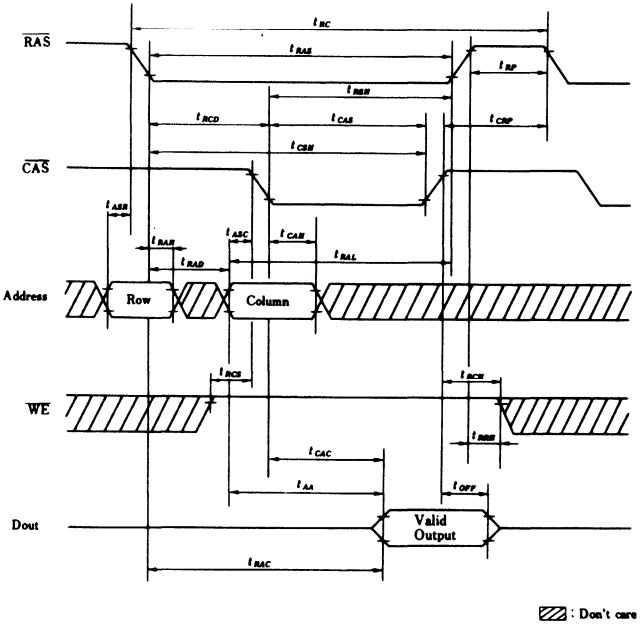
*12. An initial pause of 100μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

*13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycle.

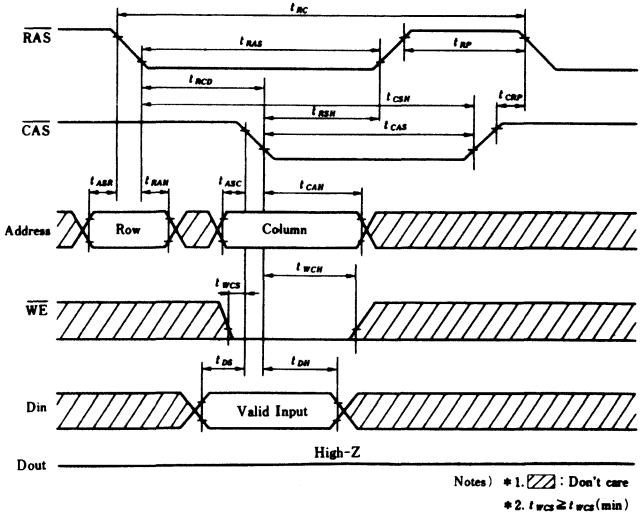
*14. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{ACP}.

Timing Waveforms

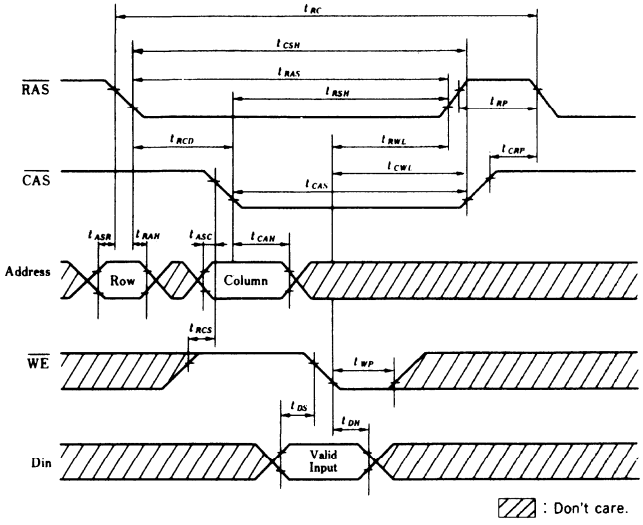
Read Cycle



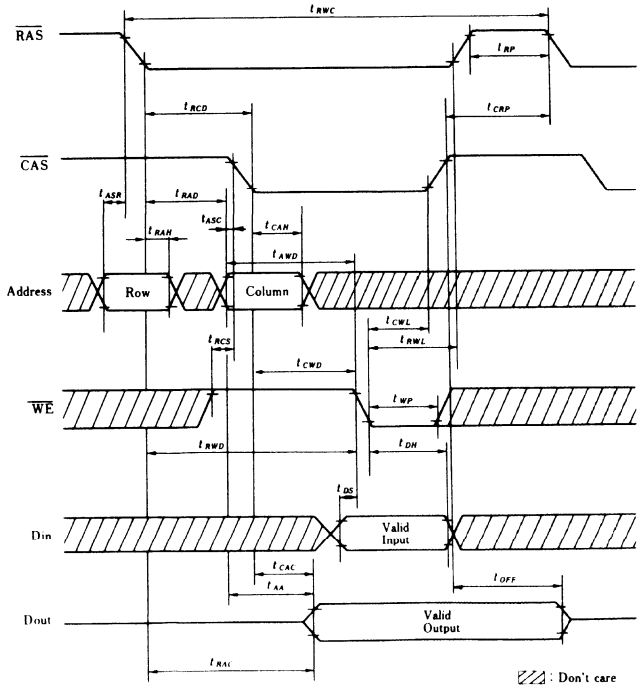
Early Write Cycle



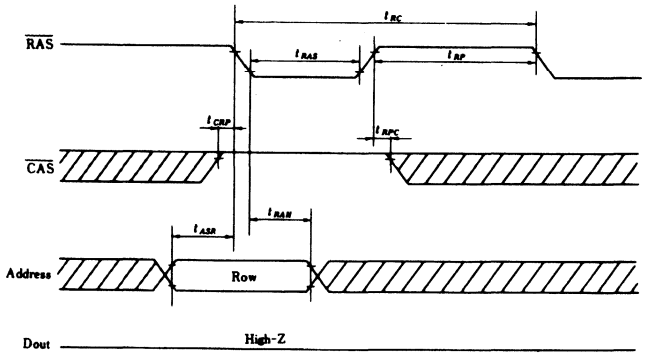
Delayed Write Cycle



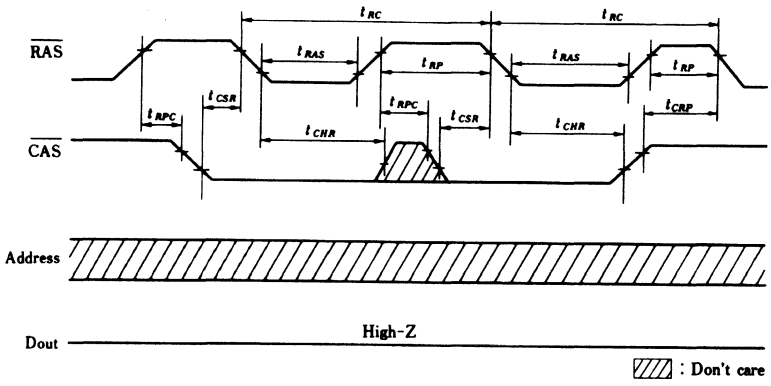
Read-Modify-Write Cycle



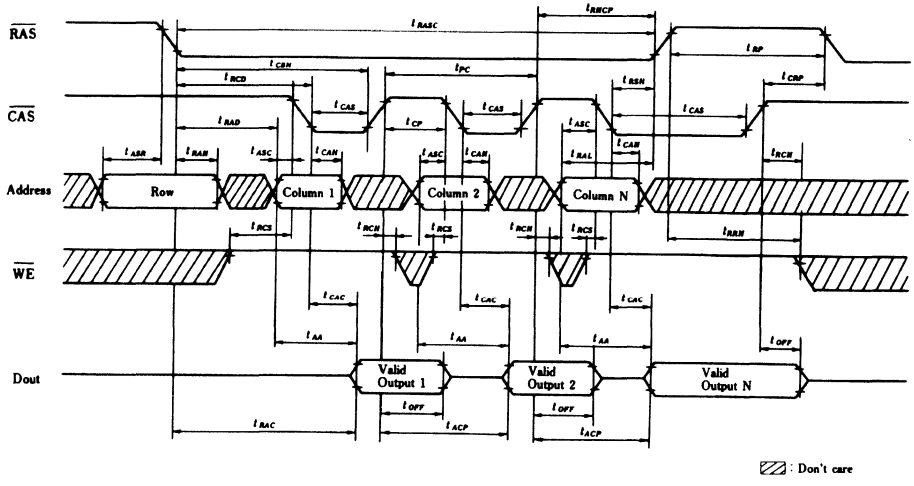
RAS-Only Refresh Cycle



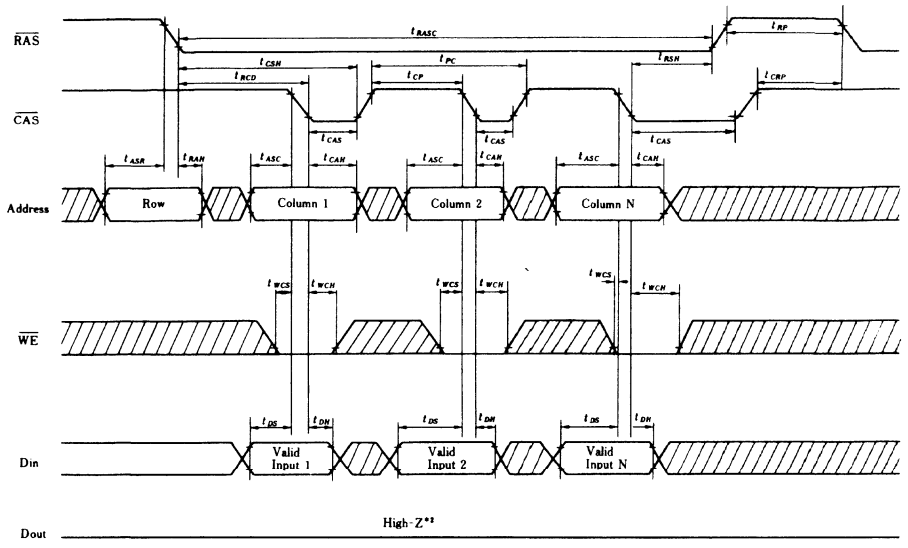
CAS-Before-RAS Refresh Cycle



Fast Page Mode Read Cycle

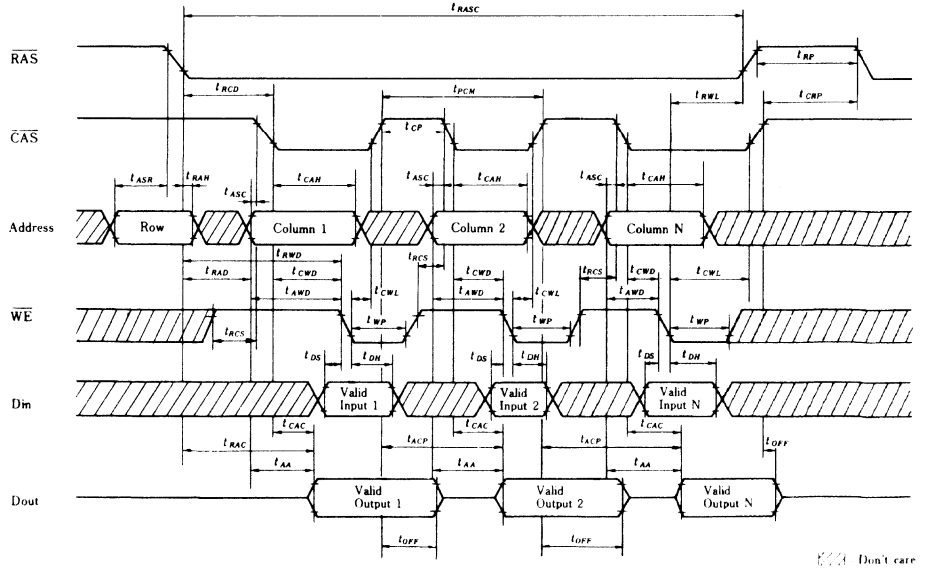


Fast Page Mode Write Cycle



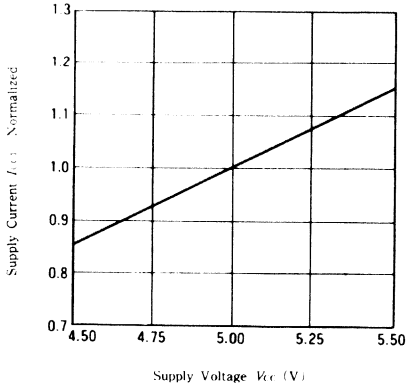
Notes) *1. ▨ : Don't care
*2. $t_{WCS} \geq t_{WCS}$ (min)

Fast Page Mode Read Modify Write Cycle

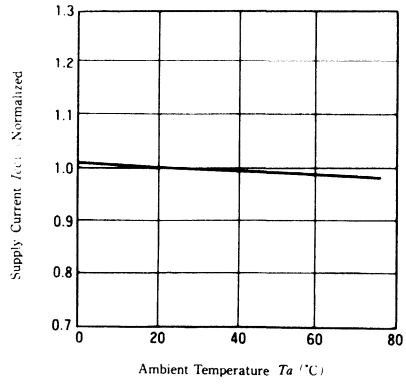


▨ : Don't care

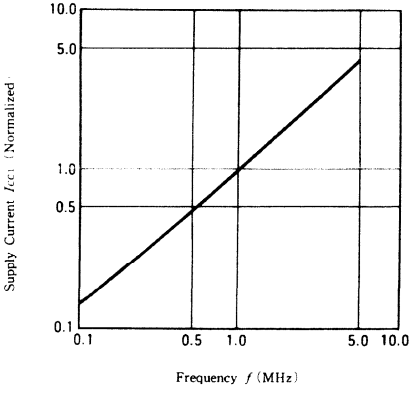
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



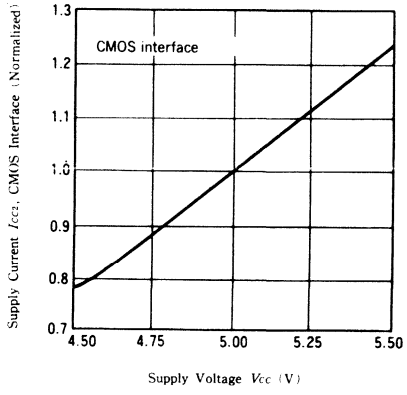
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



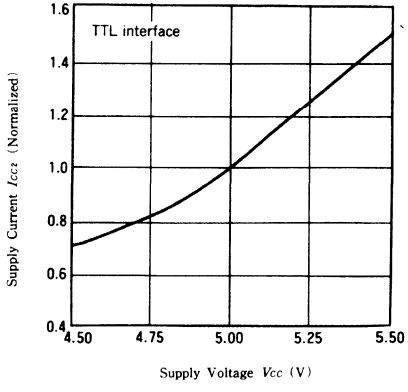
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



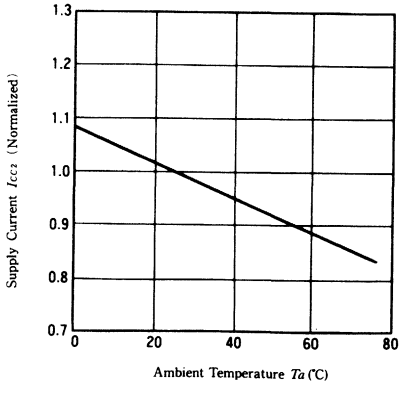
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



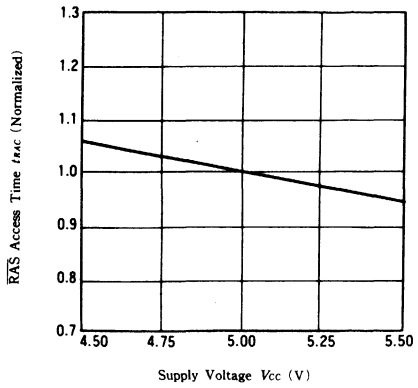
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



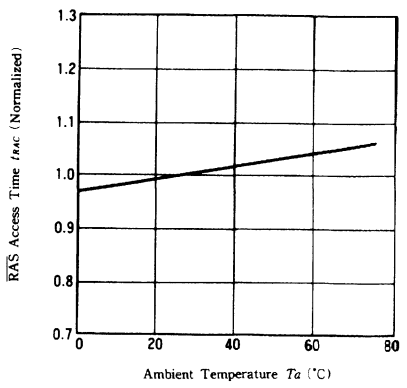
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



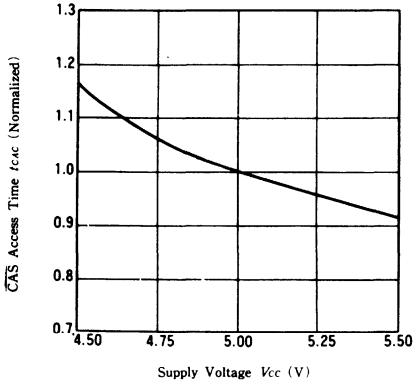
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



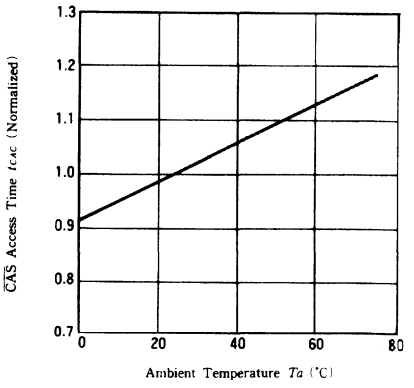
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



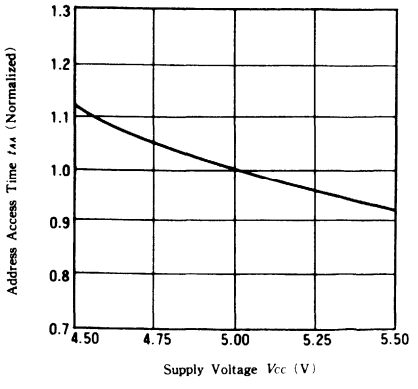
$\overline{CAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



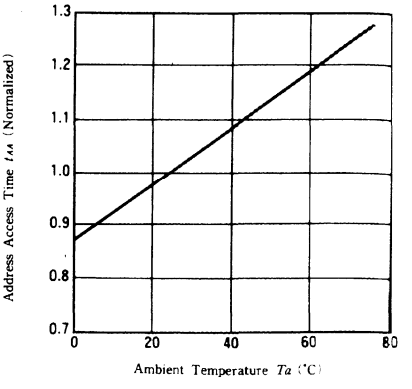
$\overline{CAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM511000H Series

1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511000H series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511000H has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511000H offers Fast Page Mode as a high speed access mode.

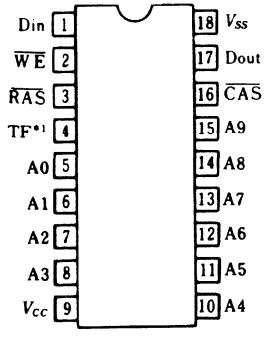
Multiplexed address input permits the HM511000H to be packaged in standard 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

Features

- High speed; Access time 60ns/70ns (max)
- Low power; 11 mW standby, 495mW/440mW active
- Single 5V supply (±10%)
- Fast page mode capability
- 512 refresh cycle; (8 ms)
- 2 variations of refresh; $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

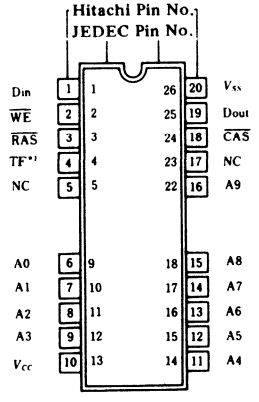
Pin Arrangement

- **HM511000HP Series**



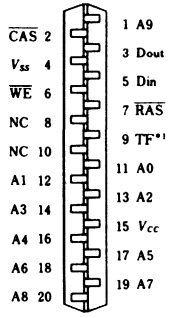
(Top View)

- **HM511000HJP Series**



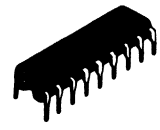
(Top View)

- **HM511000HZP Series**



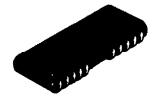
(Bottom View)

HM511000HP Series



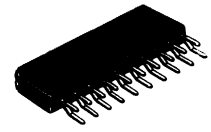
(DP-18C)

HM511000HZP Series



(CP-20D)

HM511000HJP Series



(ZP-20)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/Write input
TF*1	Test function
V_{CC}	Power (+5V)
V_{SS}	Ground

Note: 1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} +0.5V.

Ordering Information

Type No.	Access Time	Package
HM511000HP-6	60ns	300-mil 18-pin Plastic DIP
HM511000HP-7	70ns	
HM511000HJP-6	60ns	300-mil 20-pin Plastic SOJ
HM511000HJP-7	70ns	
HM511000HZP-6	60ns	400-mil 20-pin Plastic ZIP
HM511000HZP-7	70ns	

HM511001A Series

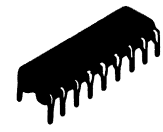
1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511001A series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511001A has realized higher density, higher performance and various functions by employing 1.3 μm CMOS process technology and some new CMOS circuit design technologies.

The HM511001A offers Nibble Mode as a high speed access mode.

Multiplexed address input permits the HM511001A to be packaged in standard, 18-pin plastic DIP, 20-pin plastic ZIP and 20-pin plastic SOJ.

HM511001AP Series

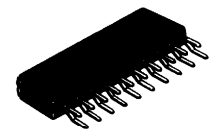


(DP-18C)

HM511001AJP Series

(CP-20D)

HM511001AZP Series



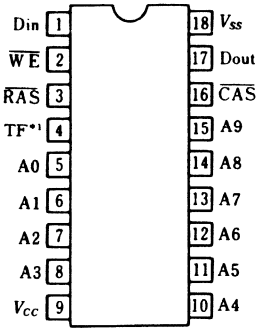
(ZP-20)

Features

- High speed; Access time 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power; 11 mW standby, 495 mW/440 mw/385 mW/330 mW/275 mW active
- Single 5V supply (±10%)
- Nibble mode capability
- 512 refresh cycle; (8 ms)
- 2 variations of refresh; $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh

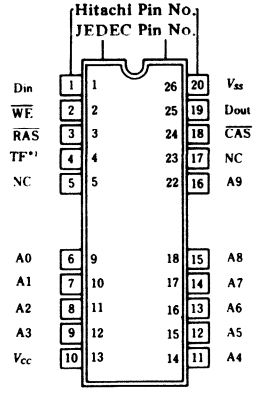
Pin Arrangement

- **HM511001AP Series**



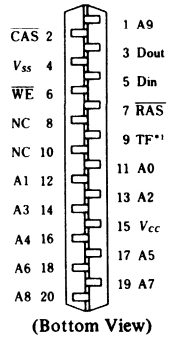
(Top View)

- **HM511001AJP Series**



(Top View)

- **HM511001AZP Series**



(Bottom View)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
A9	Nibble address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Row address input
$\overline{WE}$	Read/Write input
TF*1	Test function
V_{CC}	Power (+5V)
V_{SS}	Ground

Note: 1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

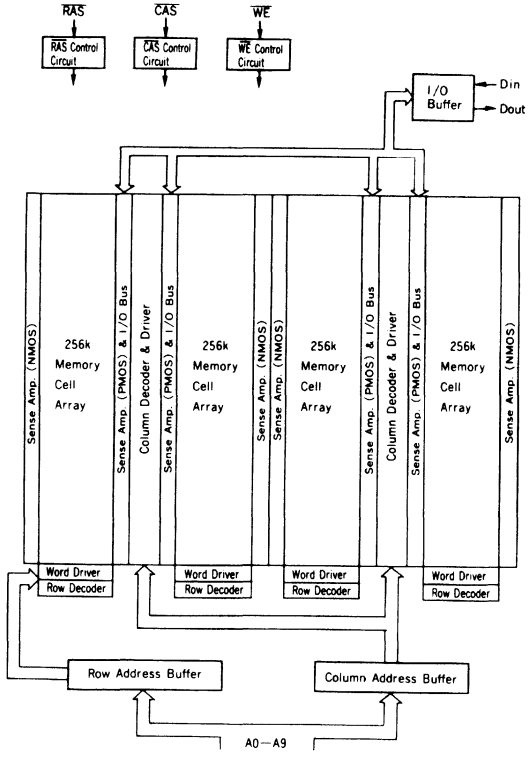
HM511001A Series

Ordering Information

Type No.	Access Time	Package
HM511001AP-6	60 ns	300-mil 18-pin Plastic Dip
HM511001AP-7	70 ns	
HM511001AP-8	80 ns	
HM511001AP-10	100 ns	
HM511001AP-12	120 ns	
HM511001AJP-6	60 ns	300-mil 20-pin Plastic SOJ
HM511001AJP-7	70 ns	
HM511001AJP-8	80 ns	
HM511001AJP-10	100 ns	
HM511001AJP-12	120 ns	

Type No.	Access Time	Package
HM511001AZP-6	60 ns	400-mil 20-pin Plastic ZIP
HM511001AZP-7	70 ns	
HM511001AZP-8	80 ns	
HM511001AZP-10	100 ns	
HM511001AZP-12	120 ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	*Iout*	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	*Topr*	0 to +70	°C
Storage temperature	*Tstg*	-55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	−2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511001A-6 Min	HM511001A-6 Max	HM511001A-7 Min	HM511001A-7 Max	HM511001A-8 Min	HM511001A-8 Max	HM511001A-10 Min	HM511001A-10 Max	HM511001A-12 Min	HM511001A-12 Max	Unit	Test condition	Note
Operating current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = Min	*1, *2
Standby current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	$\overline{RAS}$,$\overline{CAS}$=V_{IH} TTL interface Dout = High-Z	
		—	1	—	1	—	1	—	1	—	1		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC}-0.2V CMOS interface Dout = High-Z	
Refresh current	I_{CC3}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$-only refresh, t_{RC} = Min	*2
Standby current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, Dout = enable	*1
Refresh current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	$\overline{CAS}$-before-$\overline{RAS}$ refresh, t_{RC}=Min.	
Nibble mode current	I_{CC8}	—	70	—	70	—	50	—	50	—	40	mA	$\overline{RAS}$=V_{IL},$\overline{CAS}$ cycling, t_{NC}=Min	*1, *3
Input leakage	I_{LI}	−10	10	−10	10	−10	10	−10	10	−10	10	µA	V_{IN}=0 to +7V	
Output leakage	I_{LO}	−10	10	−10	10	−10	10	−10	10	−10	10	µA	V_{out}=0 to +7V, D_{out} = disabled	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{out} = −5 mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	I_{out} = 4.2 mA	

Notes) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1, *2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)*1, *10

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference lvels: 0.8V, 2.4V
- Output load: 2 TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM511001A -6		HM511001A -7		HM511001A -8		HM511001A -10		HM511001A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	*7
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	*11
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	*6
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM511001A -6		HM511001A -7		HM511001A -8		HM511001A -10		HM511001A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	*2, *3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	*3, *4
Access time from address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	*3, *4
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output buffer turn-off delay	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	*5

Write Cycle

Parameter	Symbol	HM511001A -6		HM511001A -7		HM511001A -8		HM511001A -10		HM511001A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	*8
Write command hold time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	*9
Data-in hold time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	*9

Read-Modify-Write Cycle

Parameter	Symbol	HM511001A -6		HM511001A -7		HM511001A -8		HM511001A -10		HM511001A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	145	—	155	—	190	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	60	—	70	—	80	—	90	—	110	—	ns	*8
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20	—	20	—	25	—	25	—	30	—	ns	*8
Column address to $\overline{WE}$ delay time	t_{AWD}	30	—	35	—	40	—	45	—	55	—	ns	*8

Refresh Cycle

Perameter	Symbol	HM511001A -6		HM511001A -7		HM511001A -8		HM511001A -10		HM511001A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Nibble Mode Cycle

Parameter	Symbol	HM511001A -6		HM511001A -7		HM511001A -8		HM511001A -10		HM511001A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Nibble mode access time	t_{NAC}	—	20	—	20	—	25	—	25	—	30	ns	
Nibble mode cycle time	t_{NC}	40	—	40	—	45	—	45	—	50	—	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10	—	10	—	10	—	10	—	10	—	ns	
Nibble mode $\overline{CAS}$ pulse with	t_{NCA}	20	—	20	—	25	—	25	—	30	—	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	20	—	20	—	25	—	25	—	30	—	ns	

Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM511001A -6		HM511001A -7		HM511001A -8		HM511001A -10		HM511001A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Nibble mode read-modify-write cycle time	t_{NRWC}	65	—	65	—	65	—	65	—	75	—	ns	
Nibble mode write command $\overline{CAS}$ lead time	t_{NCWL}	20	—	20	—	20	—	20	—	25	—	ns	
Nibble mode $\overline{CAS}$ to $\overline{WE}$ delay time	t_{NCWD}	20	—	20	—	20	—	20	—	25	—	ns	

Notes)

*1. AC measurements assume t_T = 5ns.

*2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.

*3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

*4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max).

*5. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

*6. Transition times are measured between V_{IH} and V_{IL}.

*7. Operation with the t_{RCD} (max) limit insures that tRAC (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

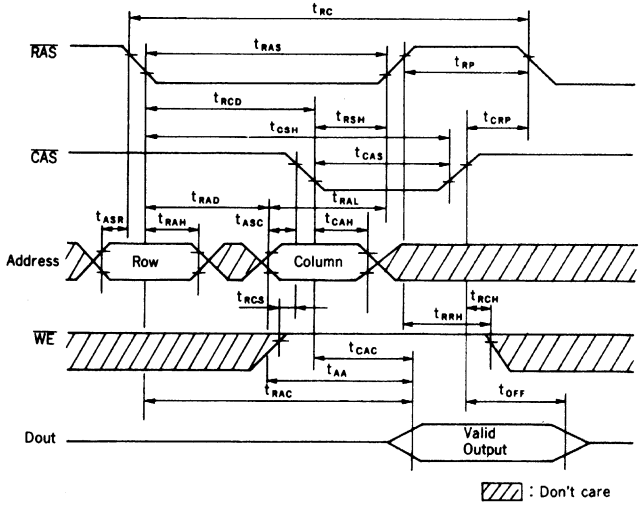
*9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

*10. An initial pause of 100μs is required after power-up followed by eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

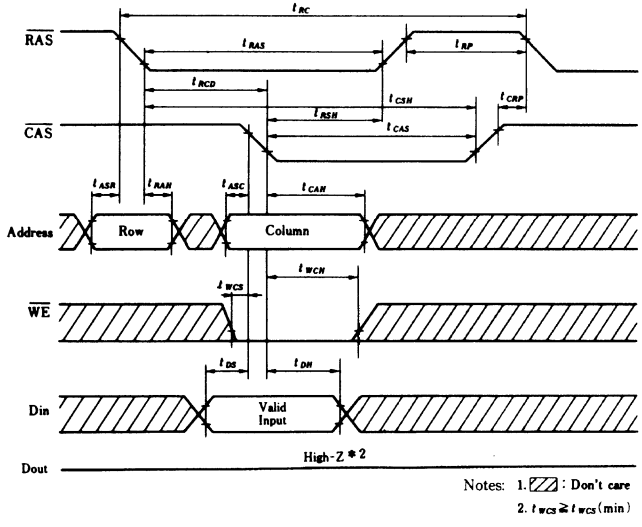
*11. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

Timing Waveforms

Read Cycle

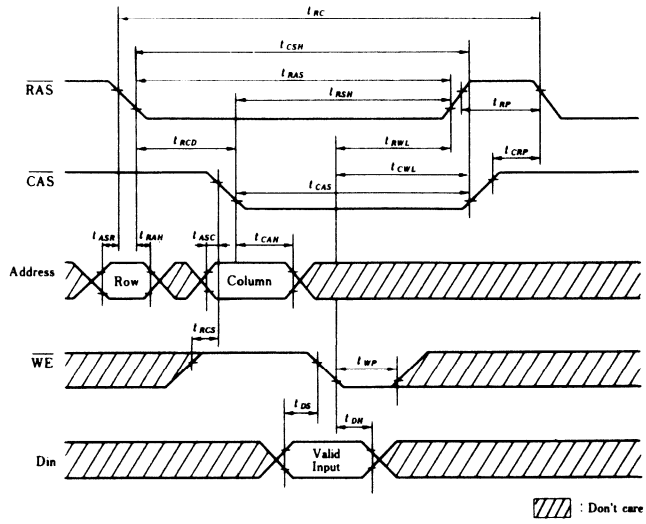


Early Write Cycle

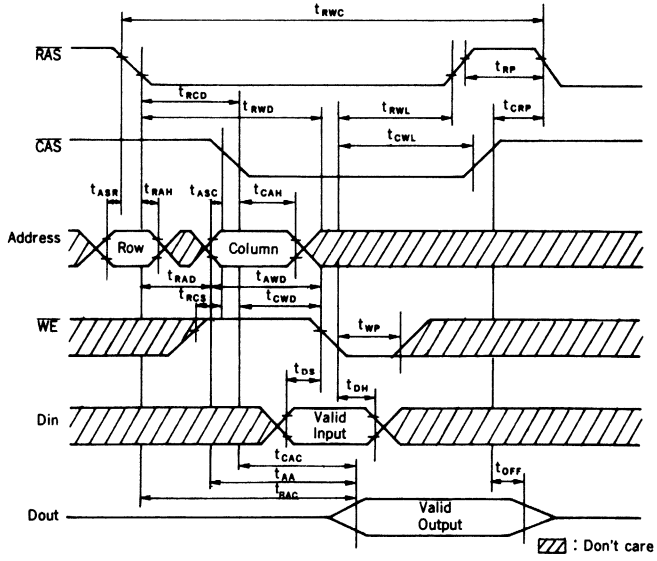


Notes: 1. ▨ : Don't care
2. $t_{WCS} \geq t_{WCS}$ (min)

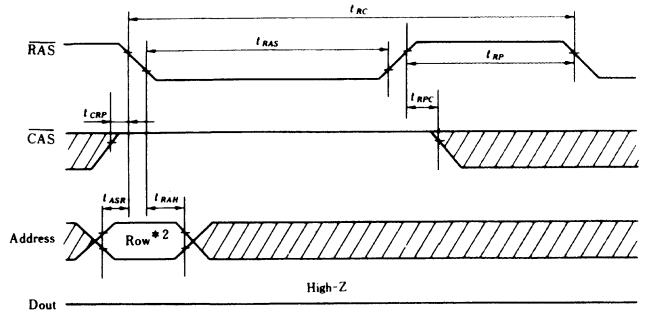
Delayed Write Cycle



Read-Modify-Write Cycle

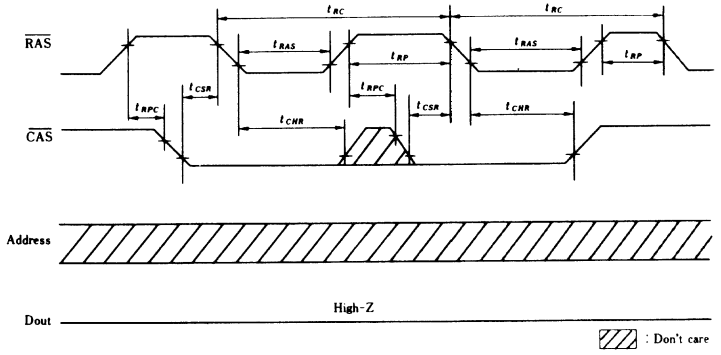


RAS-Only Refresh Cycle

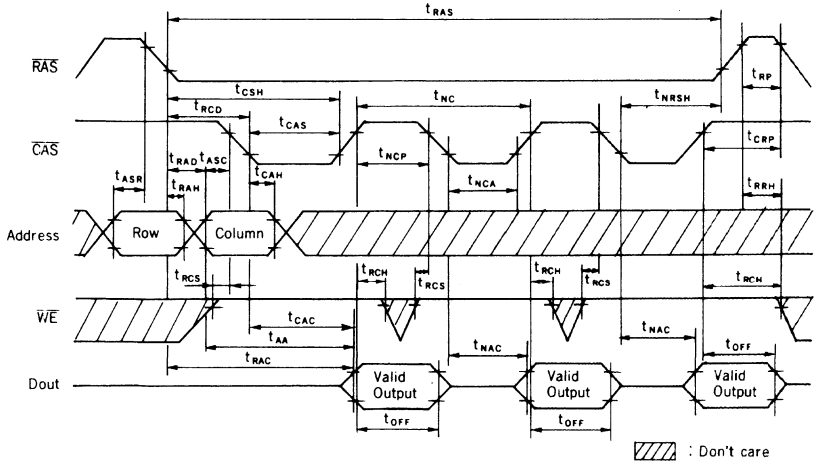


Notes: 1. ▨: Don't care
2. Refresh address A0-A8(AX0-AX8)

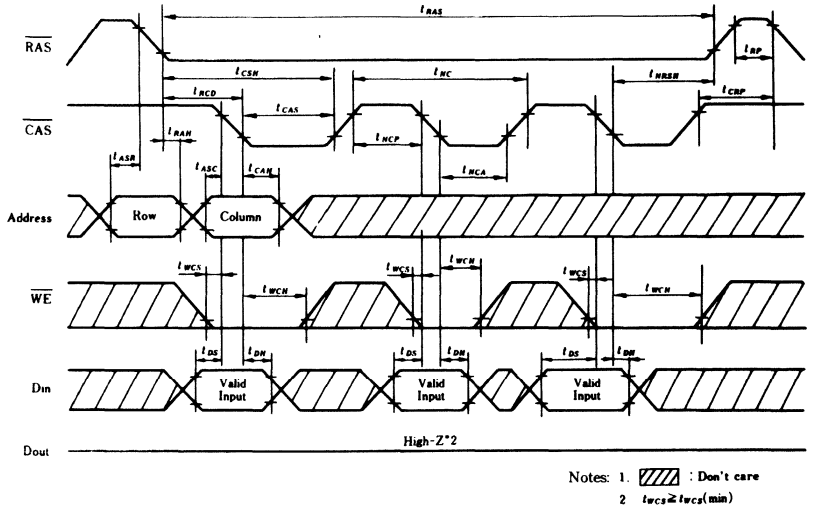
CAS-Before-RAS Refresh Cycle



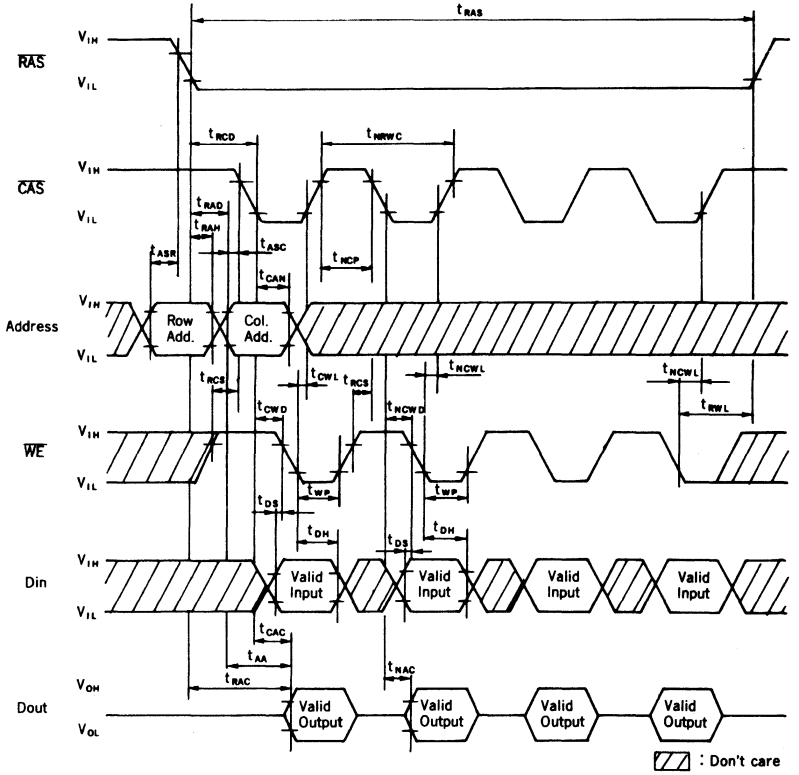
Nibble Mode Read Cycle



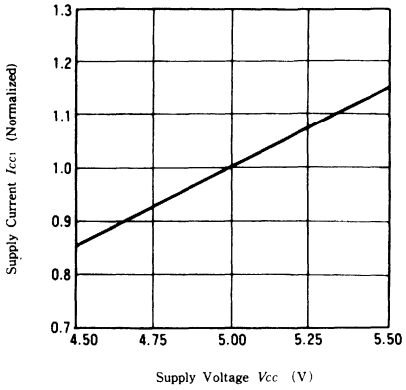
Nibble Mode Write Cycle



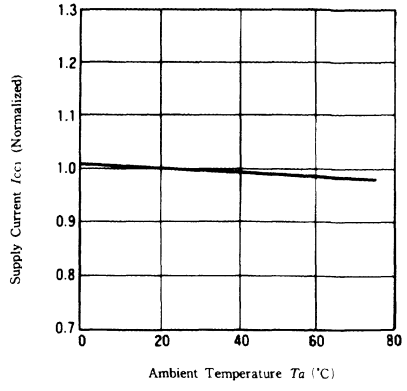
Nibble Mode Read-Modify-Write Cycle



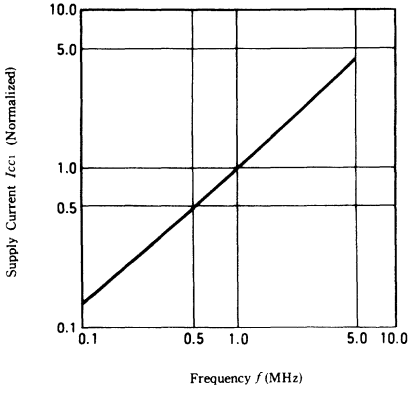
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



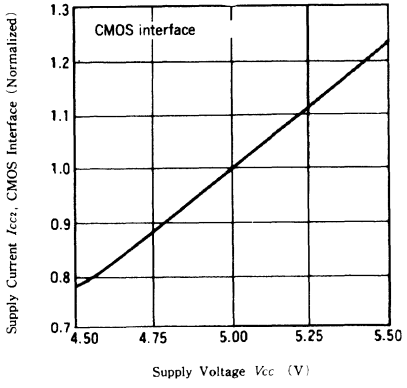
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



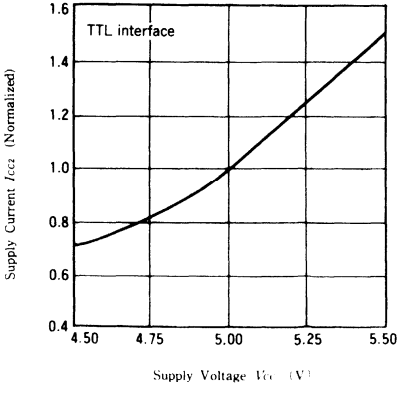
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



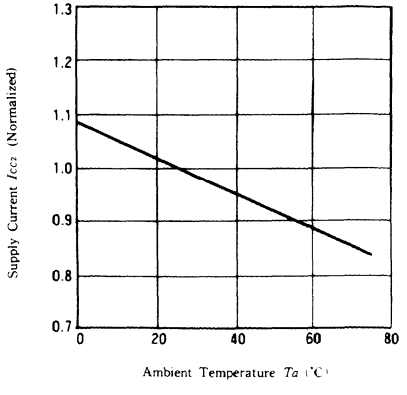
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



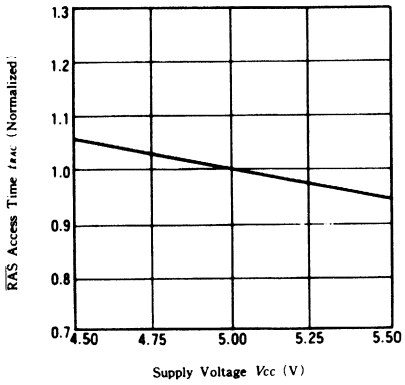
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



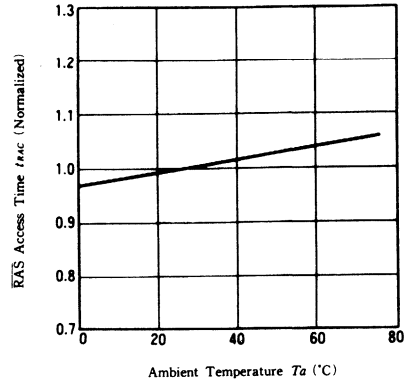
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



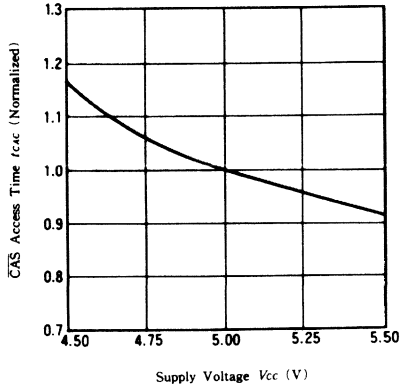
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



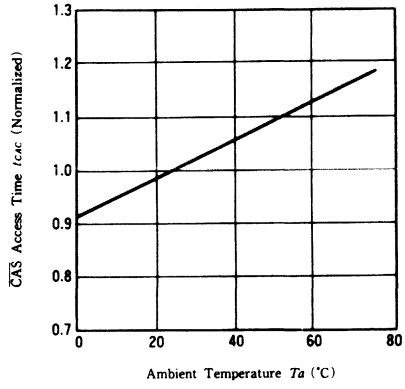
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



$\overline{CAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



$\overline{CAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



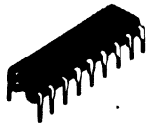
HM511002A Series

1048576-word x 1-bit CMOS Dynamic RAM

The Hitachi HM511002A Series is a CMOS dynamic RAM organized 1048576-word x 1-bit. HM511002A has realized higher density, higher performance and various functions by employing 1.3μm CMOS process technology and some new CMOS circuit design technologies. The HM511002A offers Static Column Mode as a high speed access mode.

Multiplexed address input permits the HM511002A to be packaged in standard 18-pin plastic DIP, 20-pin plastic SOJ and 20-pin plastic ZIP.

HM511002AP Series

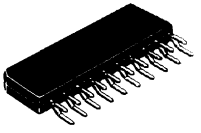


(DP-18C)

HM511002AJP Series

(CP-20D)

HM511002AZP Series



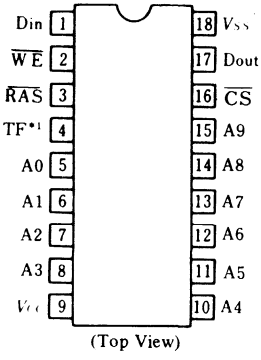
(ZP-20)

Features

- High speed; Access time 60/70/80/100/120 ns (max)
- Low power; 11 mW Standby, 495/440/385/330/275 mW Active
- Single 5V supply (±10%)
- Static column mode capability
- 512 refresh cycles; (8 ms)
- 2 variations of refresh; $\overline{RAS}$ only refresh
  $\overline{CS}$-before-$\overline{RAS}$ refresh

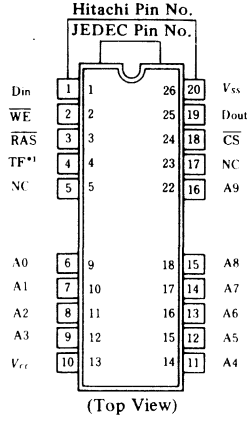
Pin Arrangement

• **HM511002AP Series**



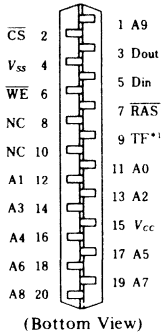
(Top View)

• **HM511002AJP Series**



(Top View)

• **HM511002AZP Series**



(Bottom View)

Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
Din	Data input
Dout	Data output
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Power (+5V)
V_{SS}	Ground
TF*1	Test function

Note)

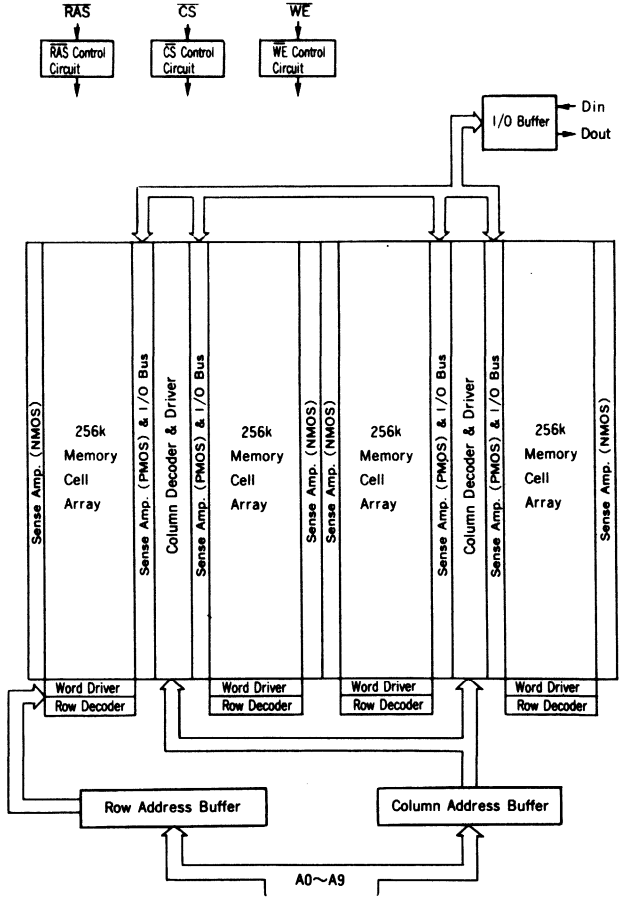
***1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.**

Ordering Information

Type No.	Access Time	Package
HM511002AP-6	60 ns	300 mil 18-pin Plastic DIP
HM511002AP-7	70 ns	
HM511002AP-8	80 ns	
HM511002AP-10	100 ns	
HM511002AP-12	120 ns	
HM511002AJP-6	60 ns	300 mil 20-pin Plastic SOJ
HM511002AJP-7	70 ns	
HM511002AJP-8	80 ns	
HM511002AJP-10	100 ns	
HM511002AJP-12	120 ns	

Type No.	Access Time	Package
HM511002AZP-6	60 ns	400 mil 20-pin Plastic ZIP
HM511002AZP-7	70 ns	
HM511002AZP-8	80 ns	
HM511002AZP-10	100 ns	
HM511002AZP-12	120 ns	

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	–	6.5	V
Input low voltage	V_{IL}	-2.0	–	0.8	V

Note) All voltages referenced to V_{SS}.

DC Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0 to +70°C)

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Test Conditions	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	90	—	80	—	70	—	60	—	50	mA	$\overline{RAS}$,$\overline{CS}$ cycling, t_{RC}=Min	*1,*2
Standby current	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	$\overline{RAS}$,$\overline{CS}$ =V_{IH} Dout =High-Z	TTL interface
		—	1	—	1	—	1	—	1	—	1		$\overline{RAS}$,$\overline{CS}$ ≧ V_{CC} -0.2V Dout =High-Z	CMOS interface
Refresh current	I_{CC3}	—	90	—	80	—	60	—	50	—	45	mA	$\overline{RAS}$-only refresh, t_{RC}=Min	*2
Standby current	I_{CC5}	—	5	—	5	—	5	—	5	—	5	mA	$\overline{RAS}$ =V_{IH},$\overline{CS}$ =V_{IL}, Dout =enable	*1
Refresh current	I_{CC6}	—	80	—	70	—	60	—	50	—	40	mA	$\overline{CS}$-before-$\overline{RAS}$ refresh, t_{RC} =Min	
Static column mode current	I_{CC9}	—	80	—	70	—	60	—	50	—	40	mA	t_{SC} = Min	*3
Input leakage	I_{LI}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	V_{IN} = 0 to +7 V	
Output leakage	I_{LO}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	V_{OUT} = 0 to +7 V, Dout = disable	
Output levels	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = -5 mA	
	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes) *1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.
*2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
*3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, Data input	C_{I1}	–	5	pF	*1
	Clocks	C_{I2}	–	7	pF	*1
Output capacitance	Data output	C_O	–	7	pF	*1,*2

Notes) *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ±10%, V_{SS} = 0V)[*1,*17]

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8V, 2.4V
- Output load: 2 TTL Gate + C_L (100pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	120	—	130	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	50	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ pulse width	t_{SP}	20	10000	20	10000	25	10000	30	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column address setup time	t_{ASW}	0	—	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{AHW}	15	—	15	—	20	—	25	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	40	20	50	22	55	25	70	25	90	ns	*8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	20	50	20	65	ns	*9
$\overline{RAS}$ hold time	t_{RSL}	20	—	20	—	25	—	30	—	30	—	ns	
$\overline{CS}$ hold time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{SRS}	10	—	10	—	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	*7
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	

Read Cycle

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	*2, *3
Access time from $\overline{CS}$	t_{ACS}	—	20	—	20	—	25	—	30	—	30	ns	*3, *4
Access time from address	t_{AA}	—	30	—	35	—	40	—	50	—	55	ns	*3,*5,*14
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	50	—	55	—	ns	
$\overline{RAS}$ to column address hold time	t_{AHR}	15	—	15	—	15	—	15	—	15	—	ns	*16
Output hold time from address	t_{AOH}	5	—	5	—	5	—	5	—	5	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	*6
Column address hold time to $\overline{RAS}$ on read	t_{AR}	60	—	70	—	80	—	100	—	120	—	ns	

Write Cycle

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	*10
Write command hold time	t_{WCH}	15	—	15	—	20	—	25	—	25	—	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	55	—	65	—	75	—	95	—	115	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	—	20	—	25	—	25	—	30	—	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20	—	20	—	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	*11
Data-in hold time	t_{DH}	15	—	15	—	20	—	25	—	25	—	ns	*11
Data-in hold time to $\overline{RAS}$	t_{DHR}	55	—	65	—	75	—	95	—	115	—	ns	
Column address hold time or $\overline{RAS}$ or write	t_{AWR}	55	—	65	—	75	—	95	—	115	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Read-write cycle time	t_{RWC}	145	—	155	—	190	—	220	—	255	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	60	—	70	—	80	—	100	—	120	—	ns	*10
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	20	—	20	—	25	—	30	—	30	—	ns	*10
Column address to $\overline{WE}$ delay time	t_{AWD}	30	—	35	—	40	—	50	—	55	—	ns	*10
Output hold time from $\overline{WE}$	t_{WOH}	0	—	0	—	0	—	0	—	0	—	ns	

Refresh Cycle

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{ZRH}	10	—	10	—	10	—	10	—	10	—	ns	

SC Mode Cycle

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{SC}$ mode cycle time	t_{SC}	35	—	40	—	45	—	55	—	60	—	ns	
$\overline{SC}$ mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	—	100000	—	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSWD}	70	—	80	—	90	—	110	—	135	—	ns	
$\overline{SC}$ mode $\overline{CS}$ precharge time	t_{SI}	10	—	10	—	10	—	10	—	15	—	ns	
Write invalid time	t_{WI}	10	—	10	—	10	—	10	—	15	—	ns	

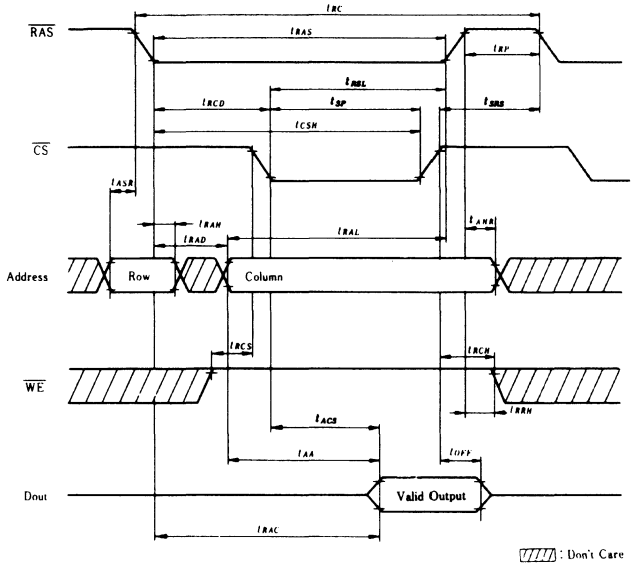
SC Mode Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM511002A -6		HM511002A -7		HM511002A -8		HM511002A -10		HM511002A -12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{SC}$ mode cycle time on read-write	t_{SRW}	70	—	80	—	90	—	105	—	120	—	ns	*12
Access time from previous $\overline{WE}$	t_{ALW}	—	65	—	75	—	85	—	100	—	115	ns	*3,*13
Previous $\overline{WE}$ to column address delay time	t_{LWAD}	20	35	20	40	25	45	25	50	30	60	ns	*15
Column address hold time to previous $\overline{WE}$	t_{AHLW}	65	—	75	—	85	—	100	—	115	—	ns	
Output enable time from $\overline{WE}$	t_{OW}	—	25	—	25	—	30	—	30	—	35	ns	

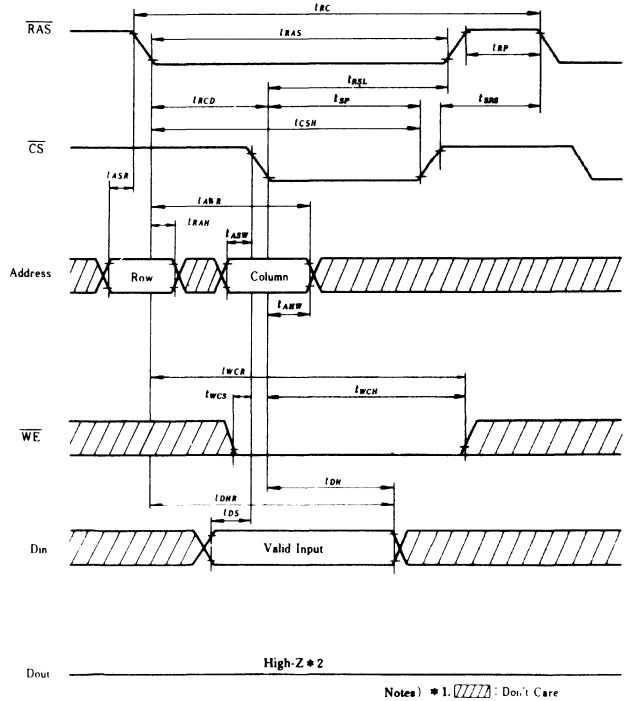
Notes)
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \leqq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geqq t_{RCD}$ (max), $t_{RAD} \leqq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leqq t_{RCD}$ (max) and $t_{RAD} \geqq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. Transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min) and $t_{AWD} \geqq t_{AWD}$ (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T.
13. Assumes that $t_{LWAD} \leqq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geqq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} is defined as the time at which the column address hold.
17. An initial pause of 100μs is required after power-up followed by eight or more initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). If internal refresh counter is used, eight or more $\overline{CS}$-before-$\overline{RAS}$ refresh cycles are required.

Timing Waveforms

- **Read Cycle**

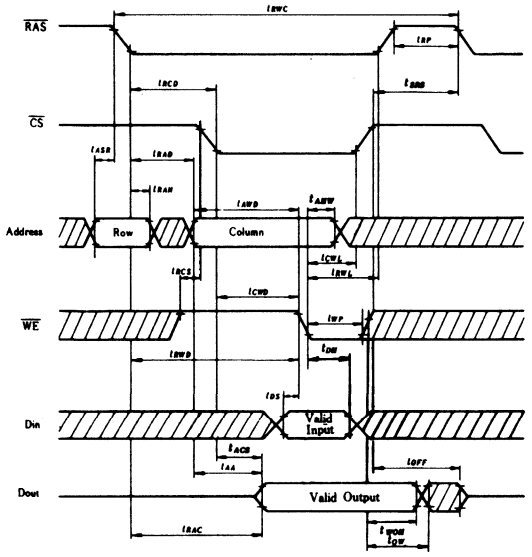


- **Early Write Cycle**



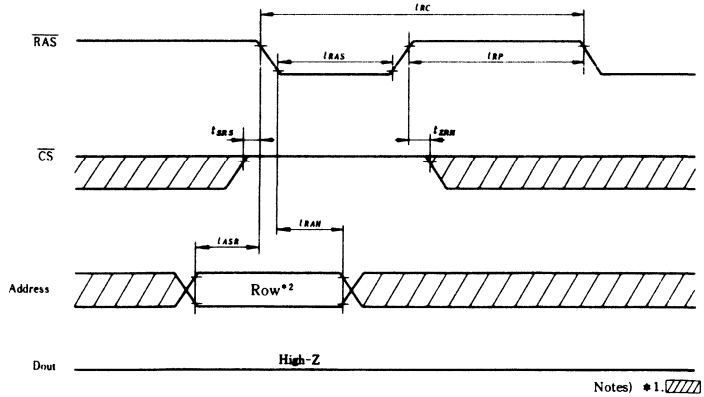
Notes) *1. : Don't Care
*2. $t_{WCS} \geq t_{WCS}$ (min)

- **Read-Modify-Write Cycle**



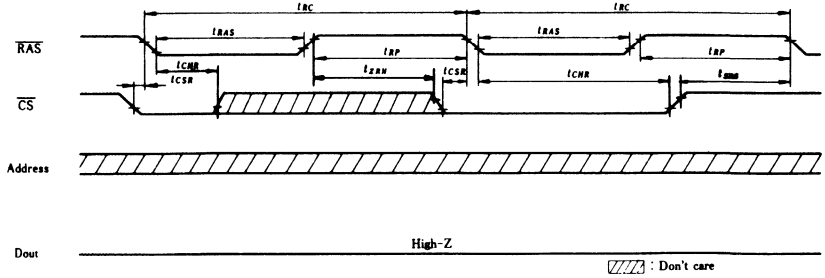
1 ▨: Don't Care

- **$\overline{RAS}$-Only Refresh Cycle**



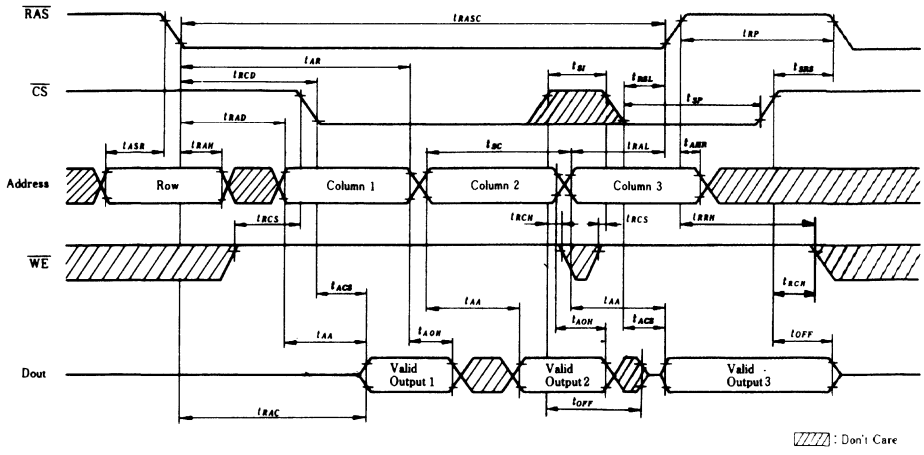
Notes) *1. ▨: Don't Care
*2. Refresh address A0-A8 (AX0-AX8)

- **$\overline{CS}$-before-$\overline{RAS}$ Refresh Cycle**

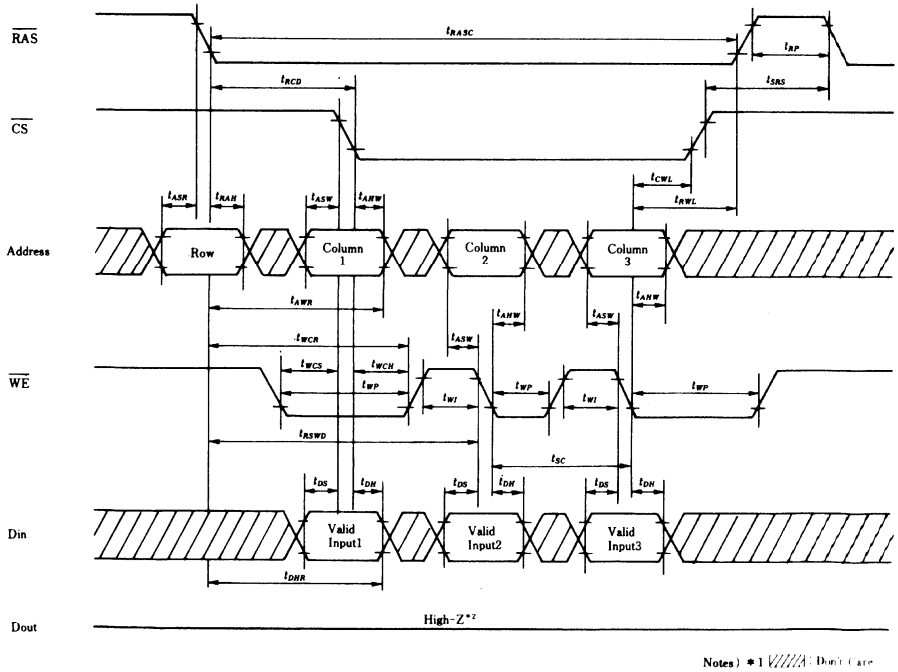


▨: Don't care

- **Static Column Mode Read Cycle**

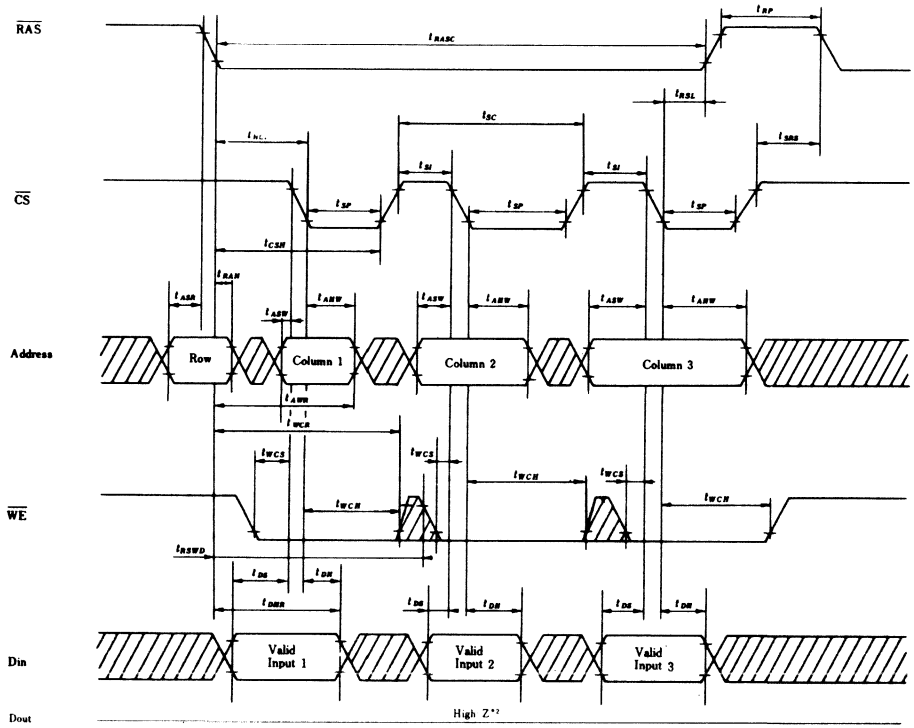


- **Static Column Mode Write Cycle-1**



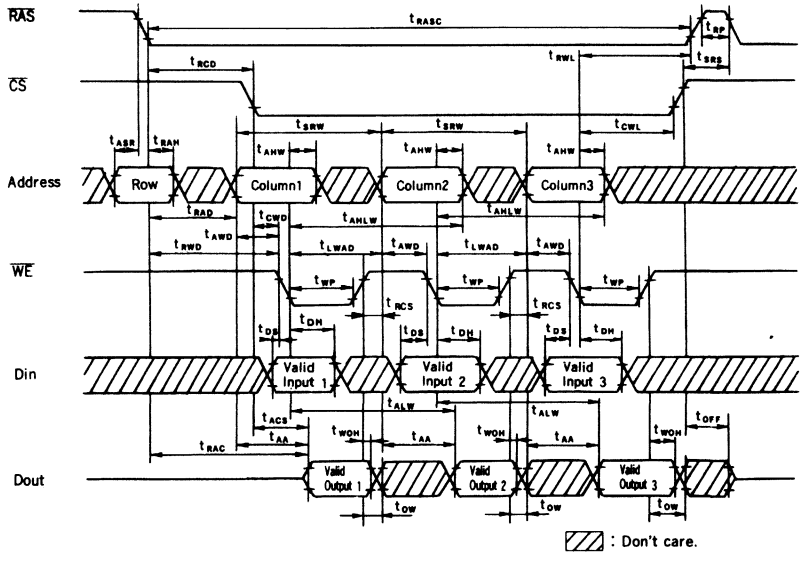
Notes) *1 : Don't Care
*2 $t_{WCS} \geq t_{WCS}$ (min)

- **Static Column Mode Write Cycle-2**

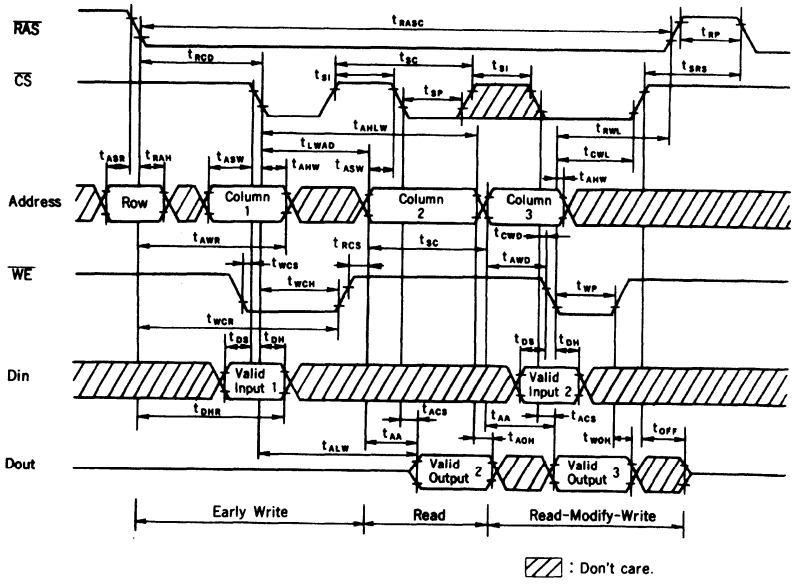


Notes) *1. ▨ : Don't care
*2. twcs ≧ twcs(min)

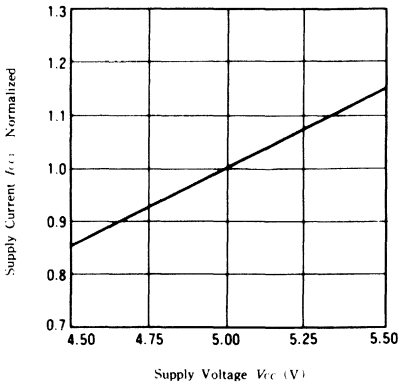
- **Static Column Mode Read-Modify-Write Cycle**



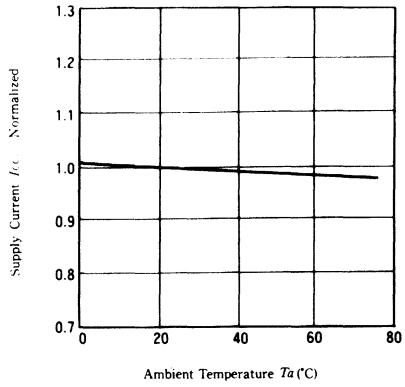
- **Static Column Mode Mixed Cycle**



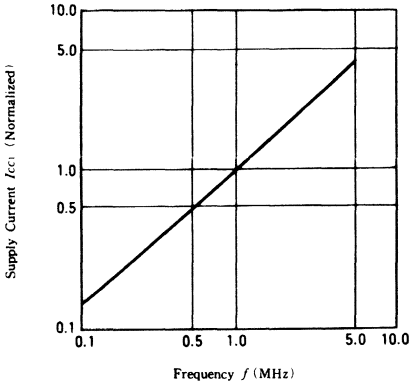
SUPPLY CURRENT (ACTIVE) vs. SUPPLY VOLTAGE



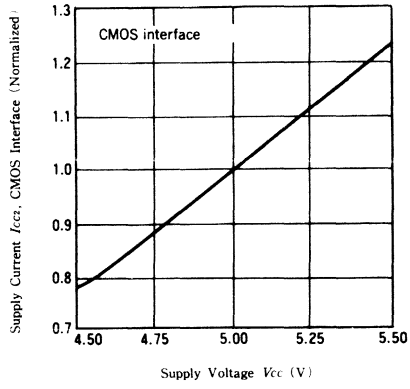
SUPPLY CURRENT (ACTIVE) vs. AMBIENT TEMPERATURE



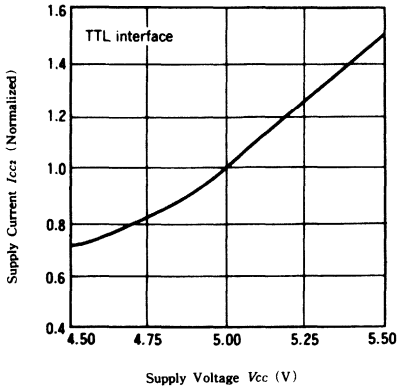
SUPPLY CURRENT (ACTIVE) vs. FREQUENCY



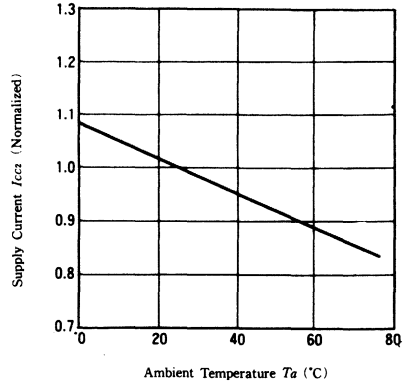
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



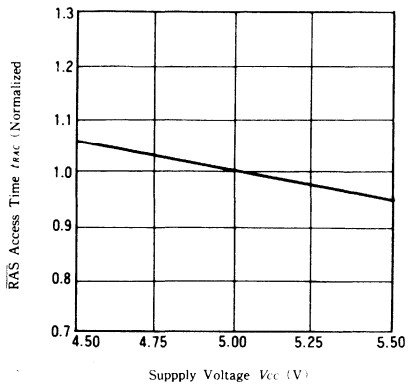
SUPPLY CURRENT (STANDBY) vs. SUPPLY VOLTAGE



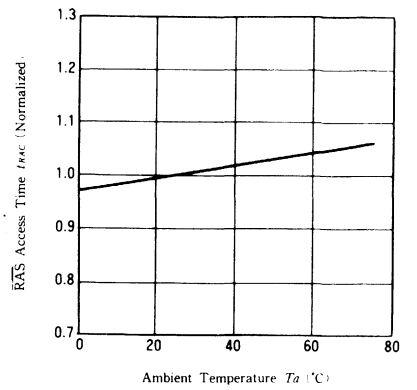
SUPPLY CURRENT (STANDBY) vs. AMBIENT TEMPERATURE



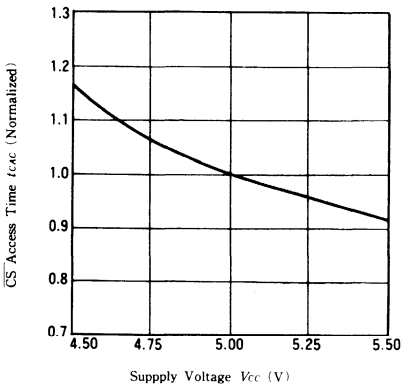
$\overline{RAS}$ ACCESS TIME vs. SUPPLY VOLTAGE



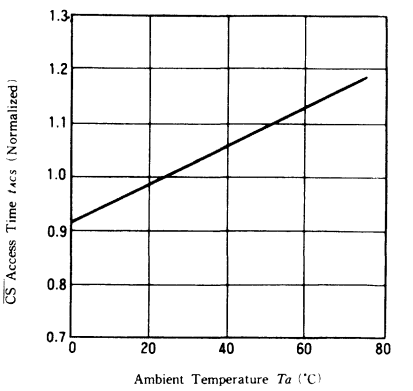
$\overline{RAS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



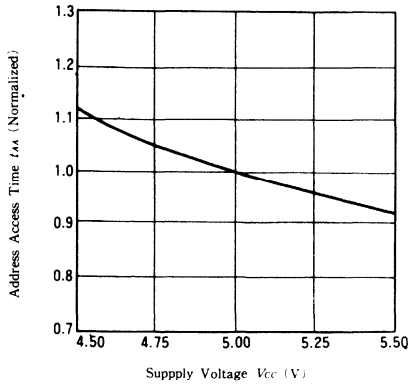
$\overline{CS}$ ACCESS TIME vs. SUPPLY VOLTAGE



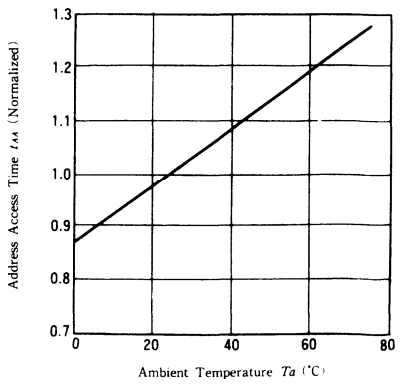
$\overline{CS}$ ACCESS TIME vs. AMBIENT TEMPERATURE



ADDRESS ACESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HM514400 Series

1,048,576-Word × 4-Bit Dynamic RAM

The Hitachi HM514400 is a CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM514400 has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514400 offers fast page mode as a high speed access mode.
Multiplexed address input permits the HM514400 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

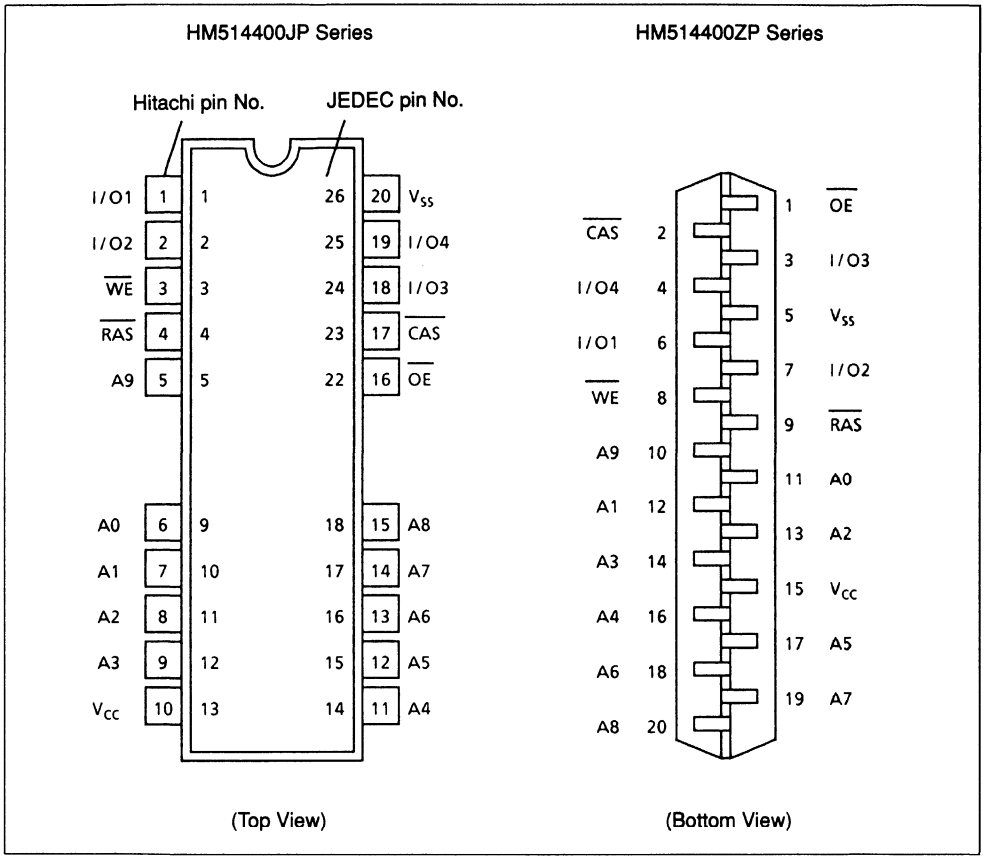
Ordering Information

Type No.	Access time	Package
HM514400JP-8	80 ns	350-mil 20-pin plastic SOJ (CP-20DA)
HM514400JP-10	100 ns	
HM514400JP-12	120 ns	
HM514400ZP-8	80 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514400ZP-10	100 ns	
HM514400ZP-12	120 ns	

Features

- Single 5 V (±10%)
- High speed
  - Access time
    80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode
    495 mW/440 mW/385 mW (max)
  - Standby mode 11 mW (max)
- Fast page mode capability
- 1,024 refresh cycles: (16 ms)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function

Pin Arrangement

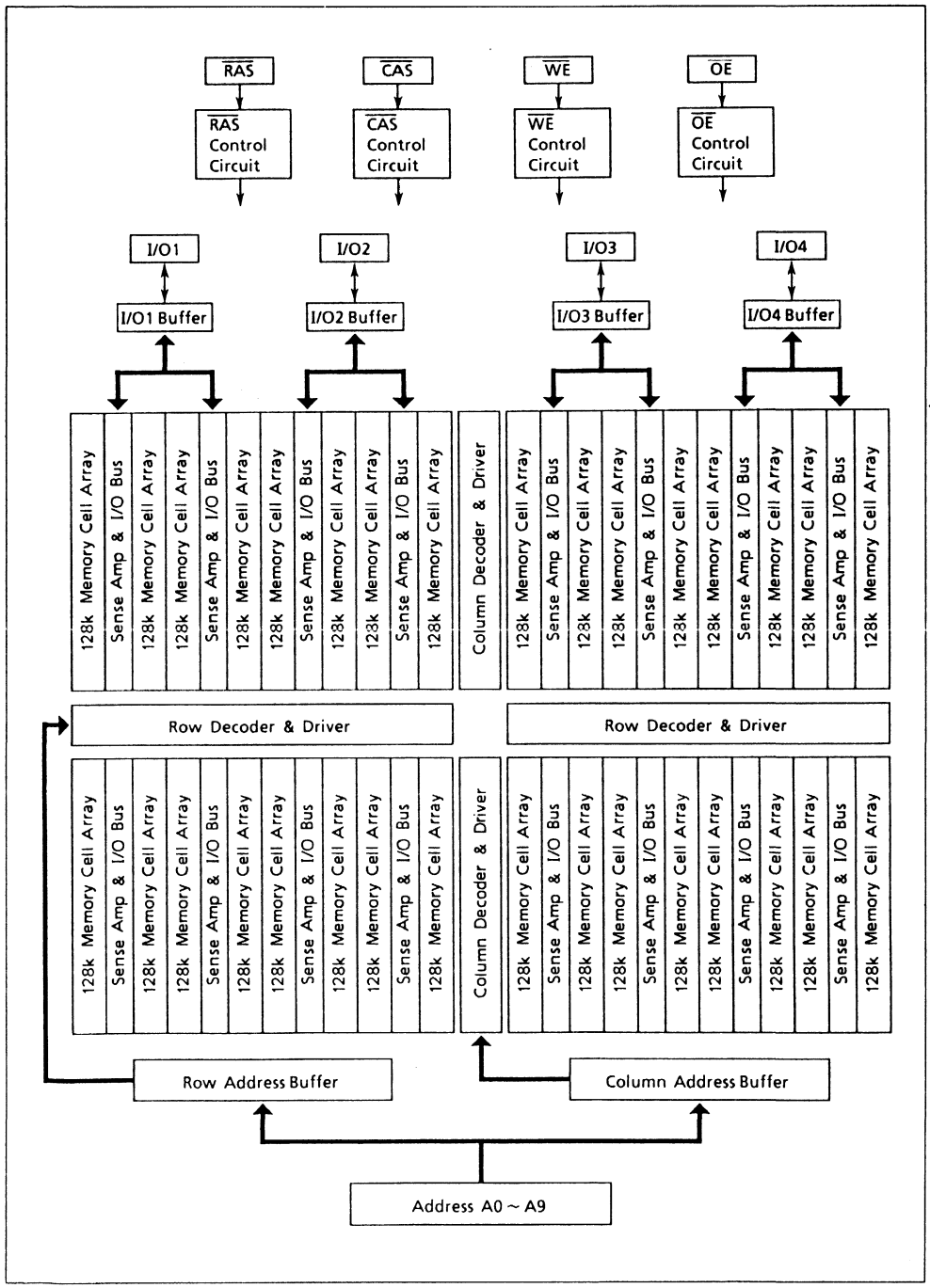


Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
I/O1 – I/O4	Data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe

Pin name	Function
$\overline{WE}$	Read/write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input high voltage		V_{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514400 -8		HM514400 -10		HM514400 -12				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2 V Dout = High-Z	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514400 -8		HM514400 -10		HM514400 -12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1, 4
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	4
Fast page mode current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = −5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout

AC Characteristics (Ta = 0°C to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*1, *14, *15, *16

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514400 -8 Min	HM514400 -8 Max	HM514400 -10 Min	HM514400 -10 Max	HM514400 -12 Min	HM514400 -12 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13, 17
Access time from address	t_{AA}	—	40	—	45	—	55	ns	3, 5 13, 17
Access time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	3, 17
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	18
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	18
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	HM514400 -8 Min	HM514400 -8 Max	HM514400 -10 Min	HM514400 -10 Max	HM514400 -12 Min	HM514400 -12 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	55	—	60	—	70	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

Refresh Cycle

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	15	—	ns	

Fast Page Mode Cycle

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12

Fast Page Mode Cycle (cont)

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	3, 13, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode read-modify-write cycle time	t_{PCM}	105	—	110	—	130	—	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	80	—	85	—	100	—	ns	10

Test Mode Cycle

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	20	—	20	—	20	—	ns	

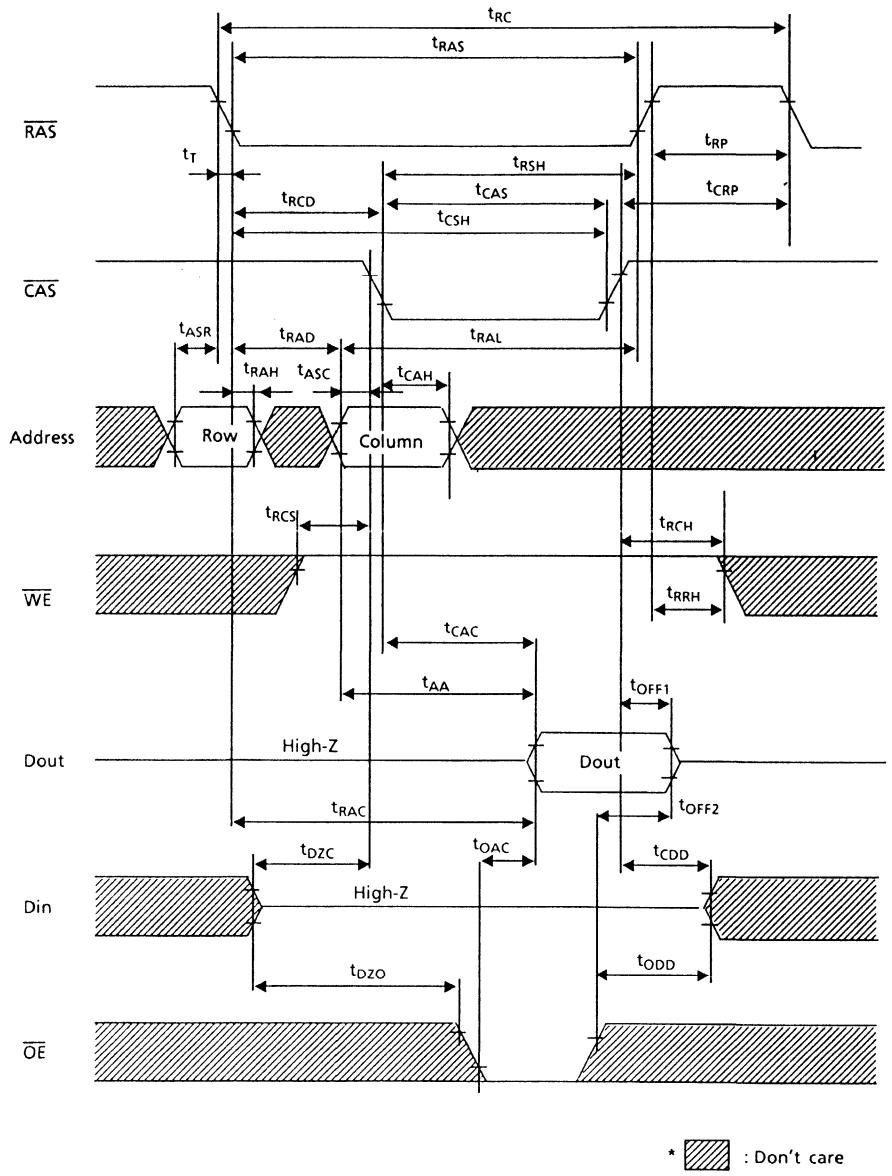
Counter Test Cycle

		HM514400 -8		HM514400 -10		HM514400 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	50	—	60	—	ns	

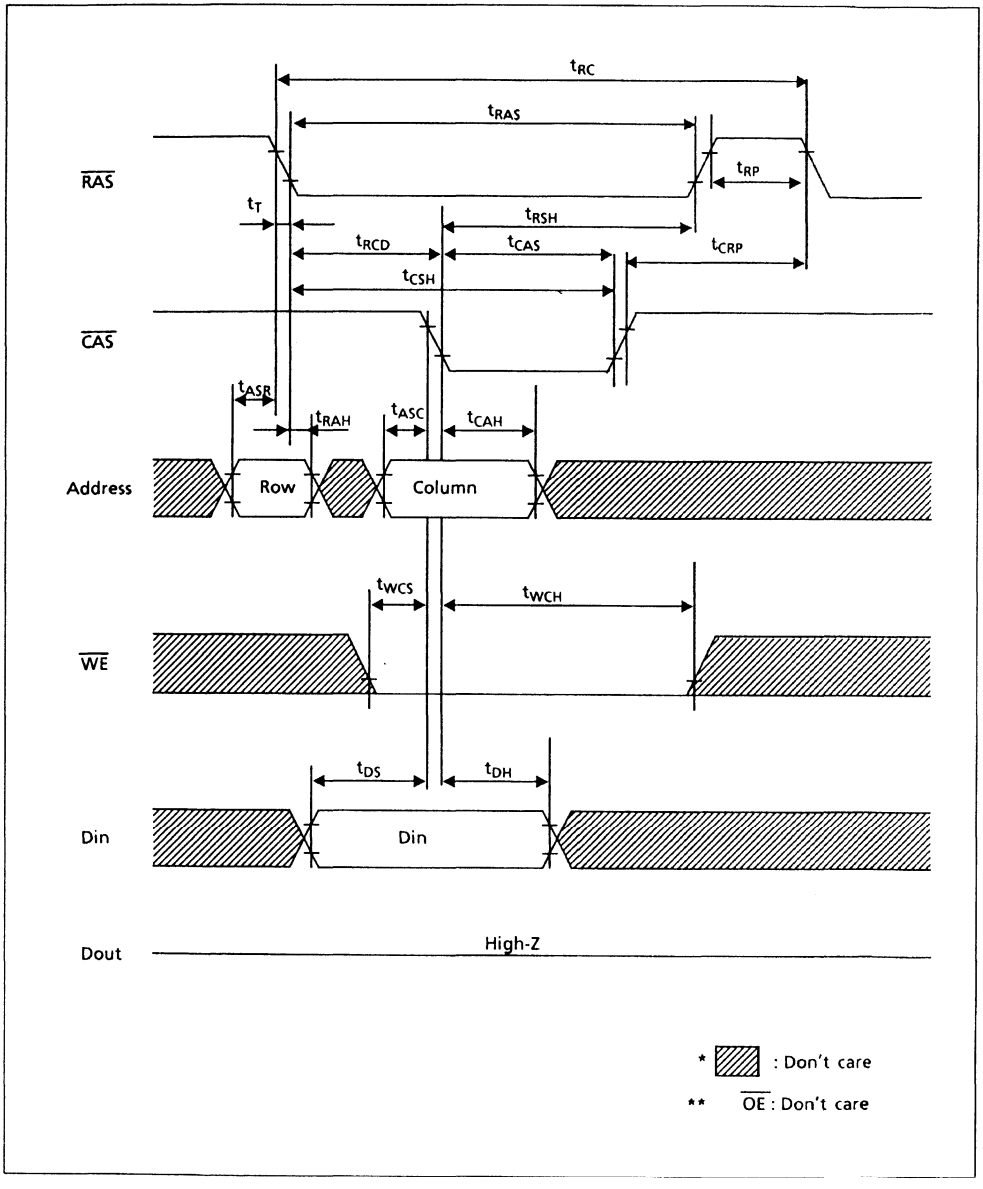
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O3 and data input pin is I/O2. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. Either t_{RCH} or t_{RRH} shall be satisfied.

Timing Waveforms

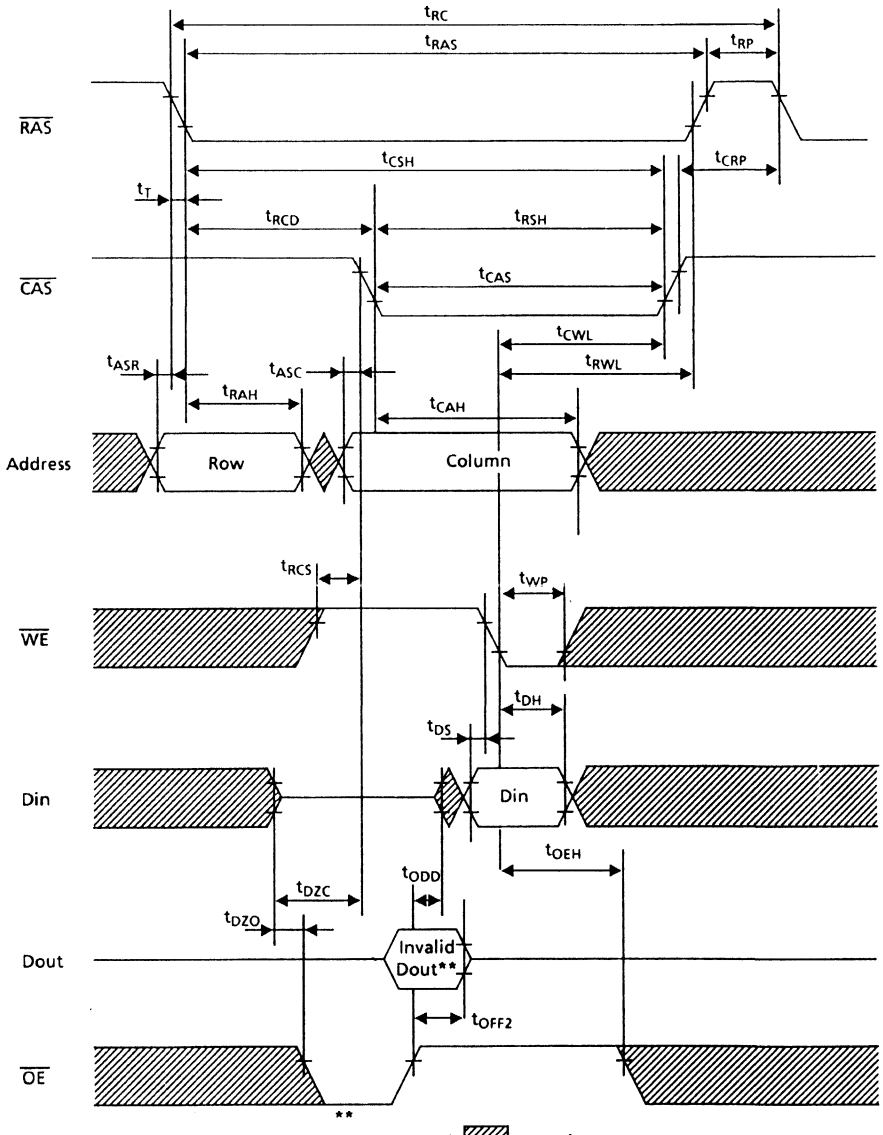
Read Cycle



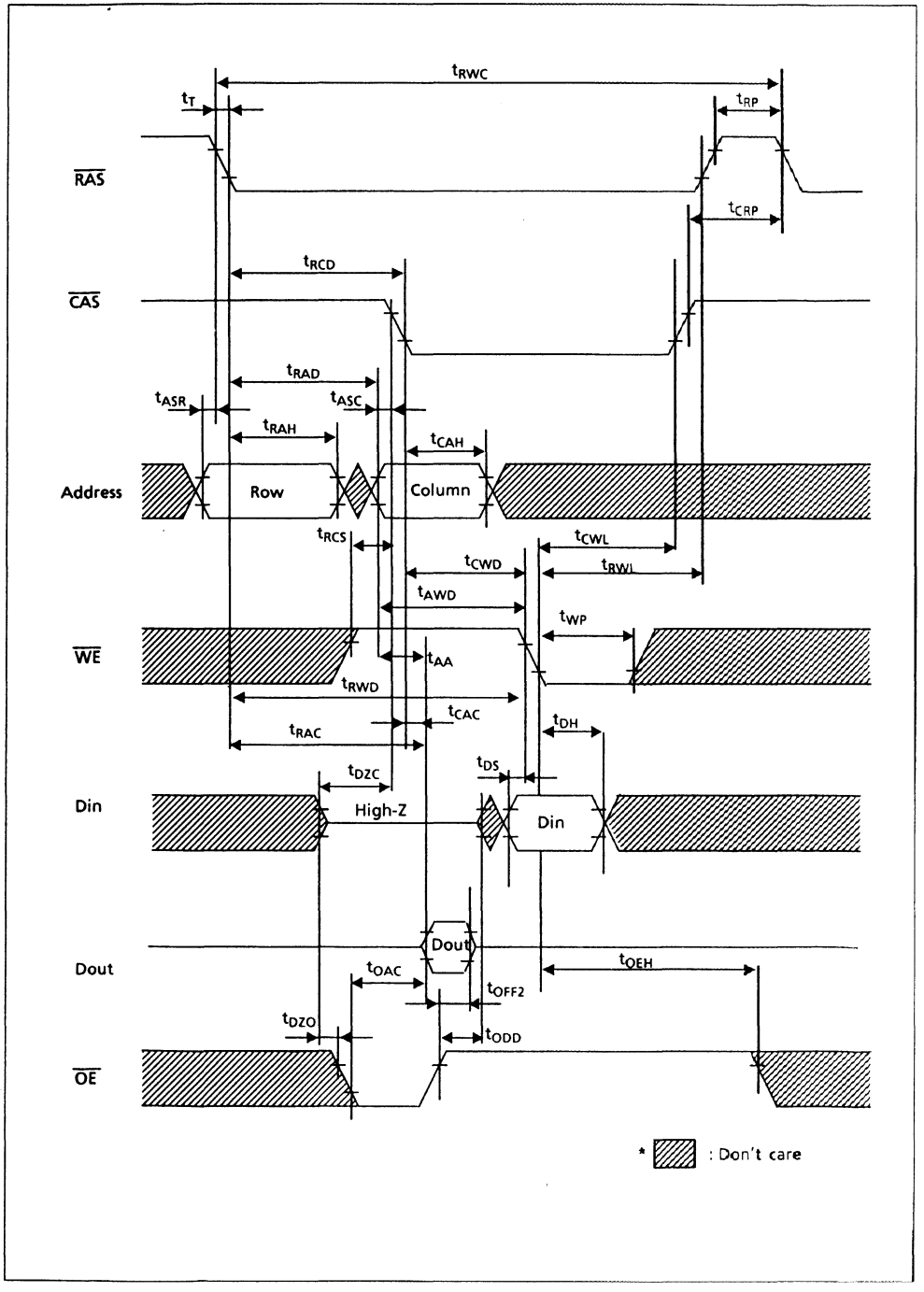
Early Write Cycle



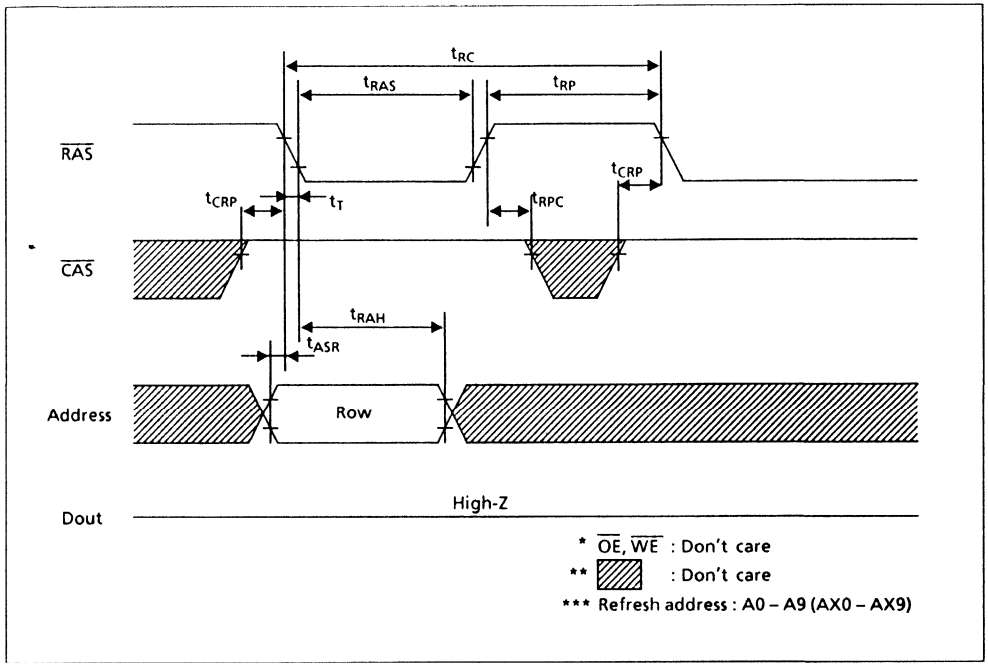
Delayed Write Cycle



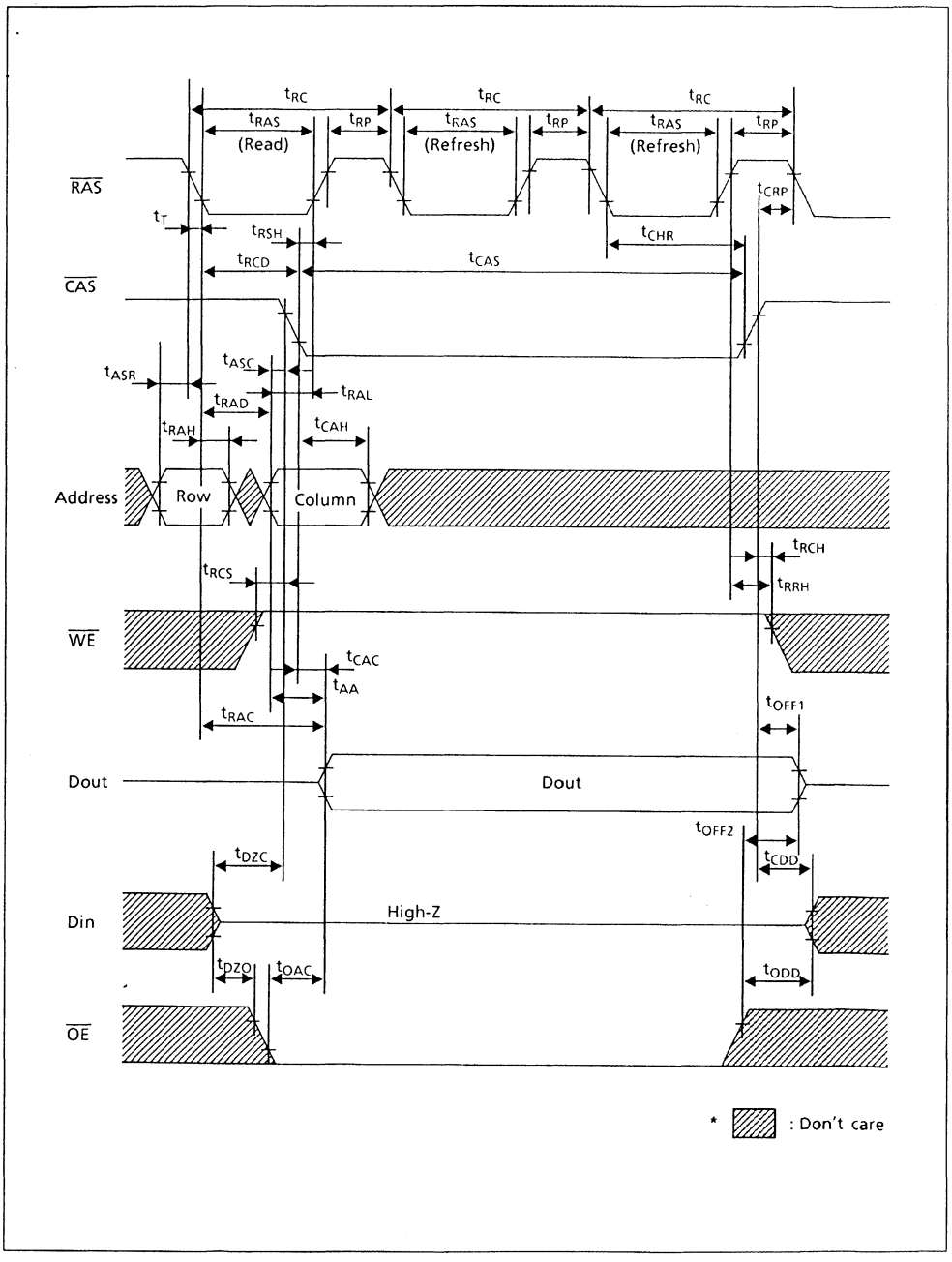
Read-Modify-Write Cycle



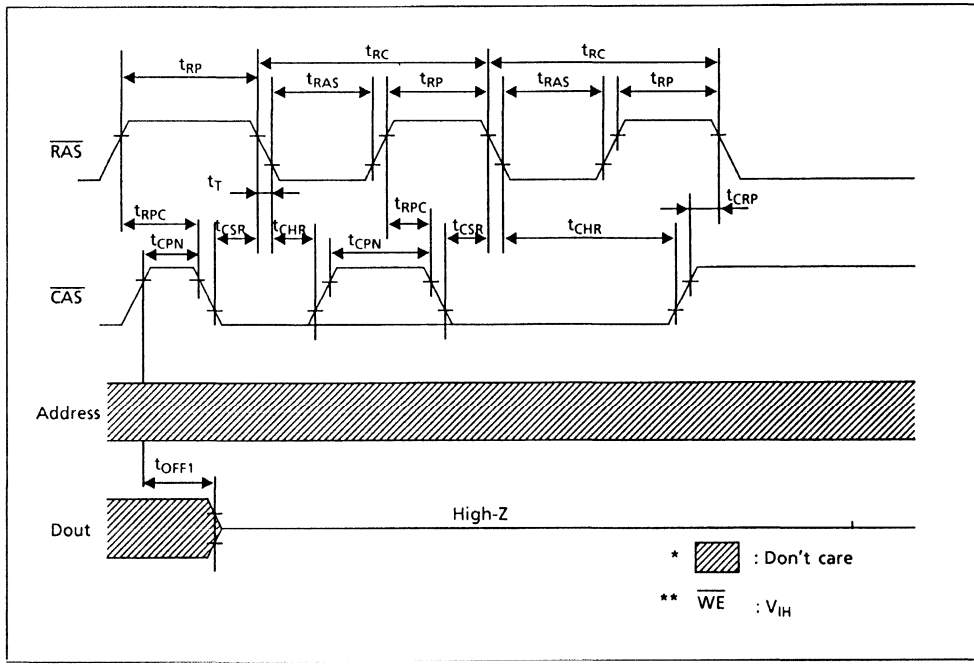
$\overline{RAS}$-Only Refresh Cycle



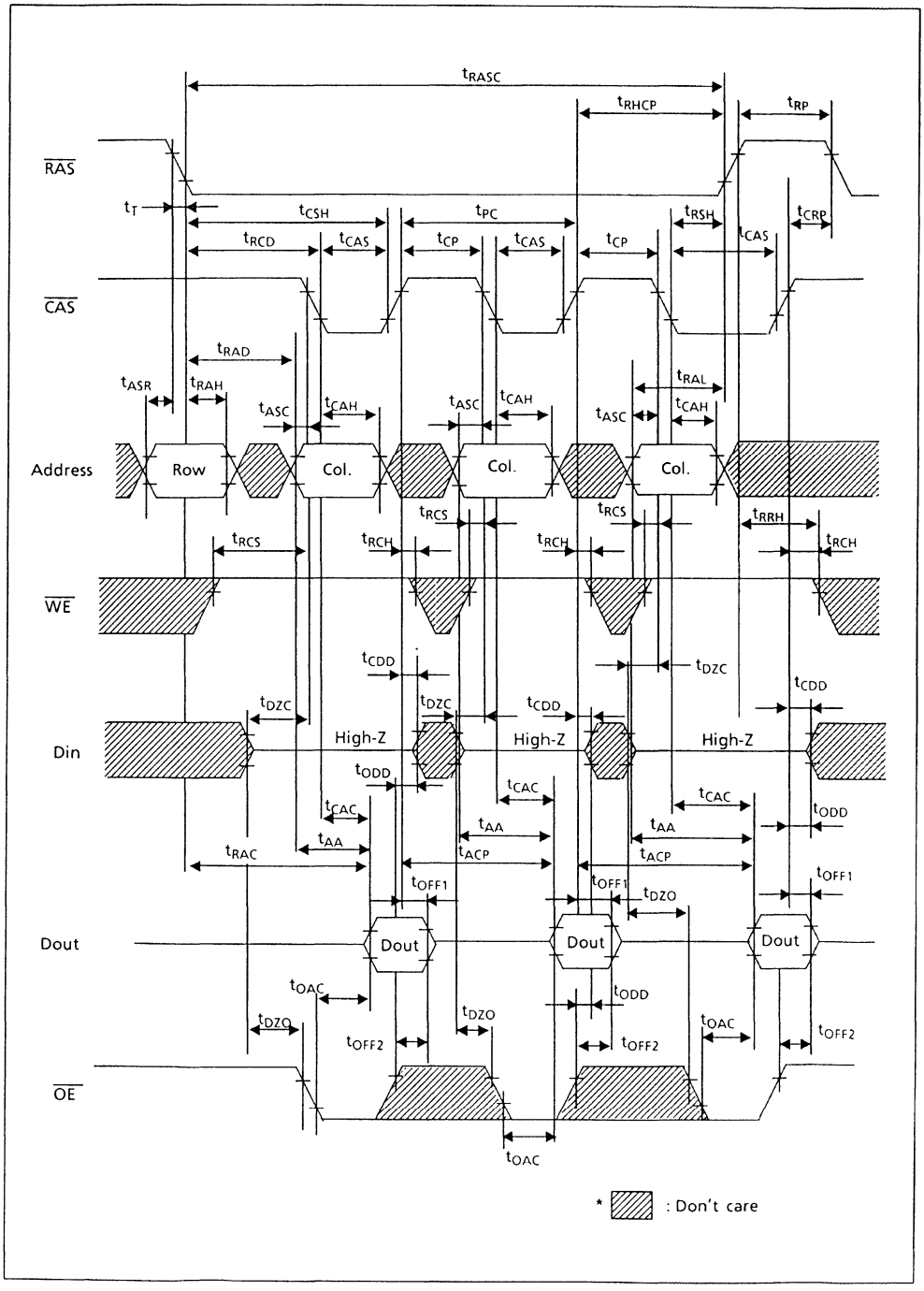
Hidden Refresh Cycle



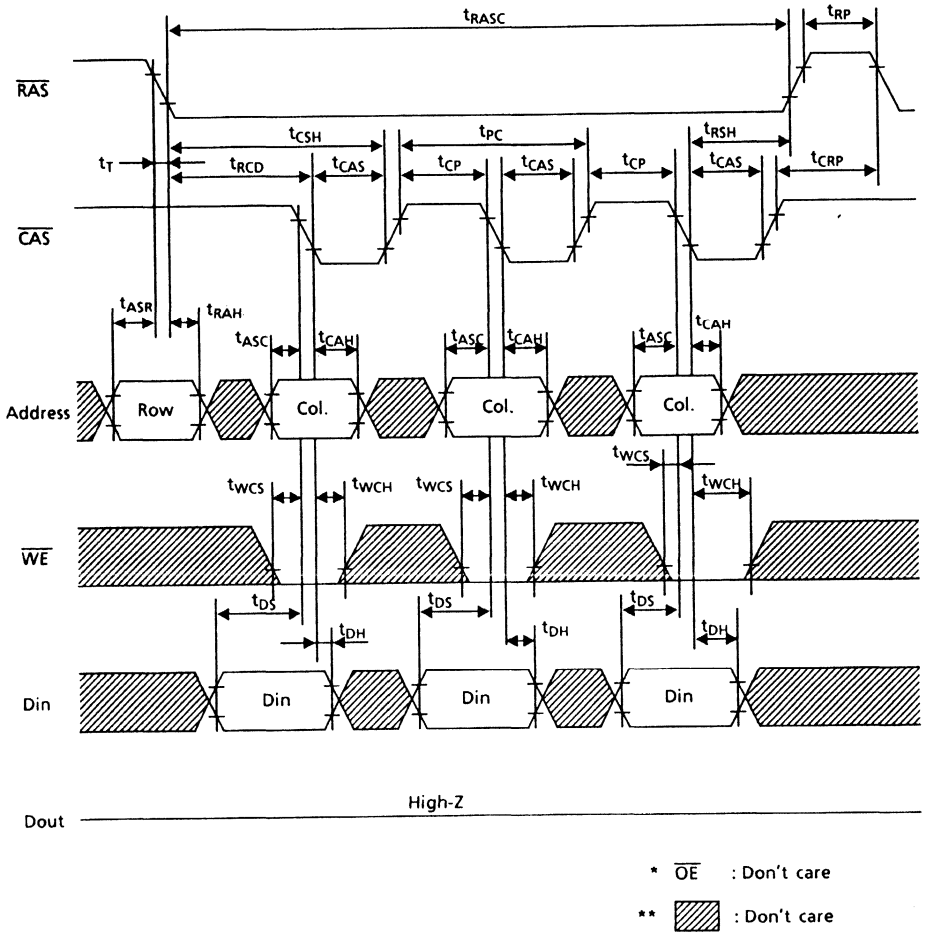
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



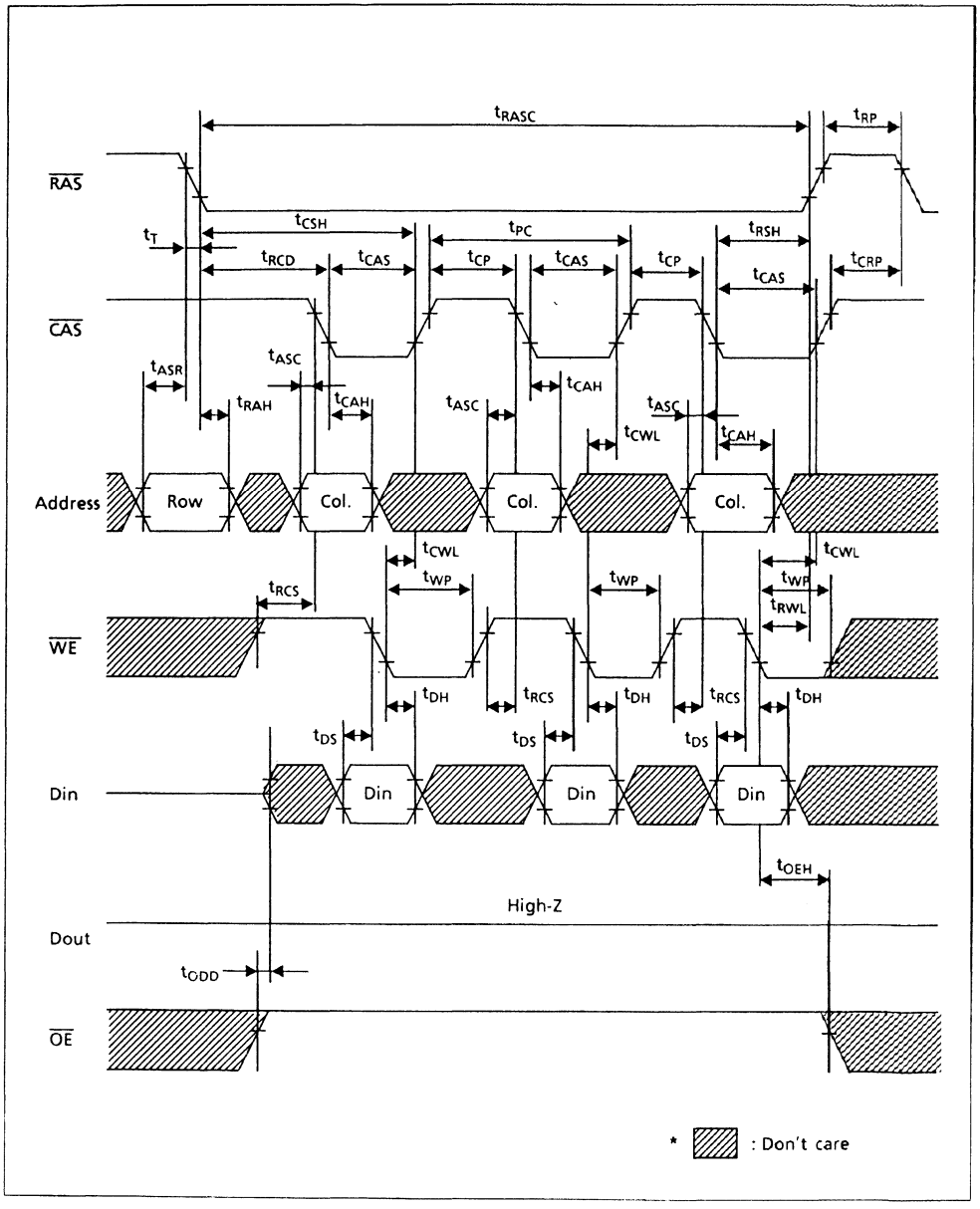
Fast Page Mode Read Cycle



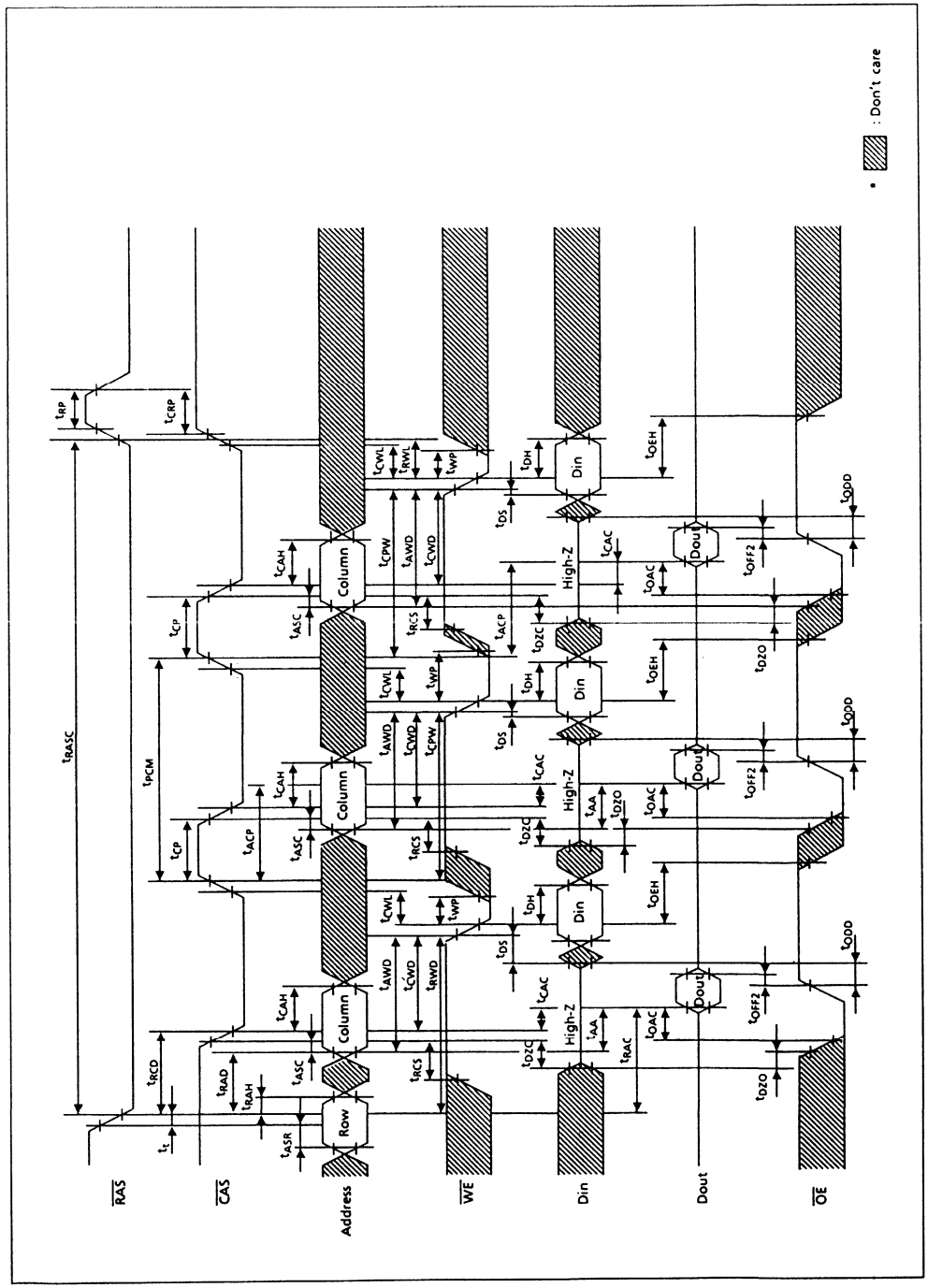
Fast Page Mode Early Write Cycle



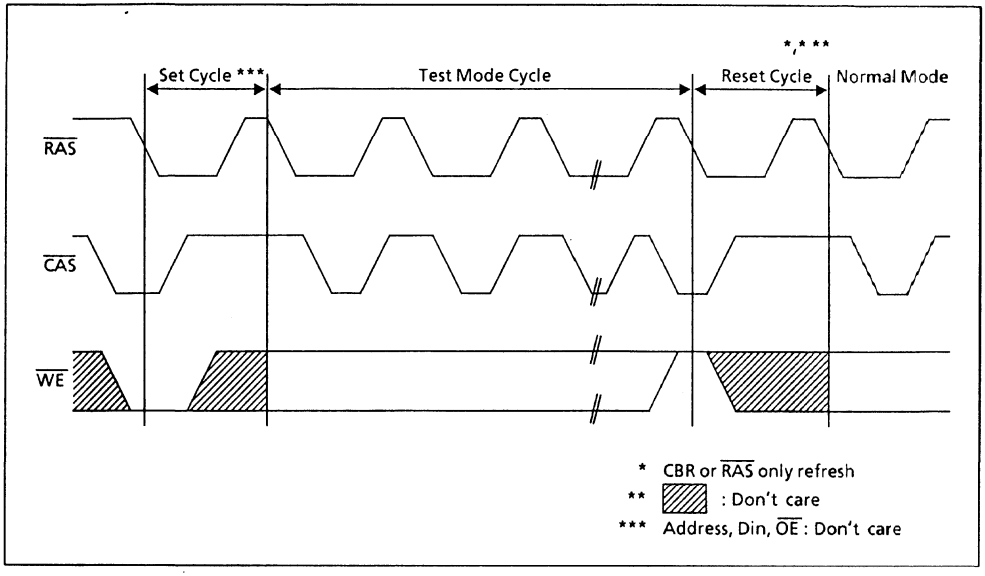
Fast Page Delayed Write Cycle



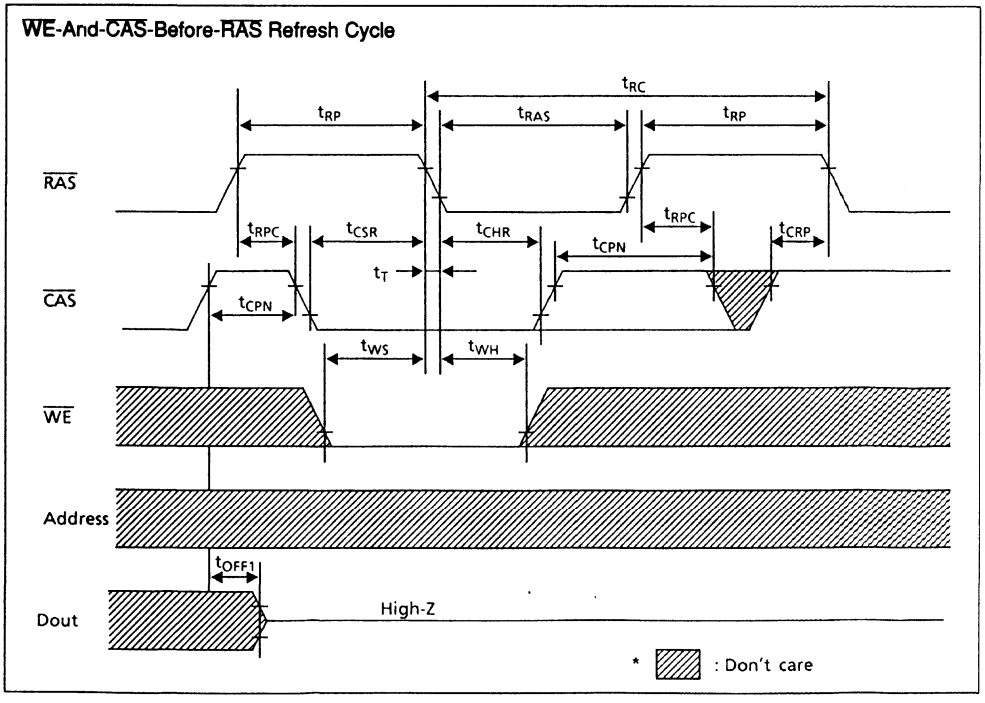
Fast Page Mode Read-Modify-Write Cycle



Test Mode Cycle

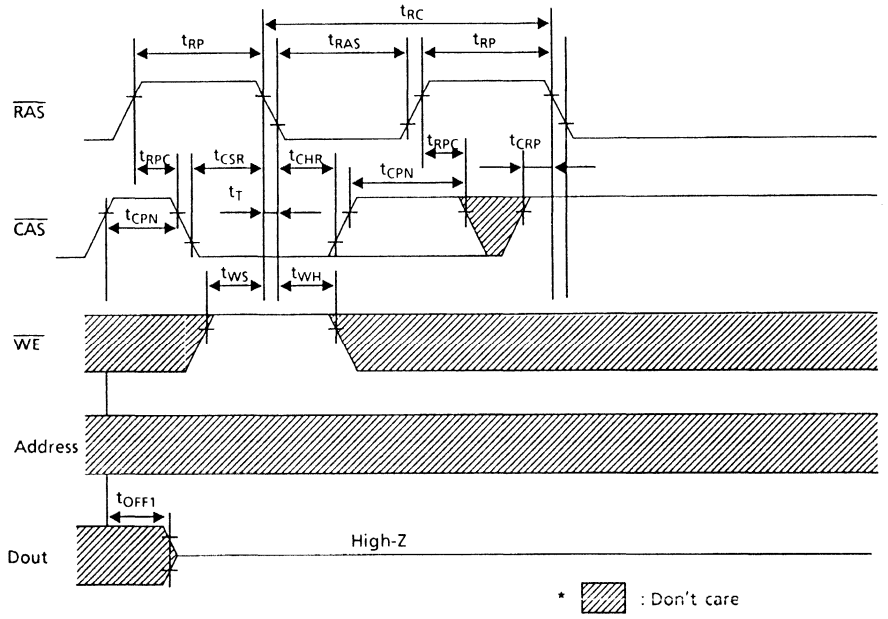


Test Mode Set Cycle

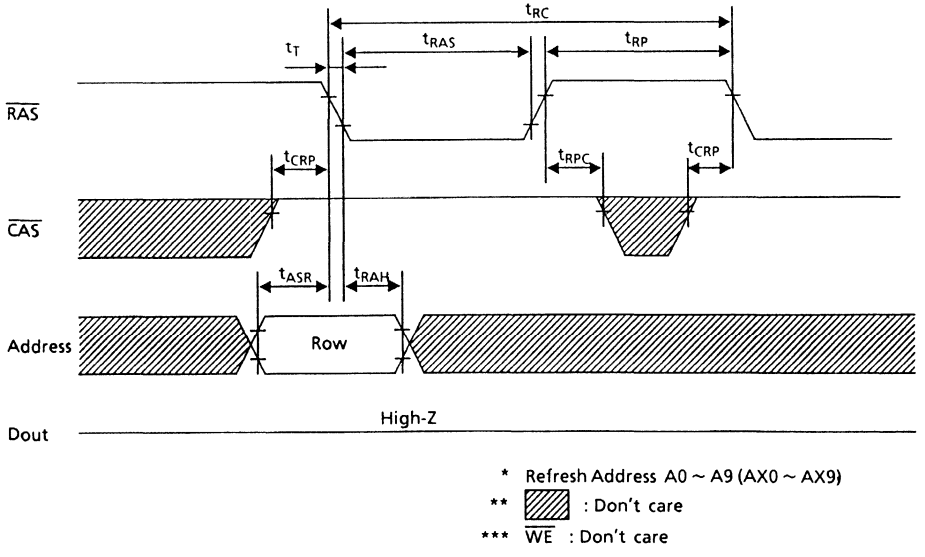


Test Mode Reset Cycle

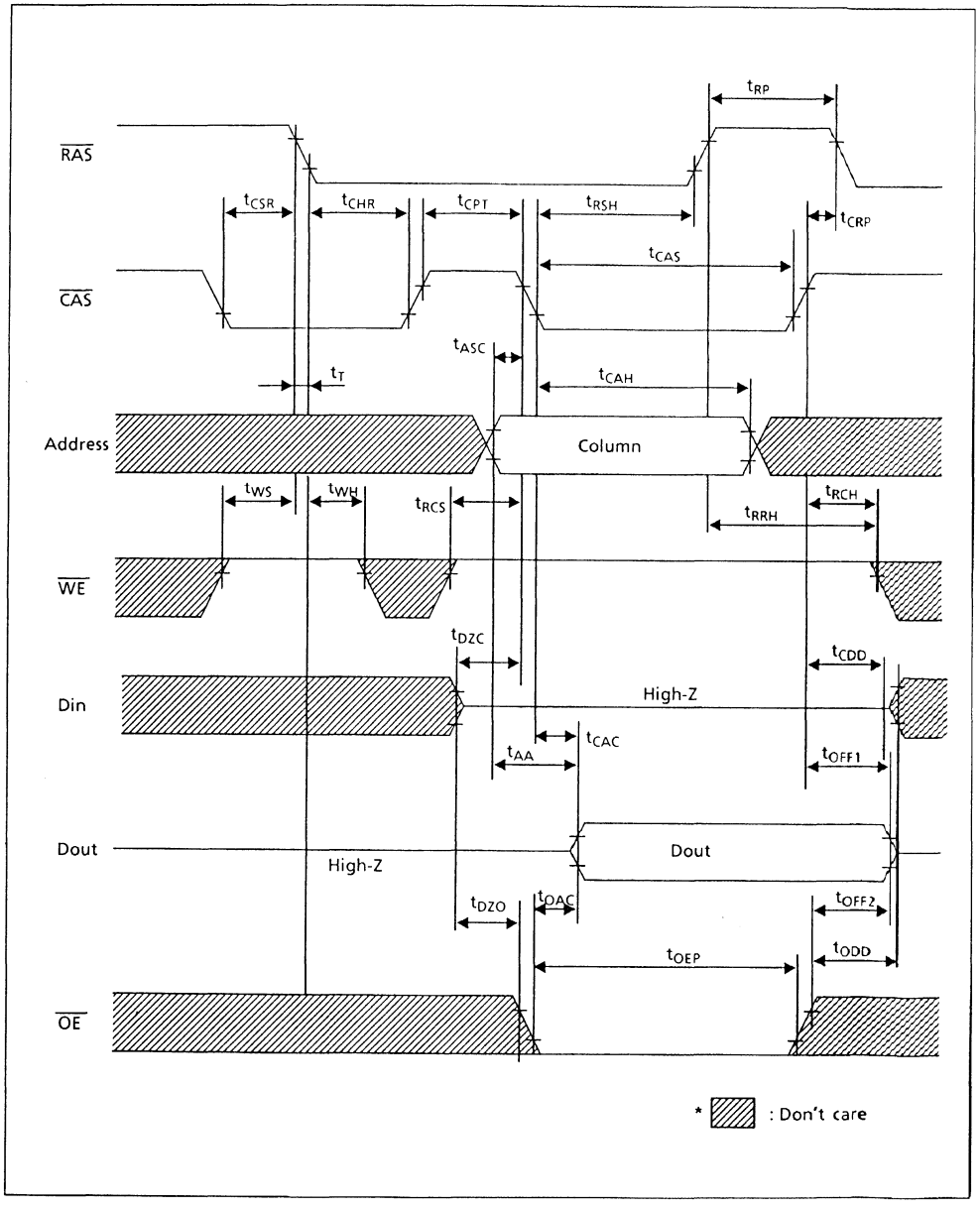
CAS-Before-RAS Refresh Cycle



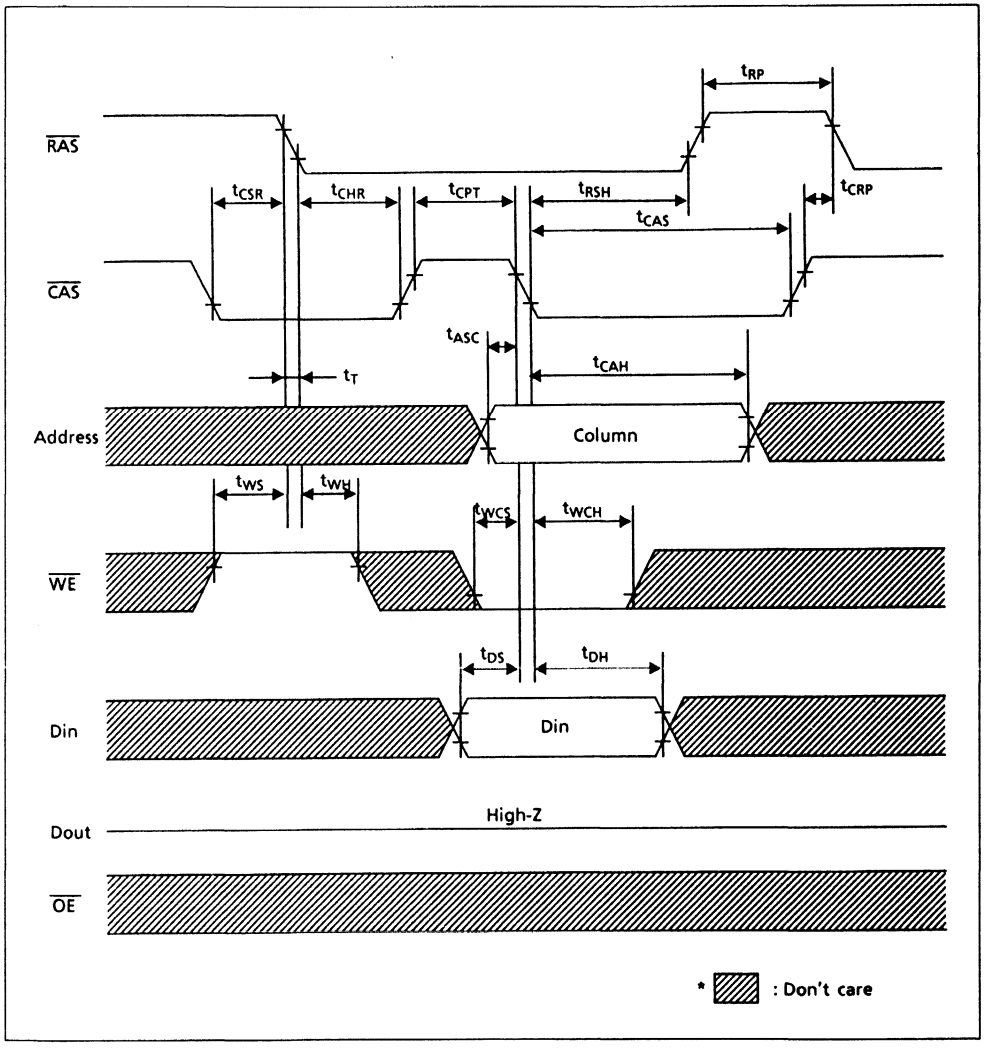
RAS-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514402 Series

1,048,576-Word × 4-Bit Dynamic RAM

The Hitachi HM514402 is a CMOS dynamic RAM organized 1,048,576-word × 4-bit. HM514402 has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514402 offers static column mode as a high speed access mode.
Multiplexed address input permits the HM514402 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Ordering Information

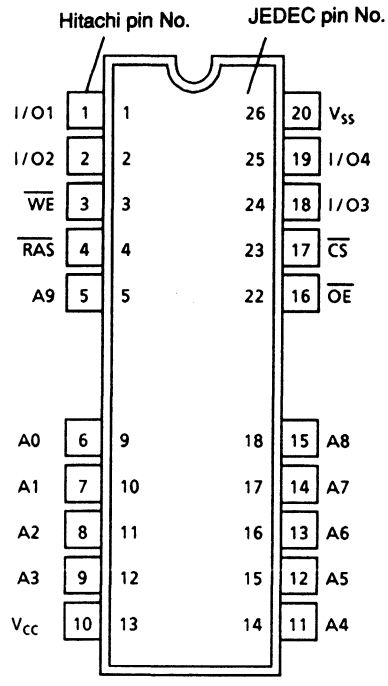
Type No.	Access time	Package
HM514402JP-8	80 ns	350-mil 20-pin plastic SOJ (CP-20DA)
HM514402JP-10	100 ns	
HM514402JP-12	120 ns	
HM514402ZP-8	80 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514402ZP-10	100 ns	
HM514402ZP-12	120 ns	

Features

- Single 5 V (±10%)
- High speed
  - Access time
    80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode
    495 mW/440 mW/385 mW (max)
  - Standby mode 11 mW (max)
- Static column mode capability
- 1,024 refresh cycles: (16 ms)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function

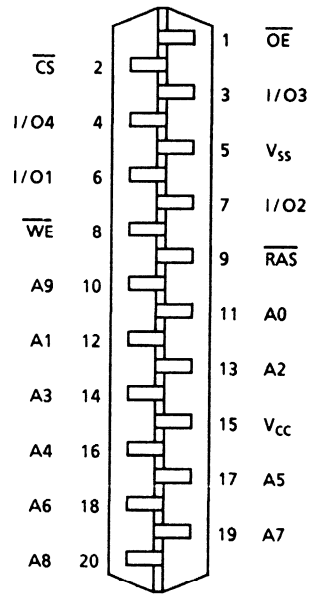
Pin Arrangement

HM514402JP Series



(Top View)

HM514402ZP Series



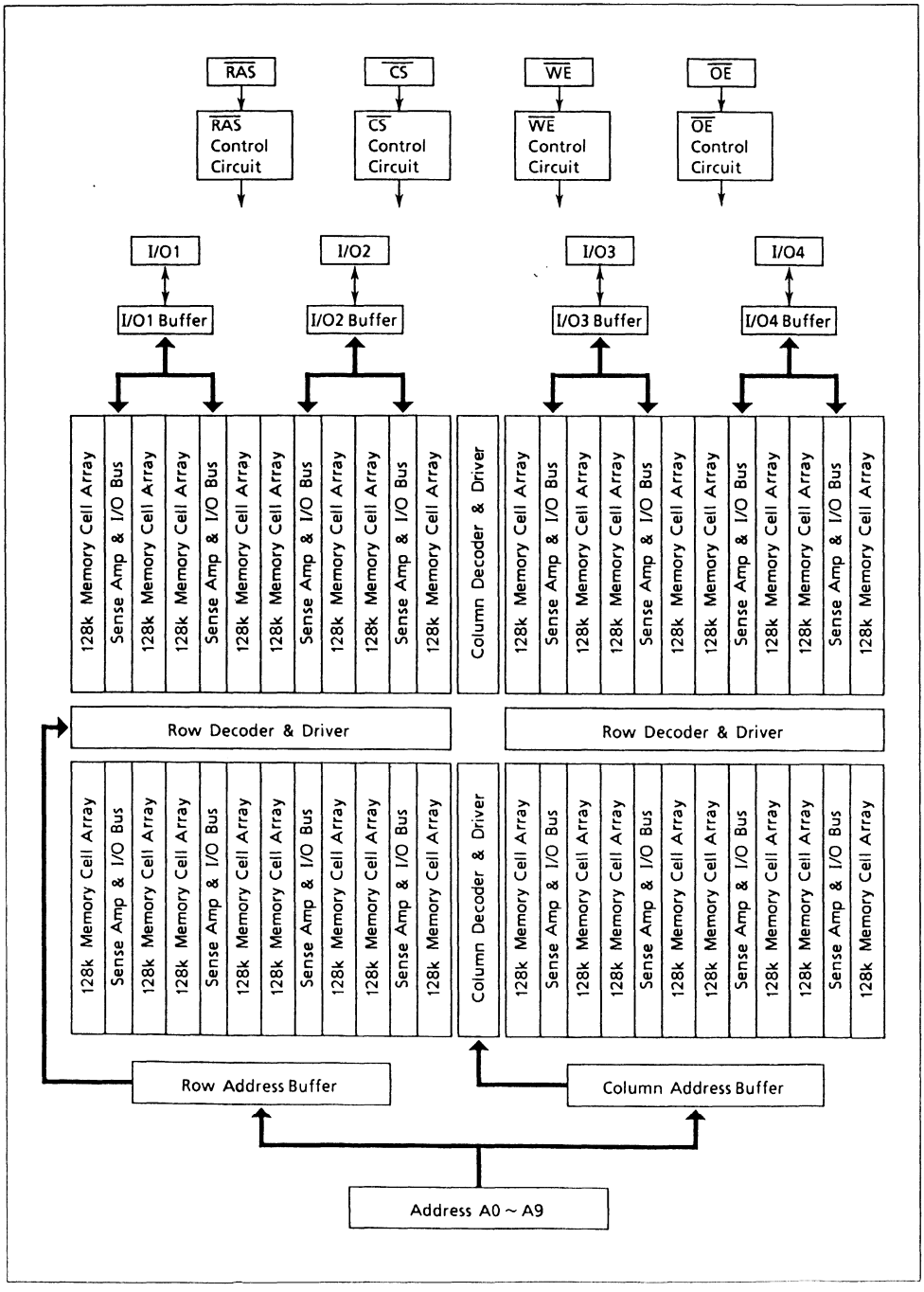
(Bottom View)

Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
I/O1 – I/O4	Data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select

Pin name	Function
$\overline{WE}$	Read/write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input high voltage		V_{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514402 -8		HM514402 -10		HM514402 -12				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} − 0.2 V Dout = High-Z	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514402 -8		HM514402 -10		HM514402 -12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1, 5
$\overline{CS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	5
Static column mode current	I_{CC9}	—	90	—	80	—	70	mA	t_{SC} = min	1, 3, 4
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.
4. Invalid address is prohibited during static colmn cycle.
5. Clock voltages ($\overline{RAS}$ and $\overline{CS}$) must be applied simultaneously with or prior to applying supply voltage.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout

AC Characteristics (Ta = 0°C to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *17, *18, *19

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM514402 -8		HM514402 -10		HM514402 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ pulse width	t_{SP}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASW}	0	—	0	—	0	—	ns	
Column address hold time	t_{AHW}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{SRS}	5	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 20
Access time from $\overline{CS}$	t_{ACS}	—	25	—	25	—	30	ns	3, 4, 20
Access time from address	t_{AA}	—	40	—	45	—	55	ns	3, 5 14, 20
Access time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	20
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CS}$	t_{RCH}	0	—	0	—	0	—	ns	21
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	21
$\overline{RAS}$ to column address hold time	t_{AHR}	15	—	15	—	15	—	ns	16
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Column address hold time to $\overline{RAS}$ on read	t_{AR}	80	—	100	—	120	—	ns	
Output buffer turn-off time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
Output hold time from address	t_{AOH}	5	—	5	—	5	—	ns	
$\overline{CS}$ to Din delay time	t_{CDD}	20	—	25	—	30	—	ns	
$\overline{CS}$ hold time from $\overline{OE}$	t_{OCH}	25	—	25	—	30	—	ns	
$\overline{OE}$ hold time from $\overline{RAS}$	t_{ROH}	80	—	100	—	120	—	ns	
$\overline{OE}$ hold time from $\overline{CS}$	t_{COH}	25	—	25	—	30	—	ns	
$\overline{OE}$ pulse width	t_{OEP}	25	—	25	—	30	—	ns	

Write Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	20	—	25	—	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	70	—	95	—	115	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	20	—	25	—	ns	11
Data-in hold time to $\overline{RAS}$	t_{DHR}	70	—	95	—	115	—	ns	
Output hold time from $\overline{WE}$	t_{WOH}	0	—	0	—	0	—	ns	
Output enable time from $\overline{WE}$	t_{OW}	30	—	30	—	35	—	ns	20
Column address hold time to $\overline{RAS}$ on write	t_{AWR}	70	—	95	—	115	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	55	—	60	—	70	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	70	—	80	—	95	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{ZRH}	10	—	10	—	10	—	ns	
$\overline{CS}$ precharge time in normal mode	t_{SIN}	10	—	10	—	15	—	ns	

Static Column Mode Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
Static column mode cycle time	t_{SC}	45	—	50	—	60	—	ns	
Static column mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSWD}	80	—	100	—	120	—	ns	
Static column mode $\overline{CS}$ precharge time	t_{SI}	10	—	10	—	15	—	ns	
Write invalid time	t_{WI}	10	—	10	—	15	—	ns	

Static Column Mode Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
Static column mode cycle time on read-write	t_{SRW}	120	—	135	—	160	—	ns	12
Access time from previous $\overline{WE}$	t_{ALW}	—	80	—	90	—	110	ns	3, 13, 20
Previous $\overline{WE}$ to column address delay time	t_{LWAD}	20	40	25	45	30	55	ns	15
Column address hold time to previous $\overline{WE}$	t_{AHLW}	80	—	90	—	110	—	ns	

Test Mode Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	20	—	20	—	20	—	ns	

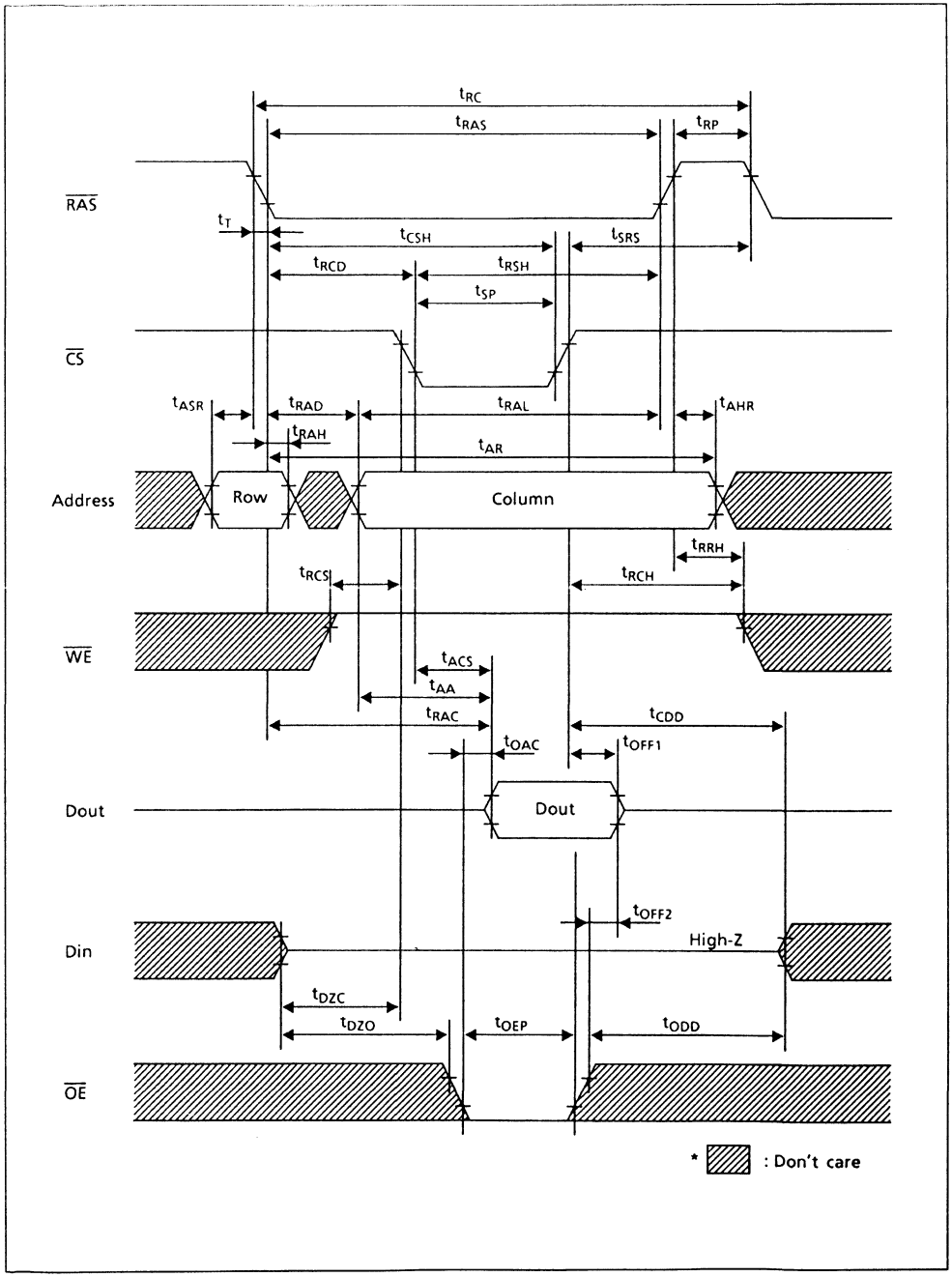
Counter Test Cycle

Parameter	Symbol	HM514402 -8 Min	HM514402 -8 Max	HM514402 -10 Min	HM514402 -10 Max	HM514402 -12 Min	HM514402 -12 Max	Unit	Notes
$\overline{CS}$ precharge time in counter test cycle	t_{CPT}	40	—	50	—	60	—	ns	

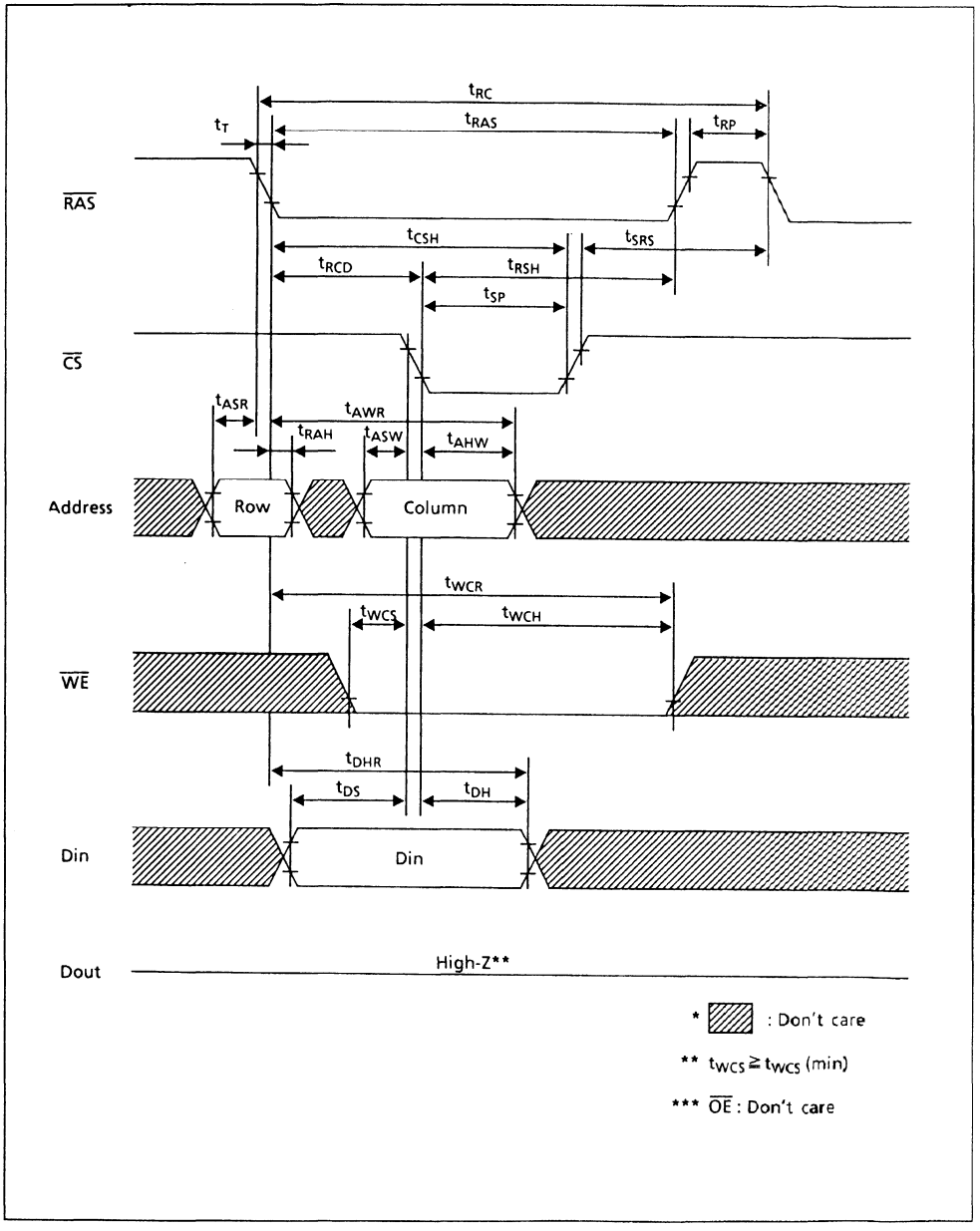
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (mas) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{SRW} (min) = t_{AWD} (min) +t_{LWAD} (max) + t_T
13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} defines the time at which the column address hold.
17. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CS}$-before-$\overline{RAS}$ refresh cycles is required. Clock voltages ($\overline{RAS}$ and $\overline{CS}$) must be applied simultaneously with or prior to applying supply voltage.
18. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffers prior to applying data to the device.
19. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O3 and data input pin is I/O2. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.
20. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{ACS}, t_{OAC}, t_{OW} and t_{ALW} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
21. Either t_{RCH} or t_{RRH} shall be satisfied.

Timing Waveforms

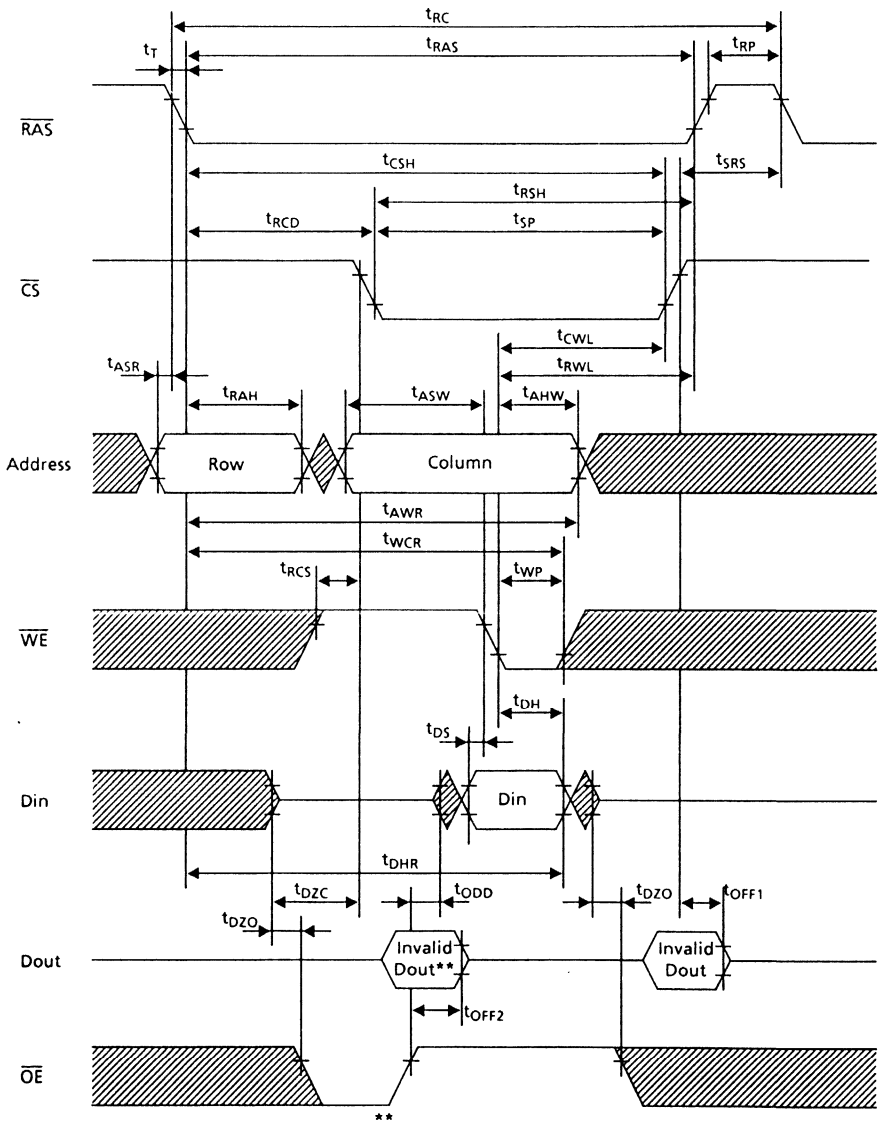
Read Cycle



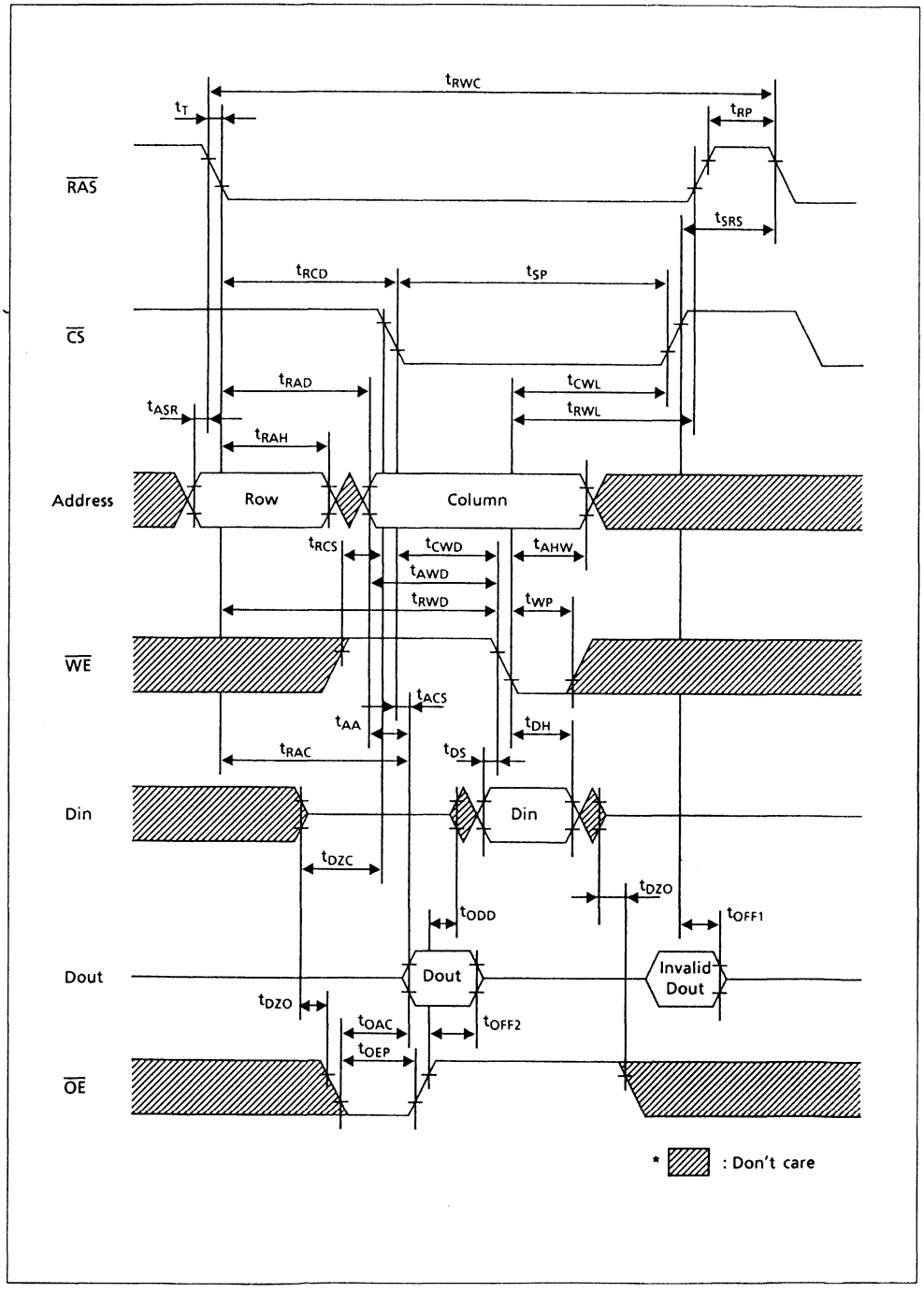
Early Write Cycle



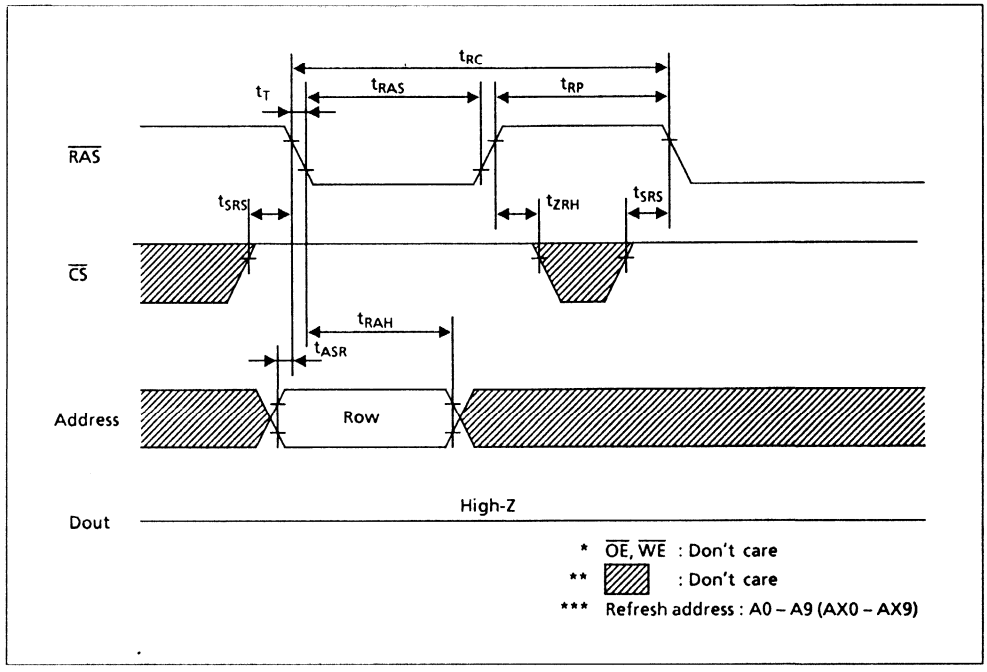
Delayed Write Cycle



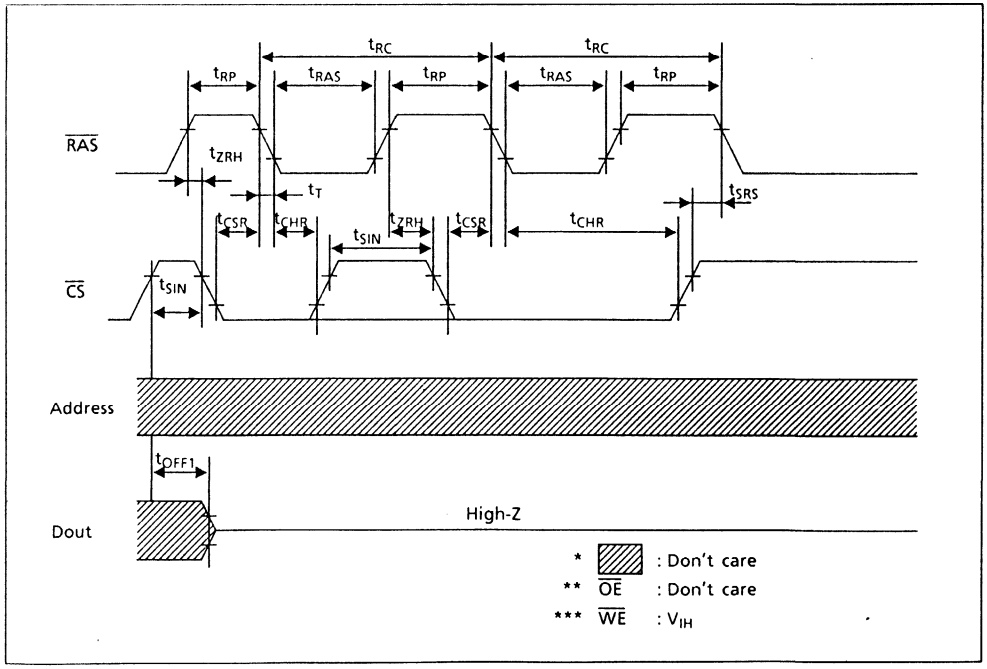
Read-Modify-Write Cycle



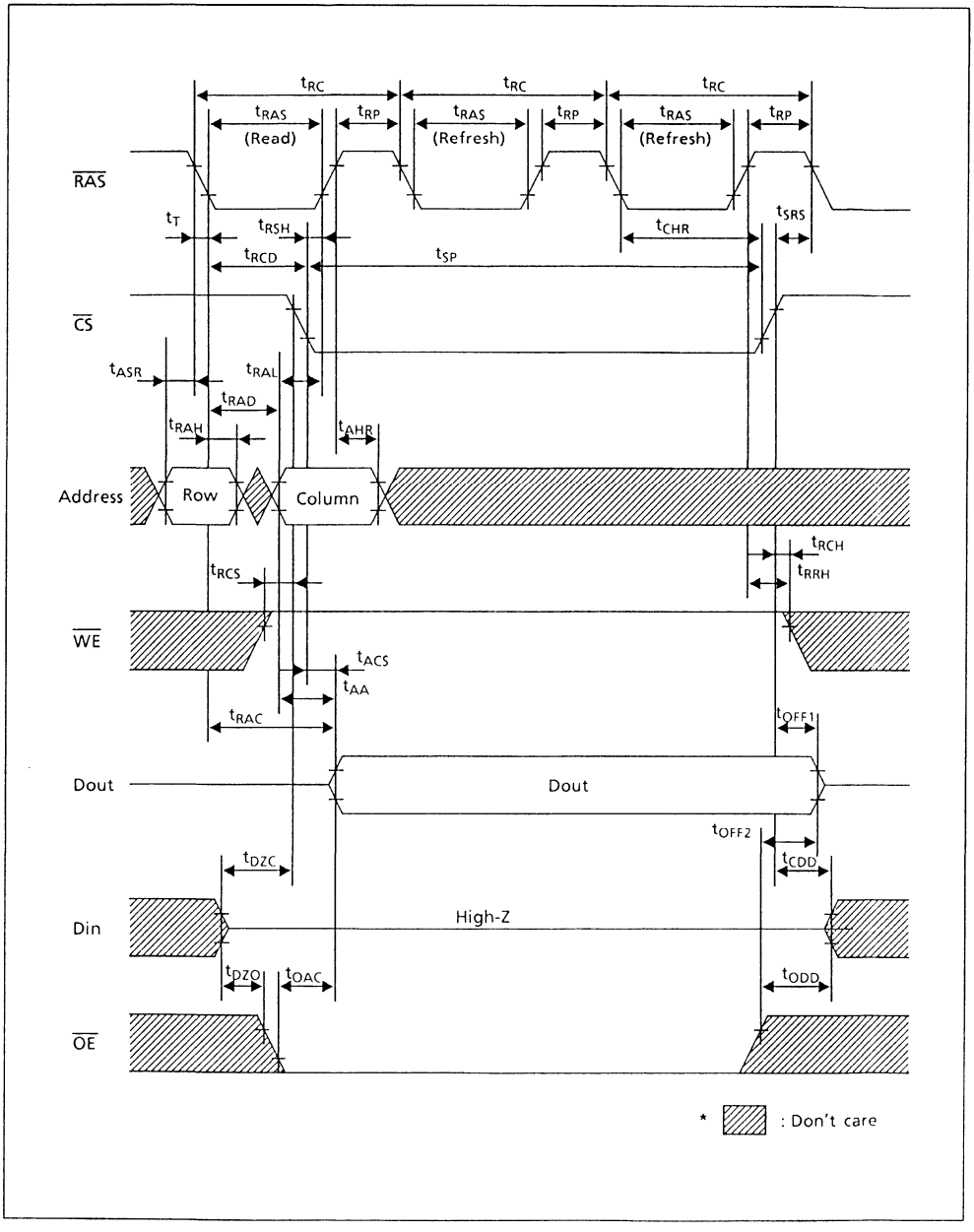
$\overline{RAS}$-Only Refresh Cycle



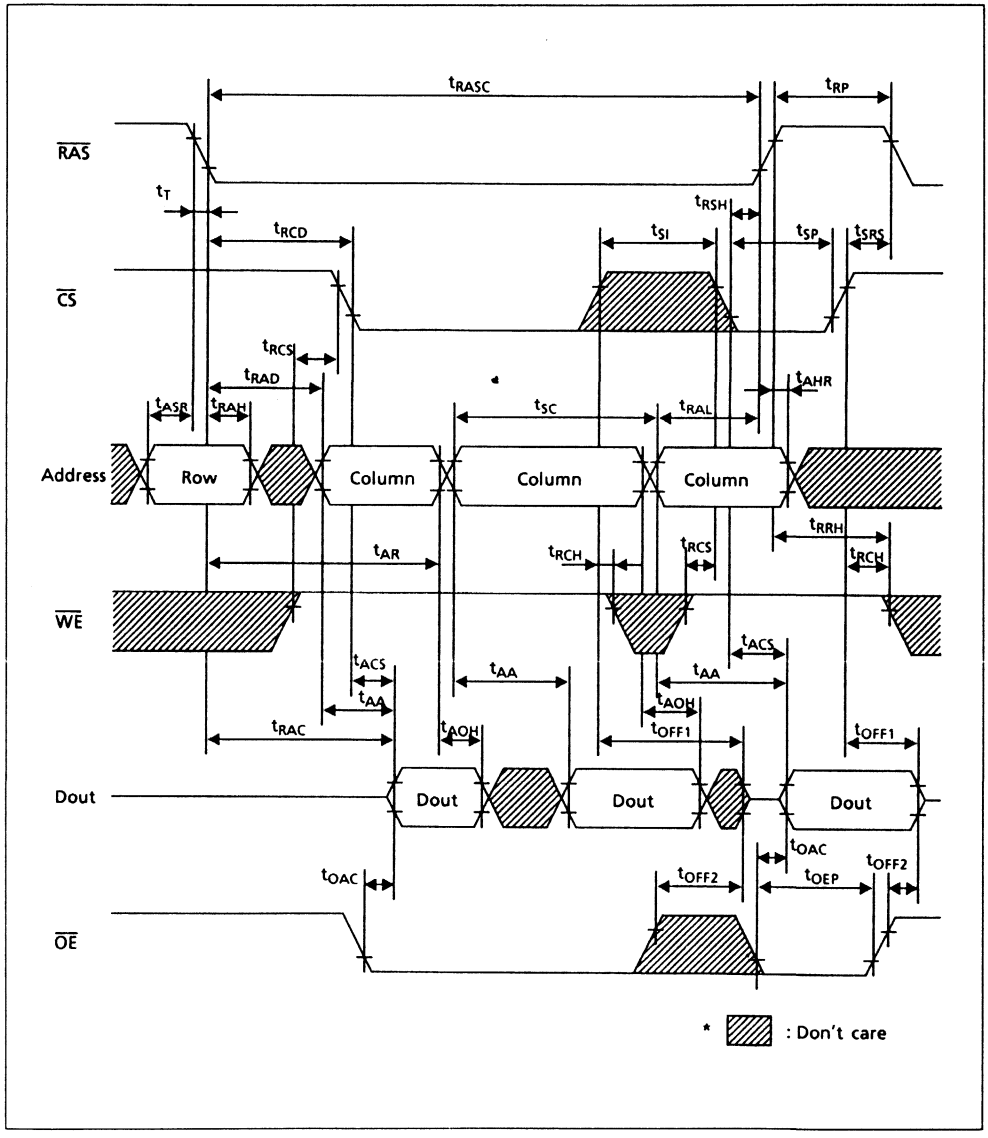
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle



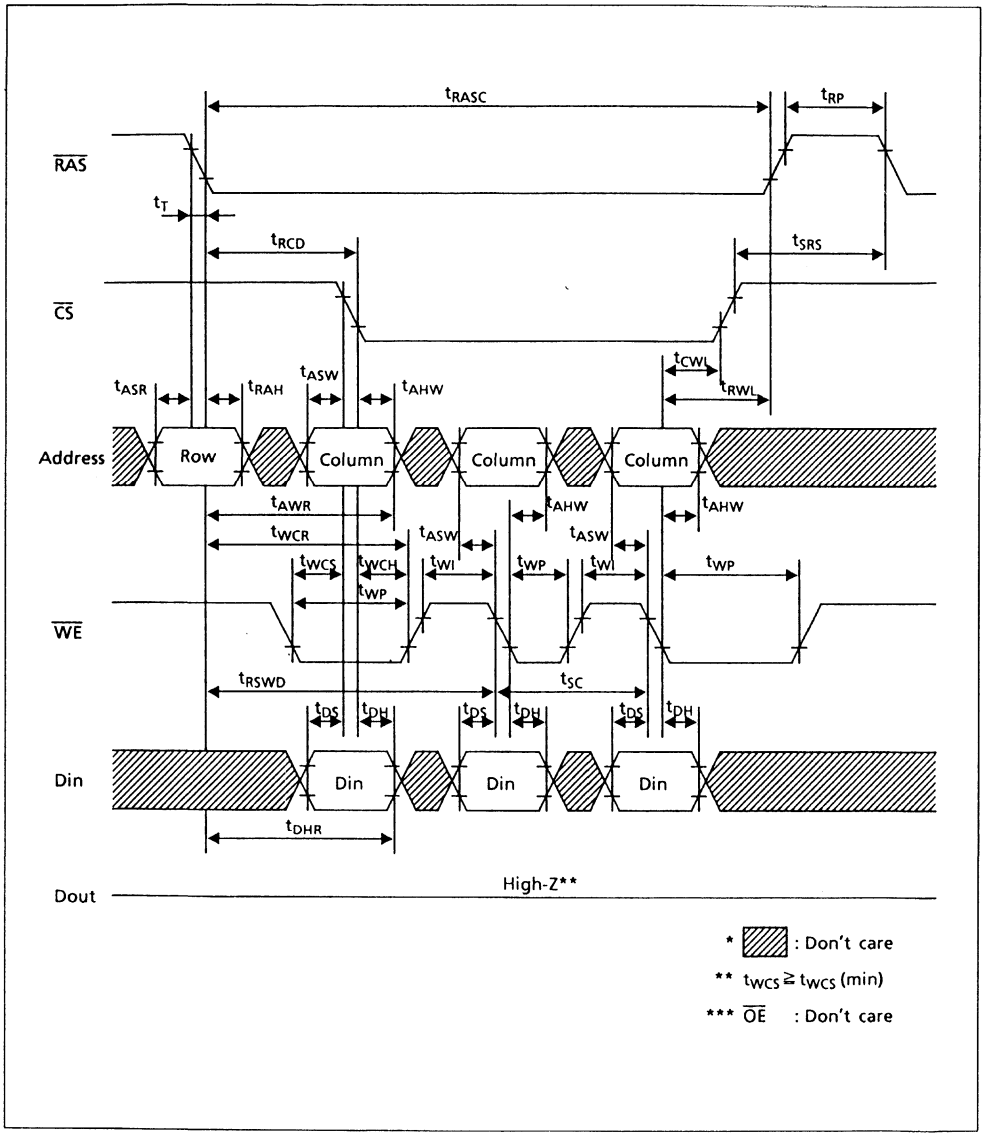
Hidden Refresh Cycle



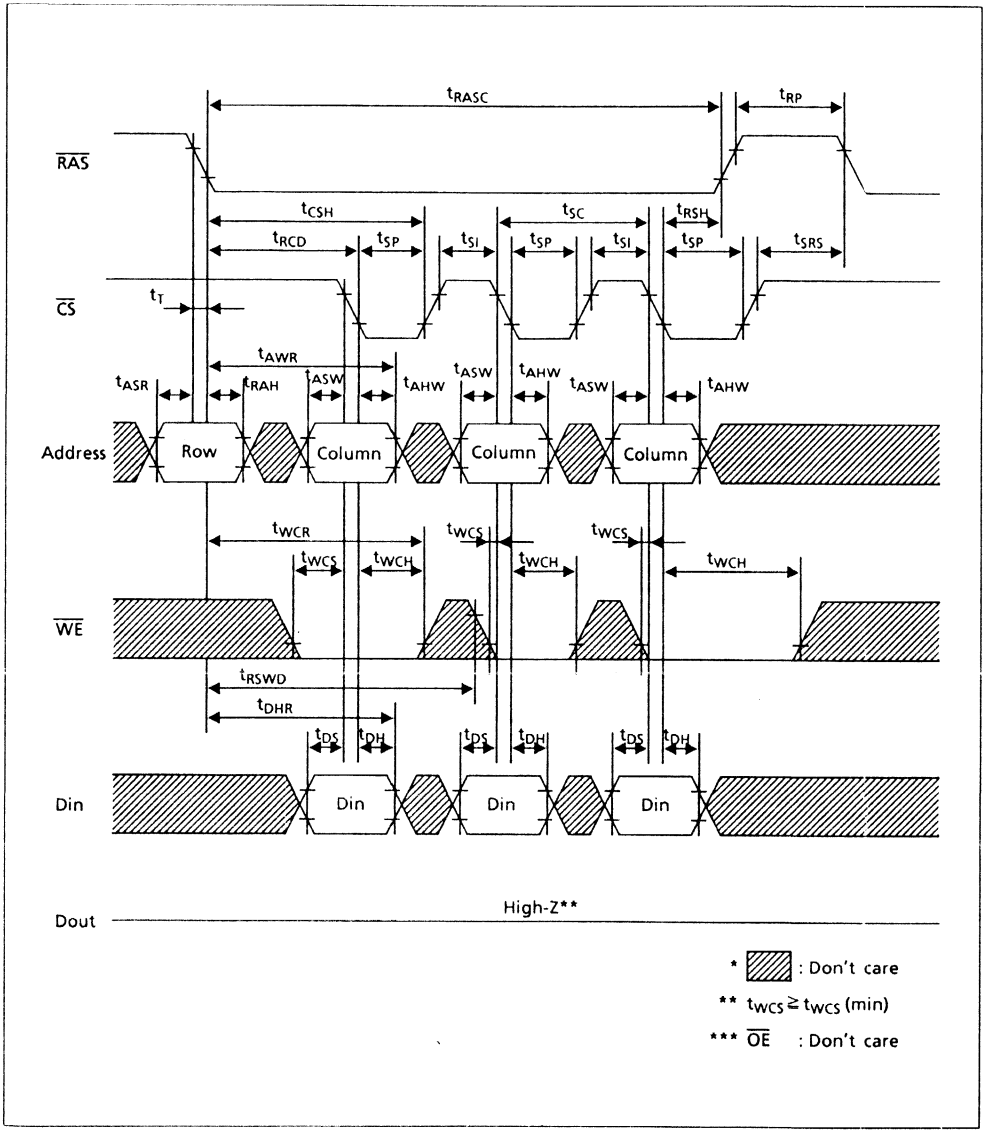
Static Column Mode Read Cycle



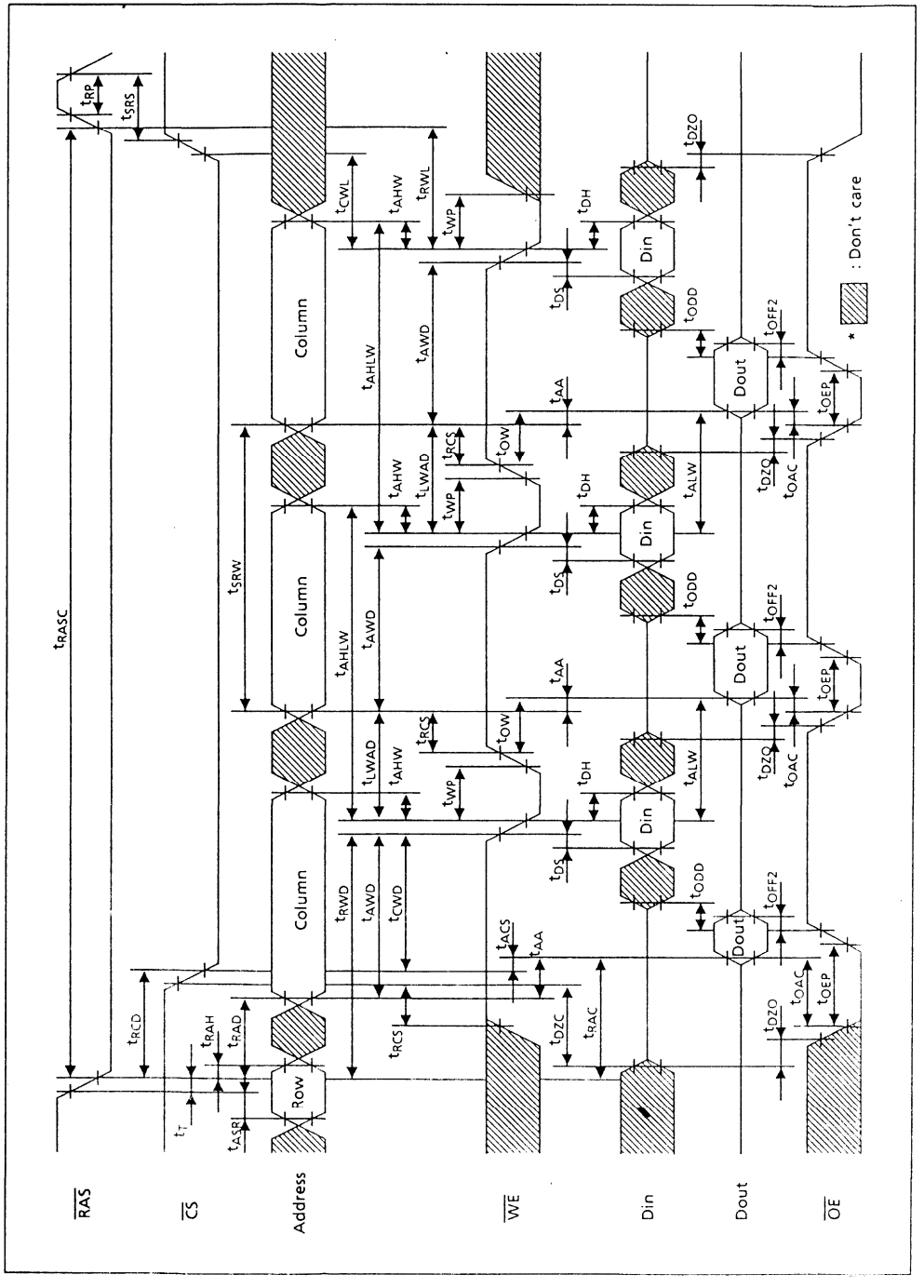
Static Column Mode Write Cycle (1)



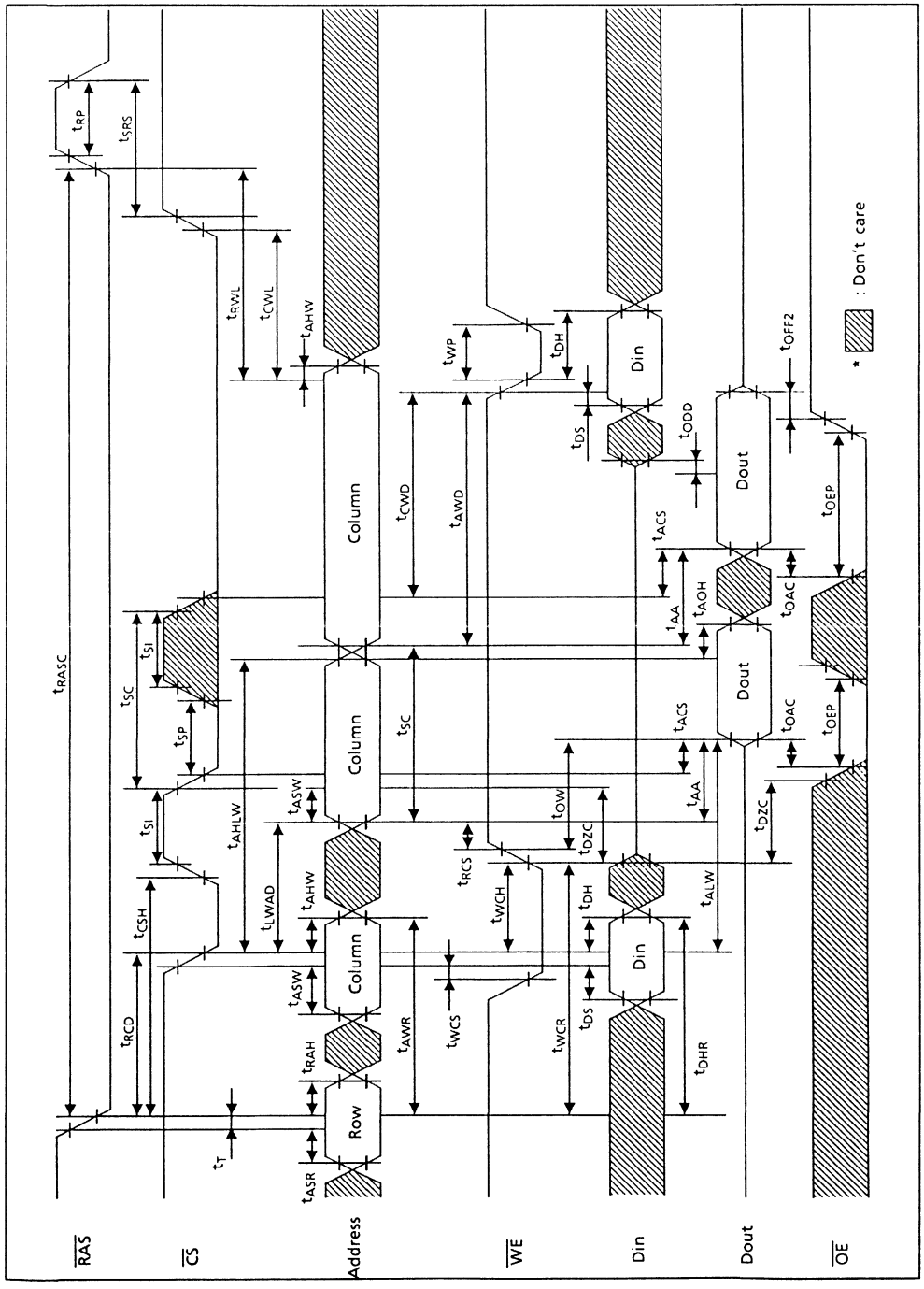
Static Column Mode Write Cycle (2)



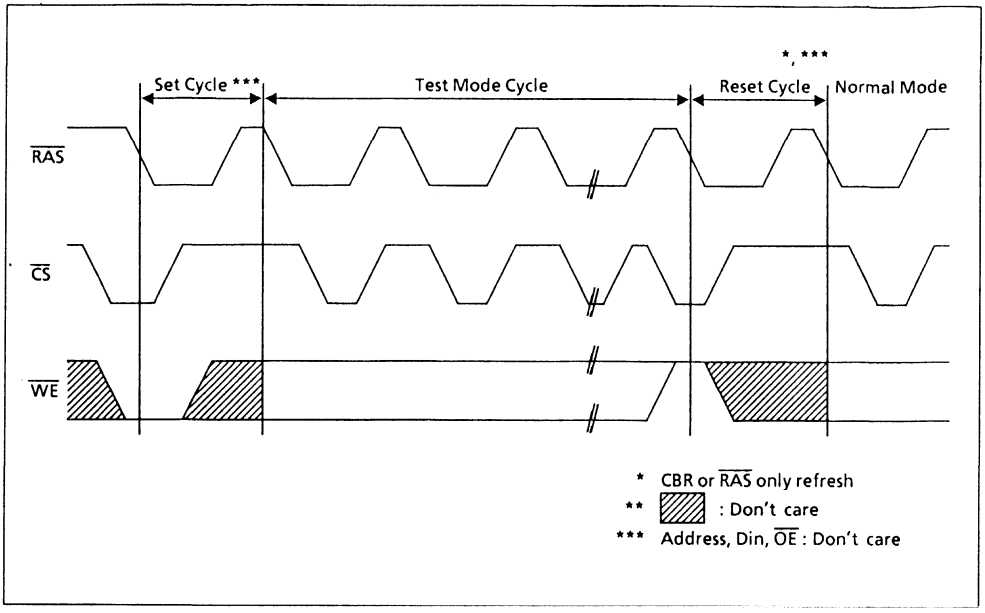
Static Column Mode Read-Modify-Write Cycle



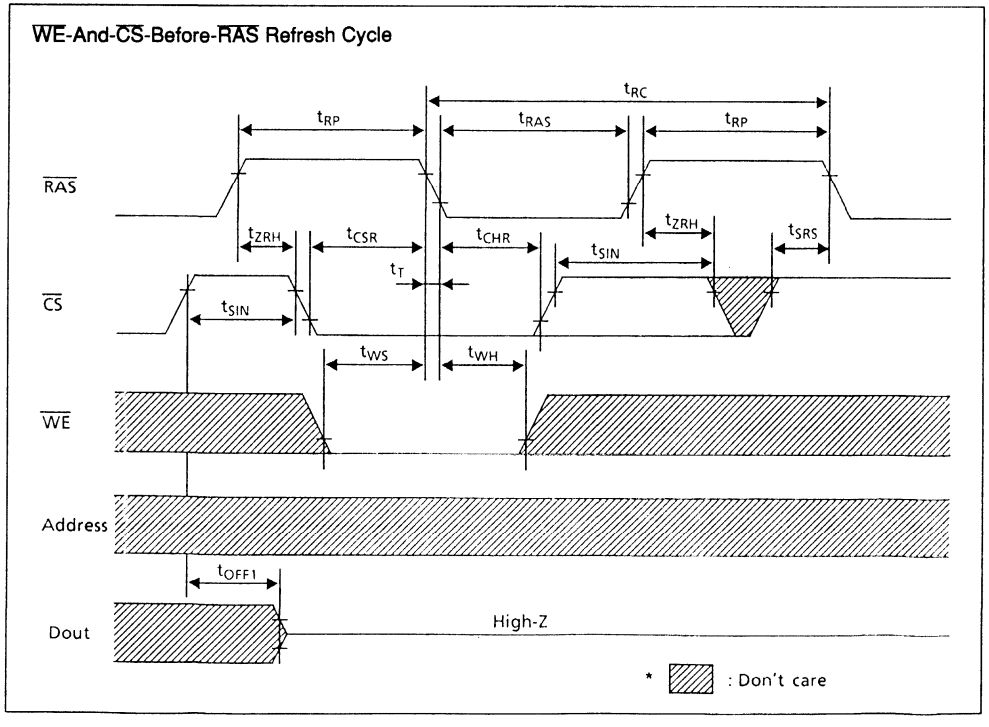
Static Column Mode Mixed Cycle



Test Mode Cycle

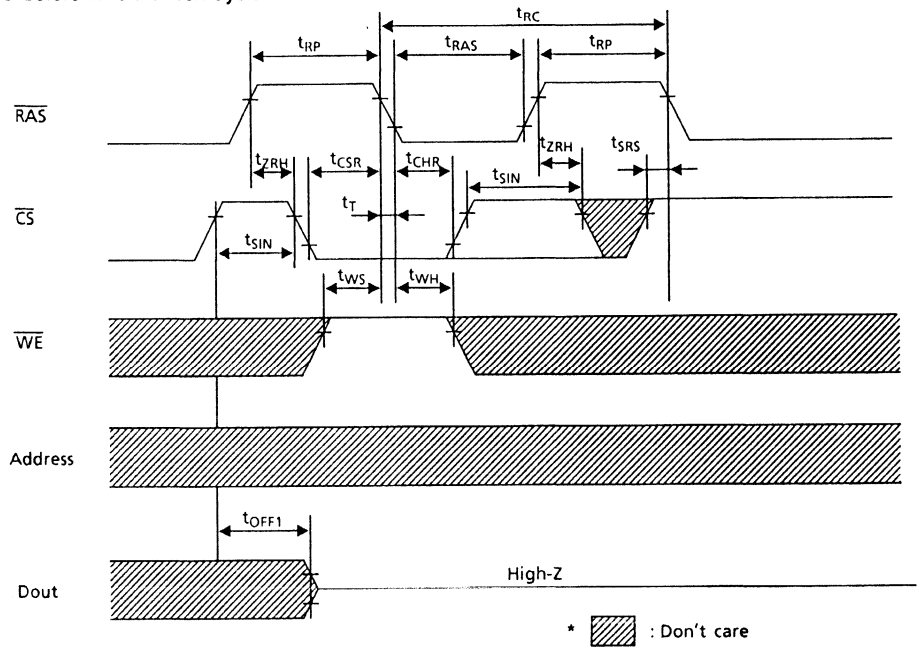


Test Mode Set Cycle

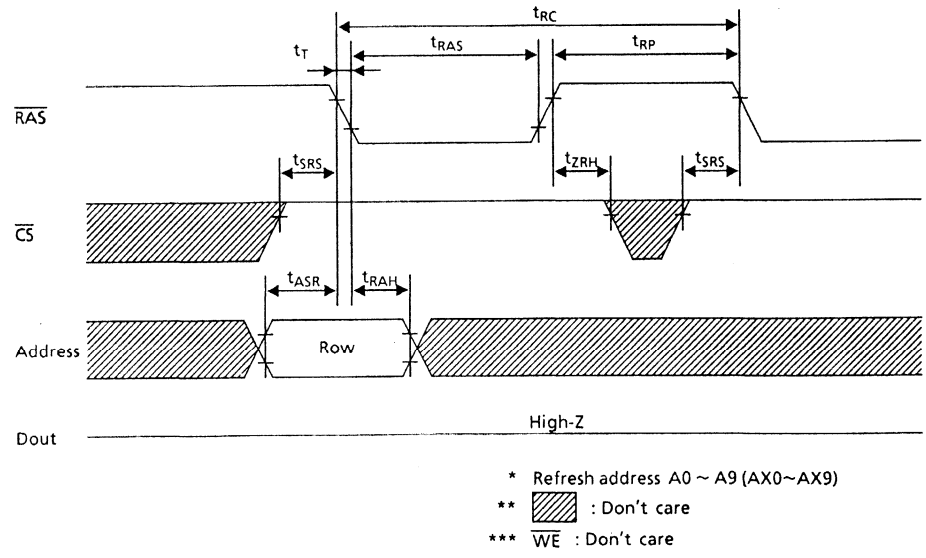


Test Mode Reset Cycle

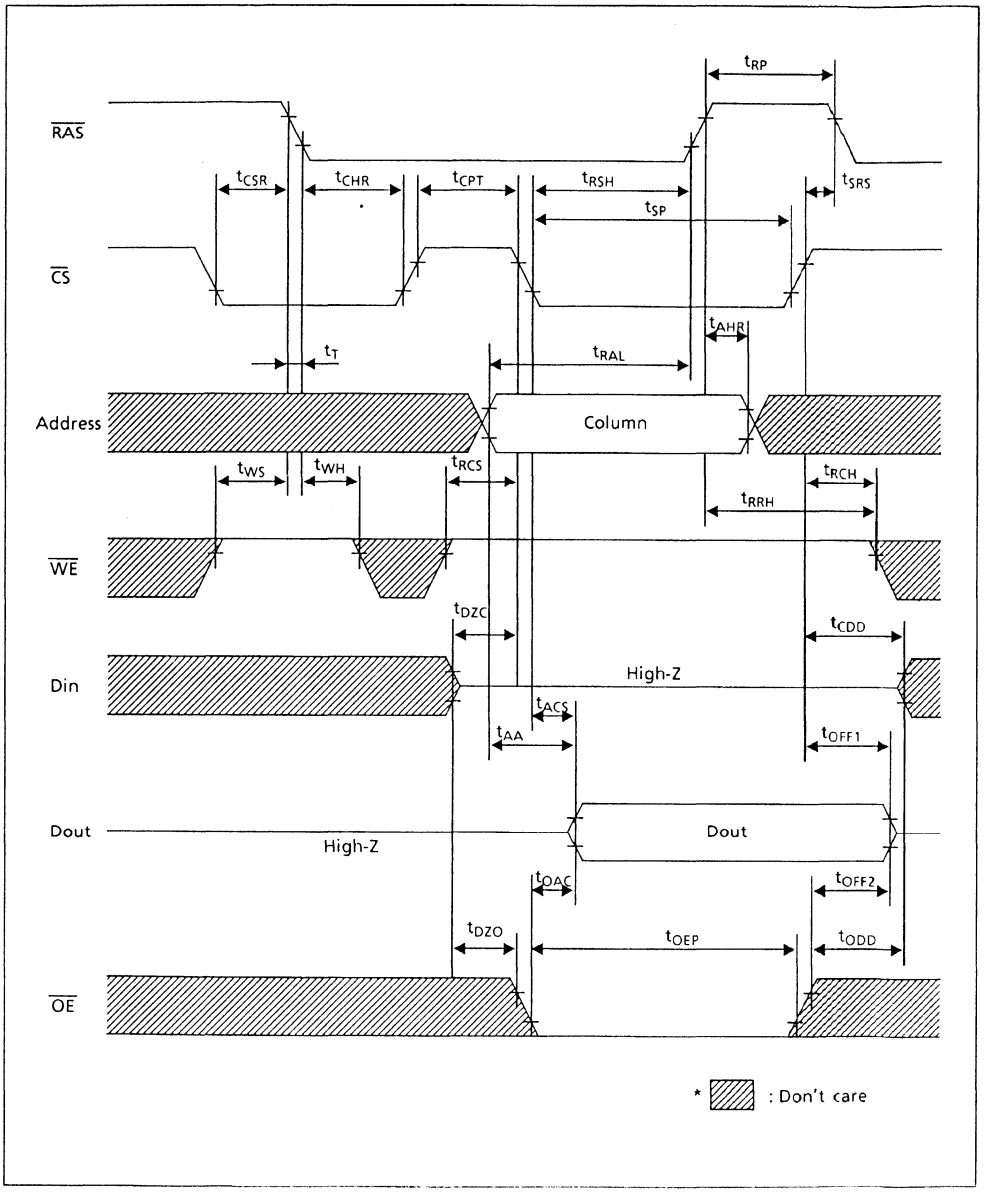
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle



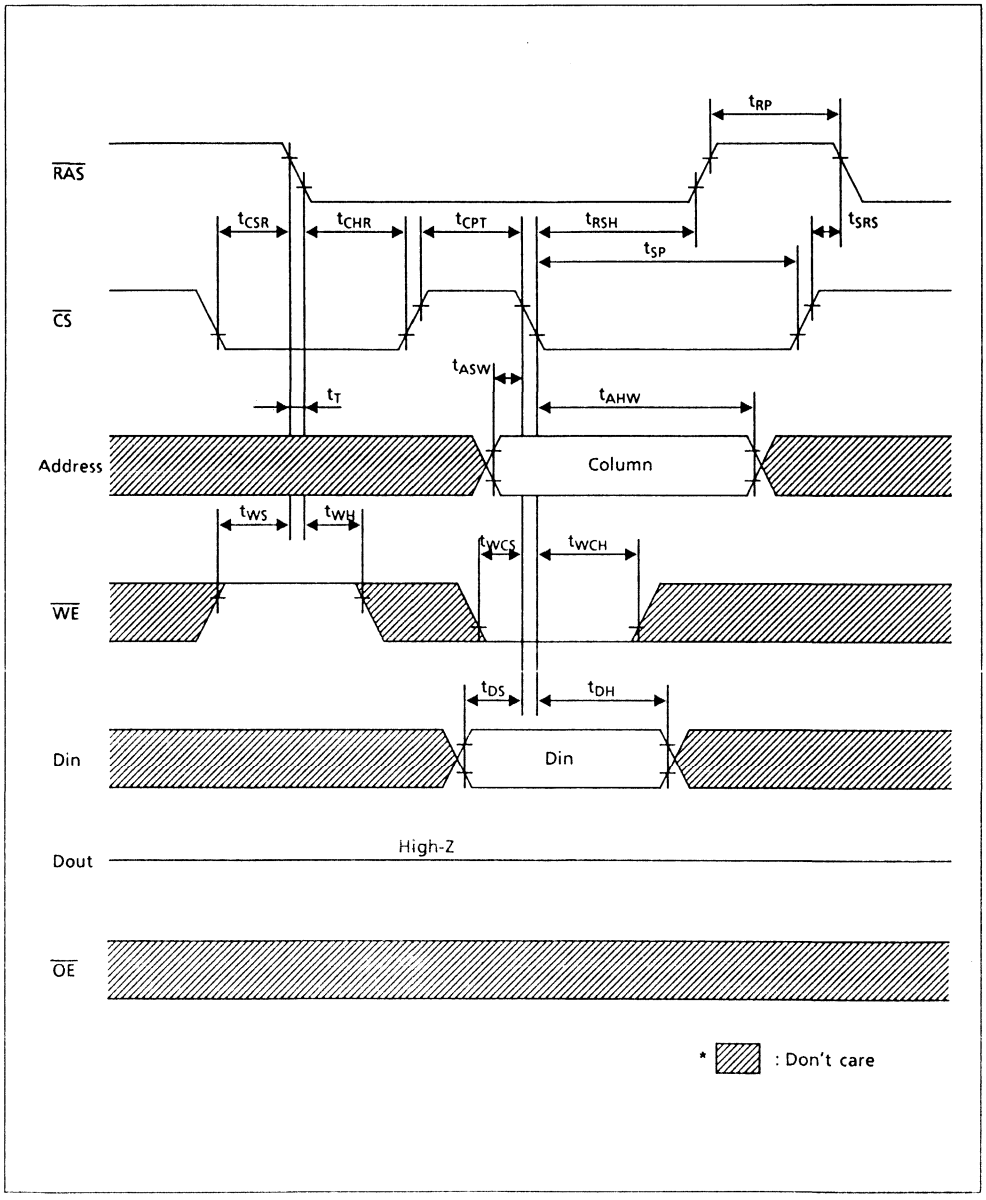
$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514410 Series — Preliminary

1,048,576-Word × 4-Bit Dynamic RAM

The Hitachi HM514410 is a CMOS dynamic RAM organized 1,048,576-word × 4–bit. HM514410 has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514410 offers fast page mode as a high speed access mode.

Multiplexed address input permits the HM514410 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Features

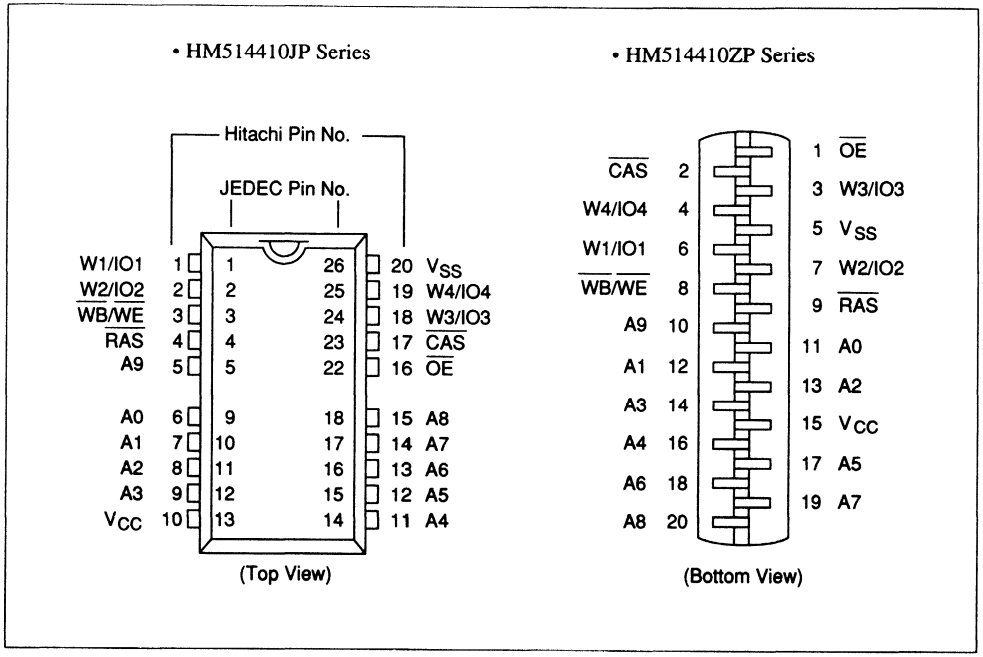
- Single 5 V (± 10%)
- High speed
  - Access time: 80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 495 mW/440 mW/385 mW (max)
  - Standby mode: 11 mW (max)
- Fast page mode capabillity
- 1,024 refresh cycle: 16 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function
- Write per bit capability

Ordering Information

Type No.	Access time	Package
HM514410JP-8	80 ns	350-mil 20-pin plastic SOJ (CP-20DA)
HM514410JP-10	100 ns	
HM514410JP-12	120 ns	
HM514410ZP-8	80 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514410ZP-10	100 ns	
HM514410ZP-12	120 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

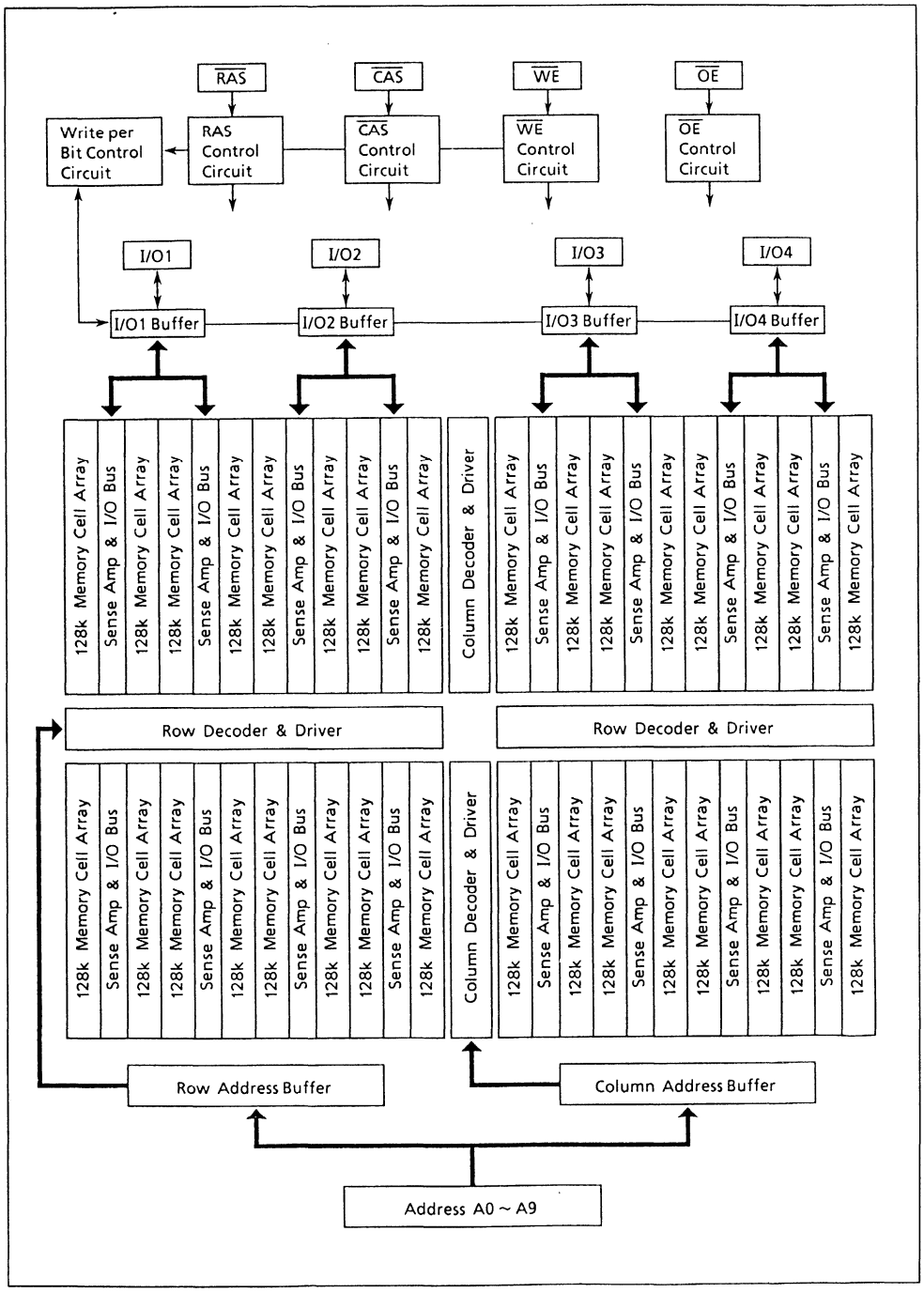
Pin Arrangement



Pin Description

Pin Name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
W1/IO1 – W4/IO4	Write select/data-in/data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WB/WE}$	Write per bit/write enable
$\overline{OE}$	Output enable
V_{CC}	Power (+5 V)
V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage		V_{SS}	0	0	0	V	
		V_{CC}	4.5	5.0	5.5	V	1
Input high voltage		V_{IH}	2.4	—	6.5	V	1
Input low voltage	(W/IO pin)	V_{IL}	−1.0	—	0.8	V	1
	(Others)	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514410								
		-8		-10		-12				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2 V Dout = High-Z	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514410								
		-8		-10		-12				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1, 4
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	4
Fast page mode current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = −5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, data-out)	$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *14, *15, *16

Test Conditions

- Input rise and fall times: 5ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate +C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	10	—	10	—	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	20	—	25	—	30	—	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{CAS}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 17
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 13, 17
Access time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 13, 16, 17
Access time from $\overline{OE}$	t_{OAC}	—	25	—	25	—	30	ns	17
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	20
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	20
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF1}	0	20	0	25	0	30	ns	6
Output buffer turn-off to $\overline{OE}$	t_{OFF2}	0	20	0	25	0	30	ns	6
$\overline{CAS}$ to Din delay time	t_{CDD}	20	—	25	—	30	—	ns	

Write Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	210	—	245	—	285	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	—	135	—	160	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	55	—	60	—	70	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	70	—	80	—	95	—	ns	10
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	25	—	25	—	30	—	ns	

Refresh Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time (normal mode)	t_{CPN}	10	—	10	—	15	—	ns	

Fast Page Mode Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	3, 13, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode read-modify-write cycle time	t_{PCM}	105	—	110	—	130	—	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	80	—	85	—	100	—	ns	

Test Mode Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	20	—	20	—	20	—	ns	

Counter Test Cycle

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	50	—	60	—	ns	

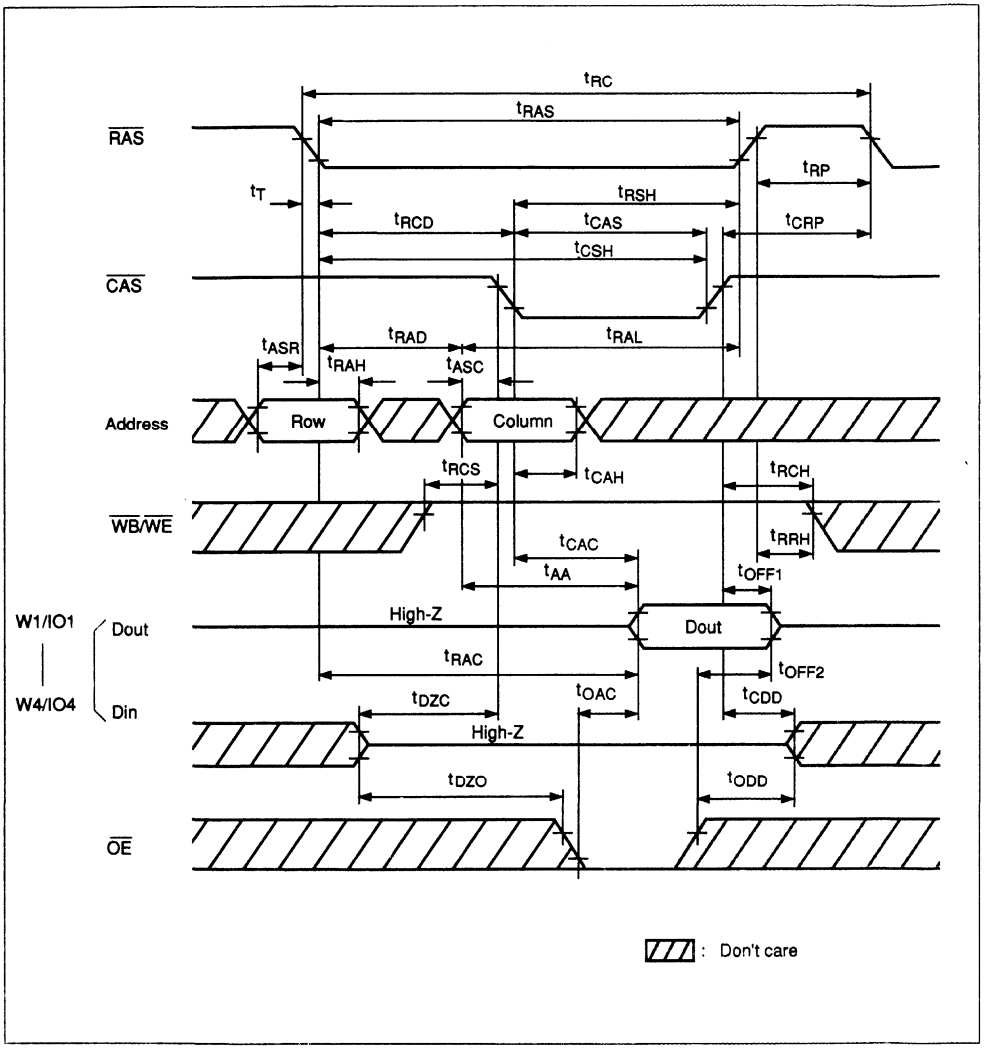
Write Per Bit *18, *19

		HM514410							
		-8		-10		-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write per bit setup time	t_{WBS}	0	—	0	—	0	—	ns	
Write per bit hold time	t_{WBH}	12	—	15	—	15	—	ns	
Write per bit selection setup time	t_{WDS}	0	—	0	—	0	—	ns	
Write per bit selection hold time	t_{WDH}	12	—	15	—	15	—	ns	

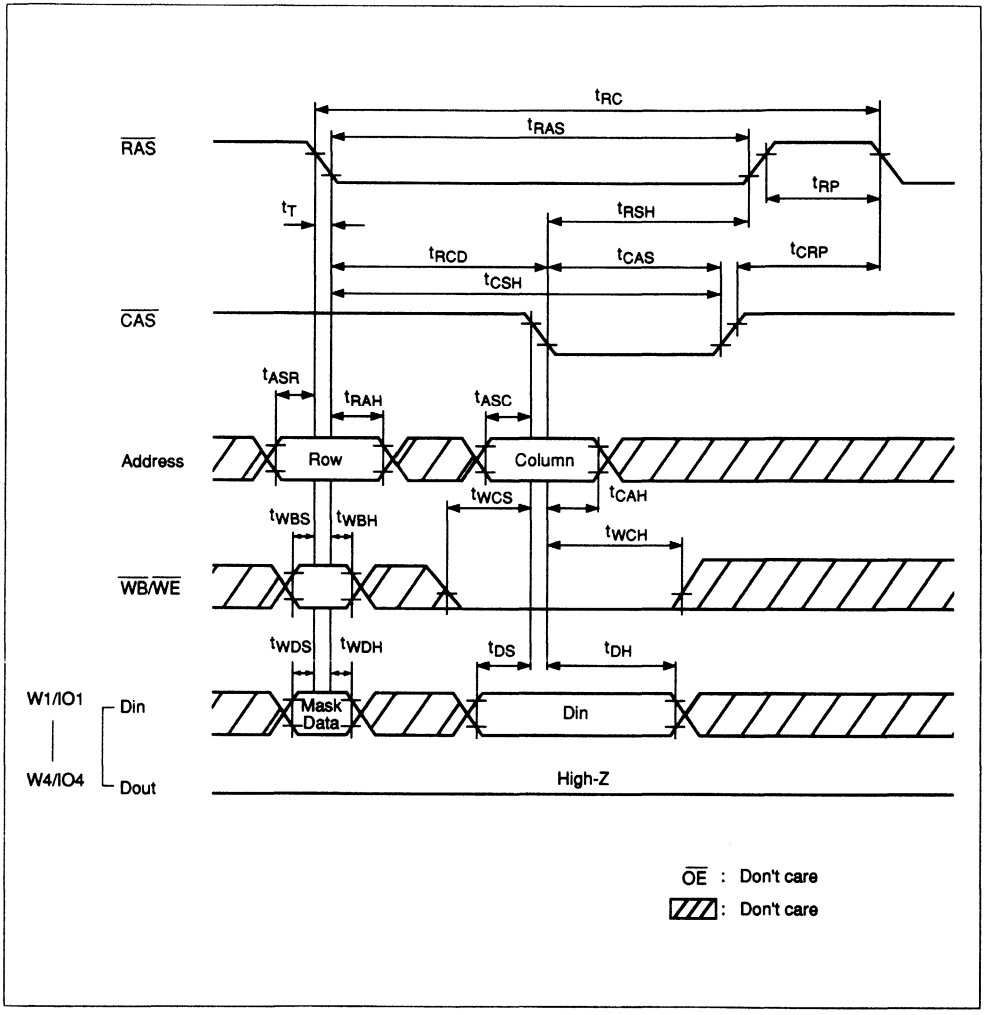
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before -$\overline{RAS}$ refresh cycles is required. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is I/O3 and data input pin is I/O2. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{CAC}, t_{AA}, t_{OAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. When using the write-per-bit capability, $\overline{WB/WE}$ must be low as $\overline{RAS}$ falls.
19. The data bits to which the write operation is applied can be specified by keeping W1/IO1, W2/IO2, W3/IO3 and W4/IO4 high with setup and hold time referenced to the $\overline{RAS}$ negative transition.
20. Either t_{RCH} or t_{RRH} shall be satisfied.

Timing Waveform

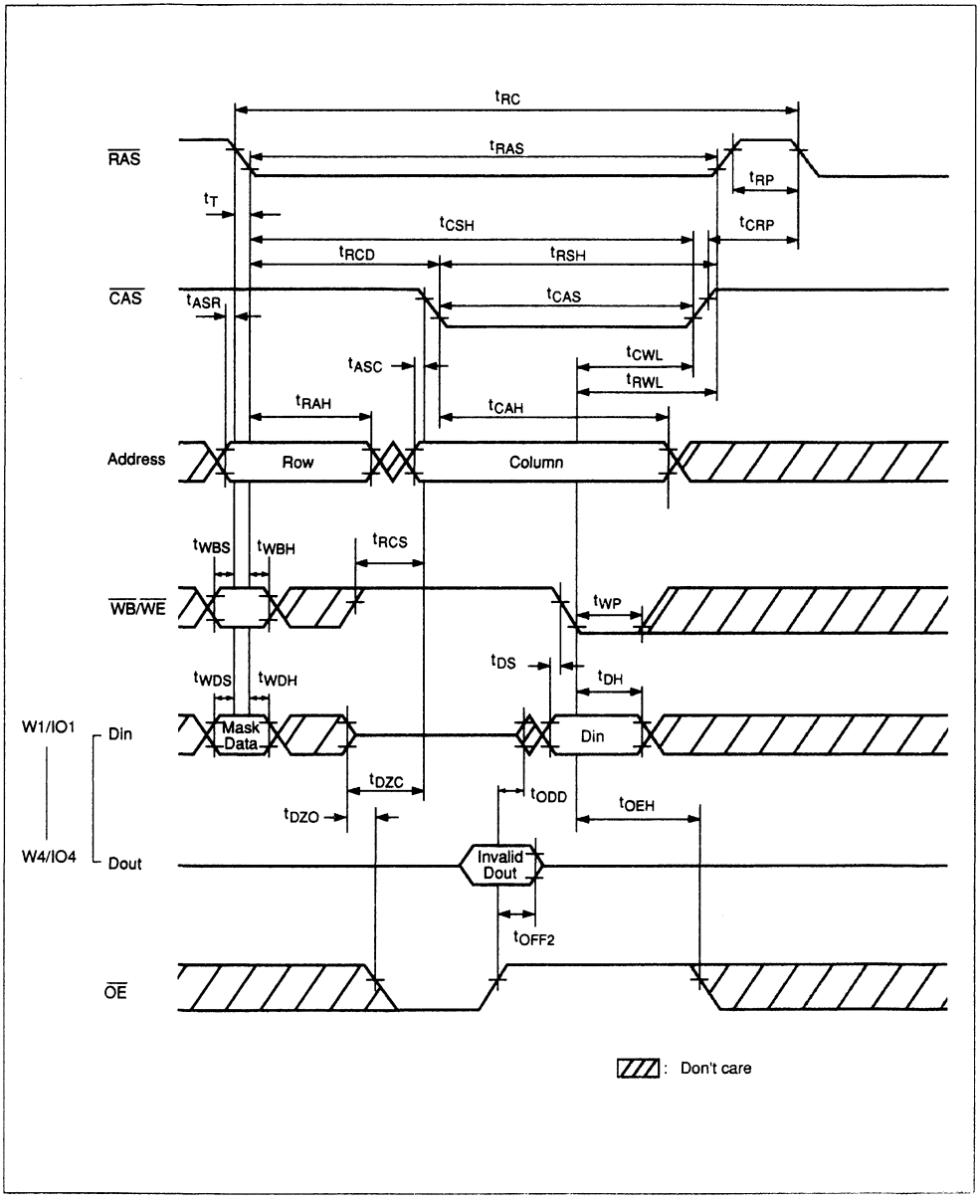
Read Cycle



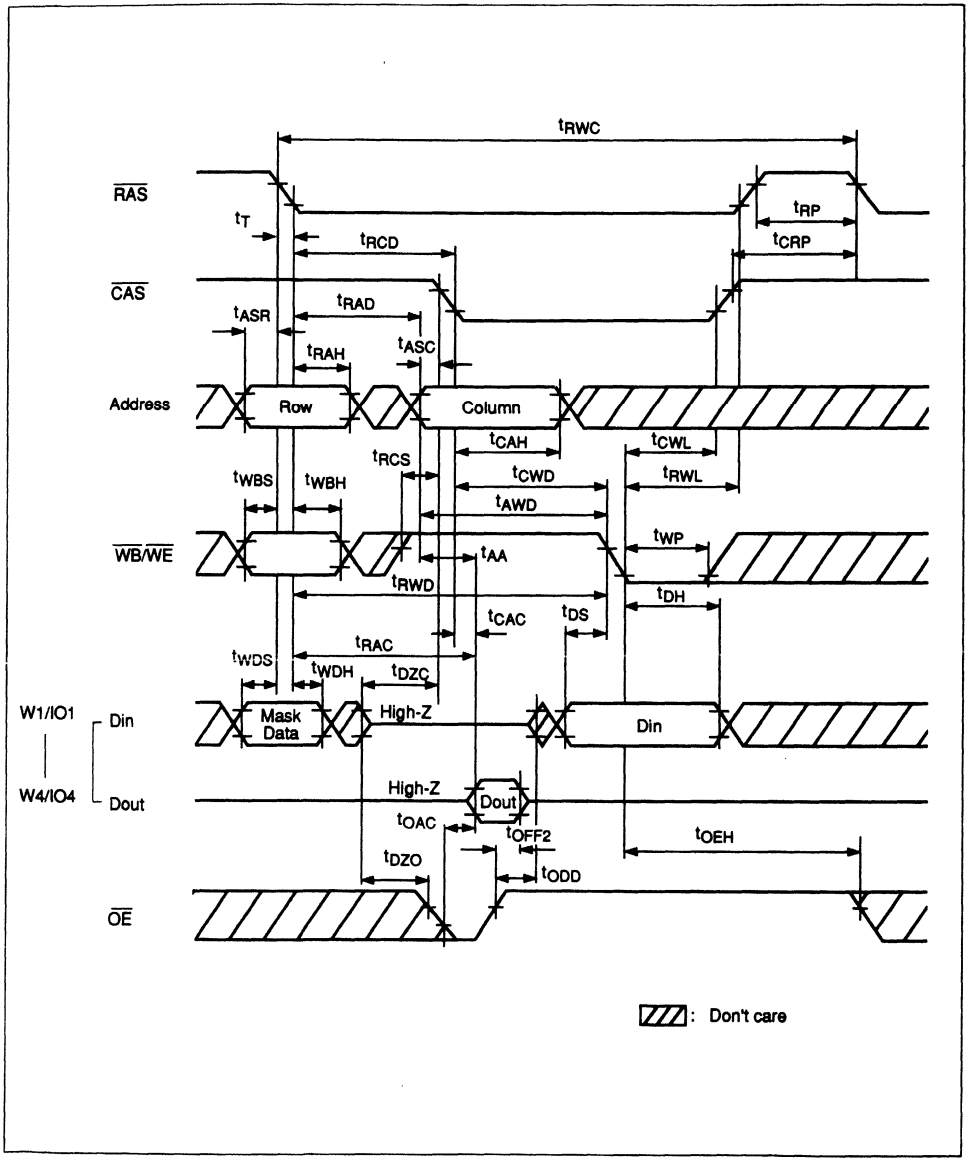
Early Write Cycle



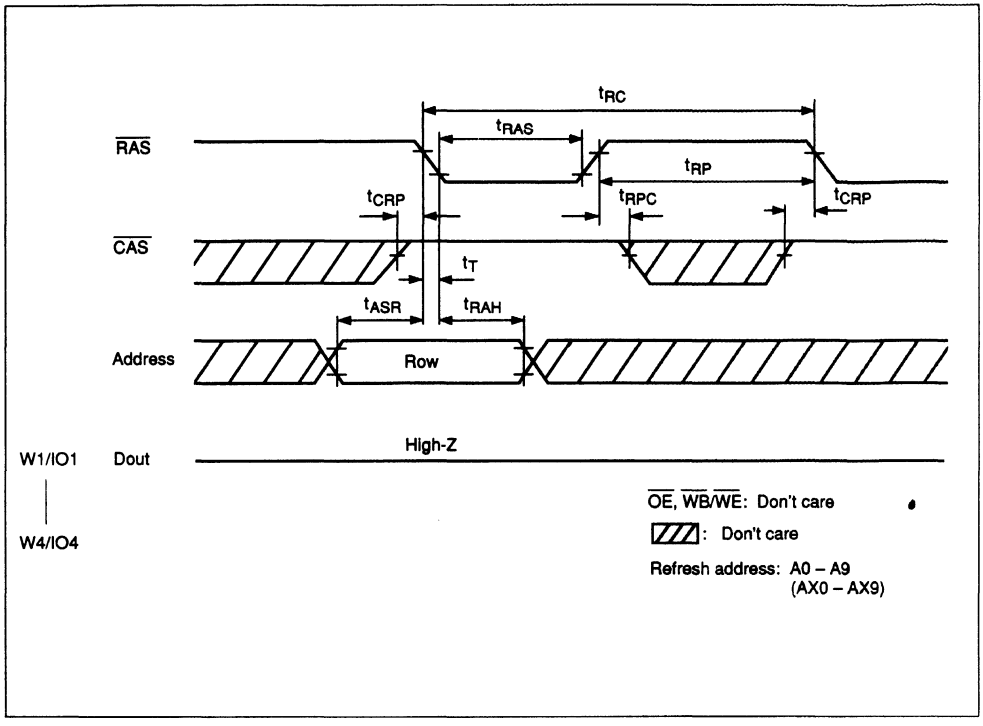
Delayed Write Cycle



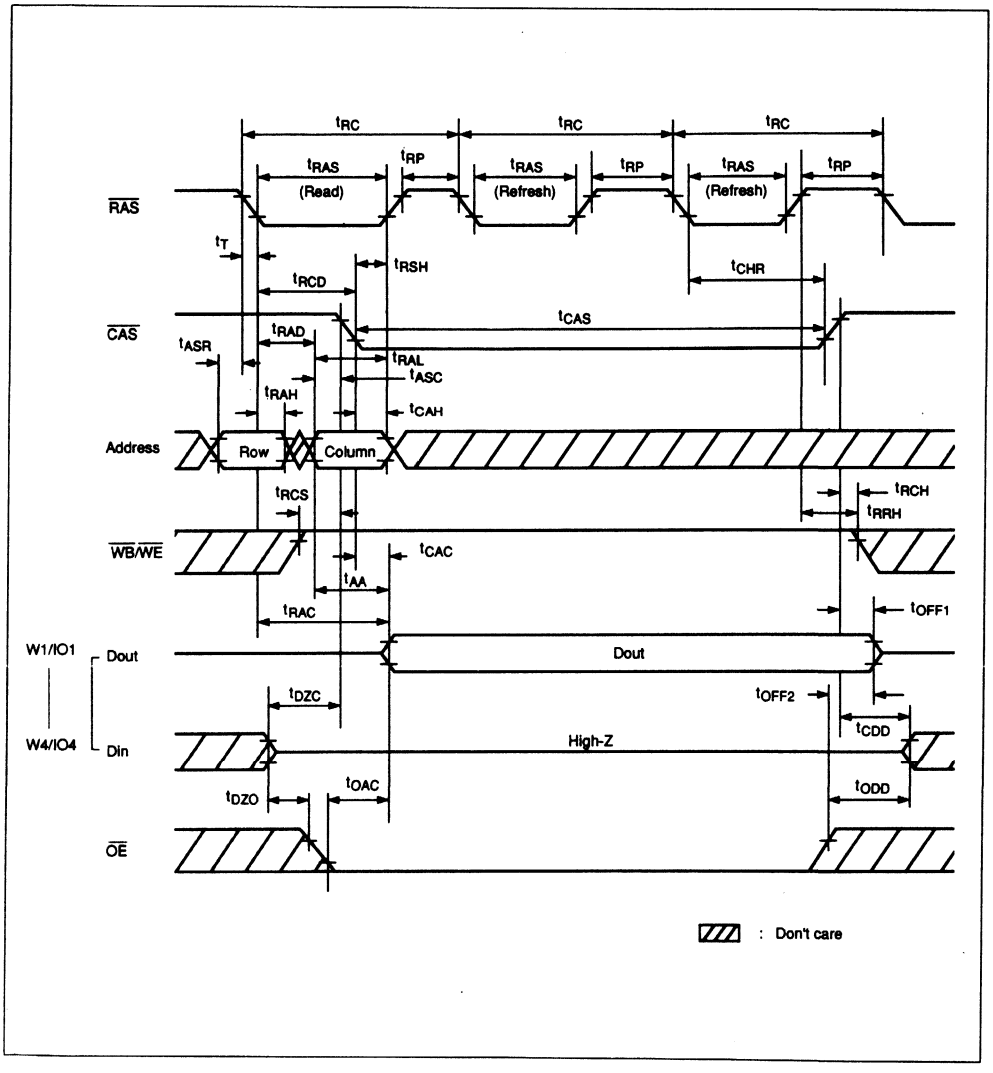
Read-Modify-Write Cycle



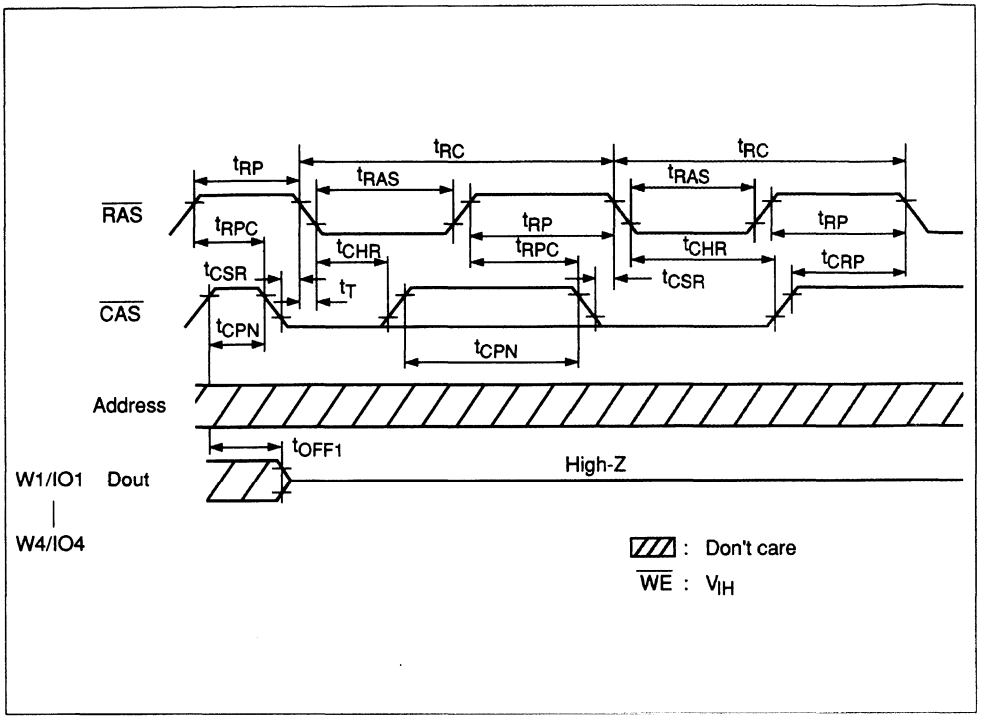
$\overline{RAS}$-Only Refresh Cycle



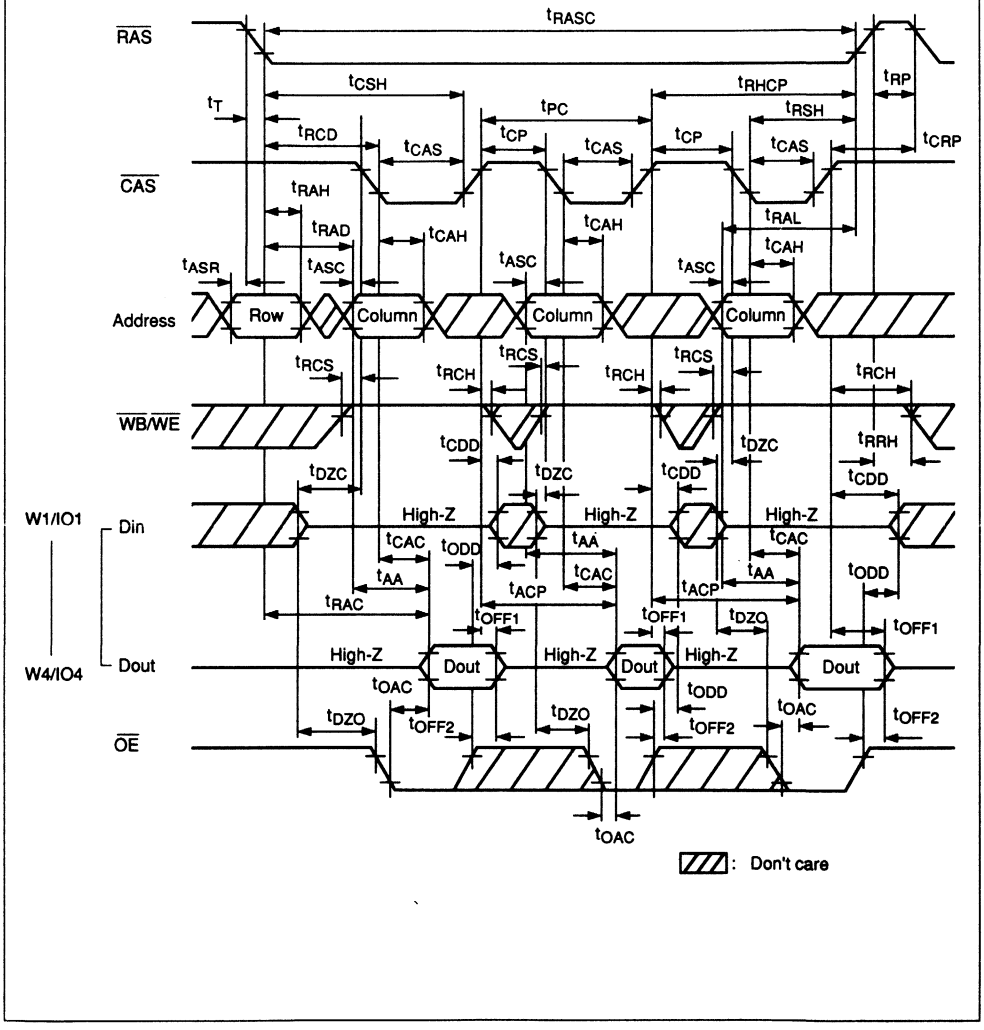
Hidden Refresh Cycle



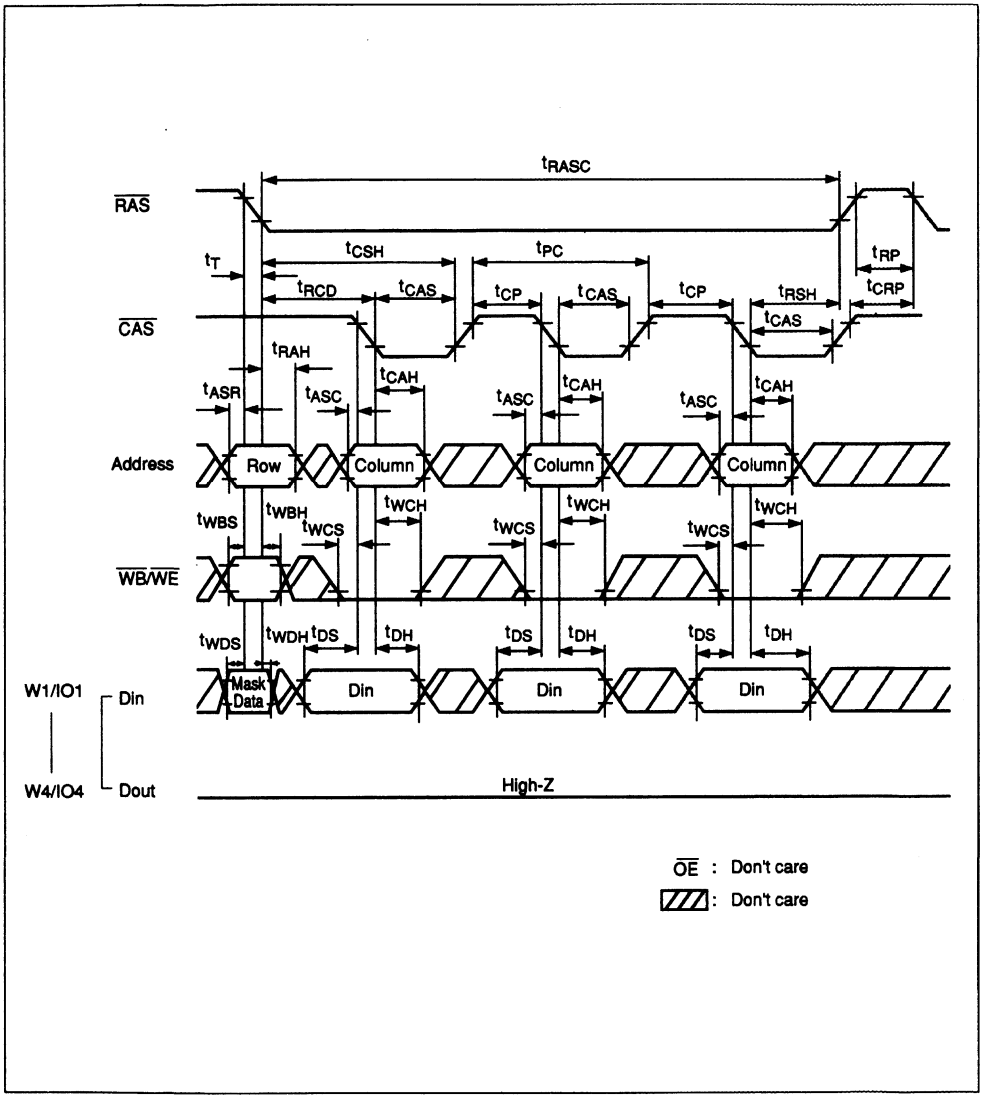
$\overline{CAS}$-Before-$\overline{RAS}$-Refresh Cycle



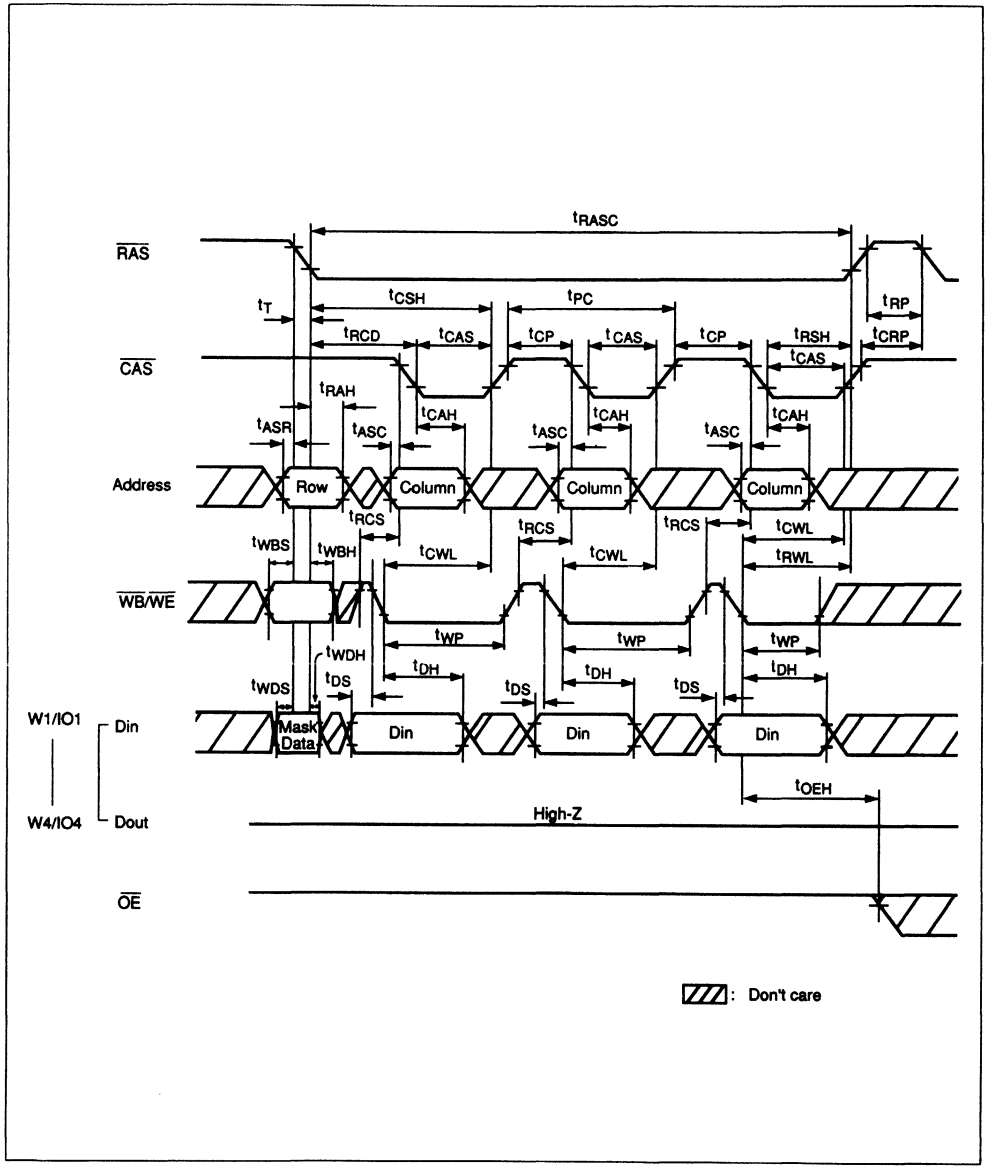
Fast Page Mode Read Cycle



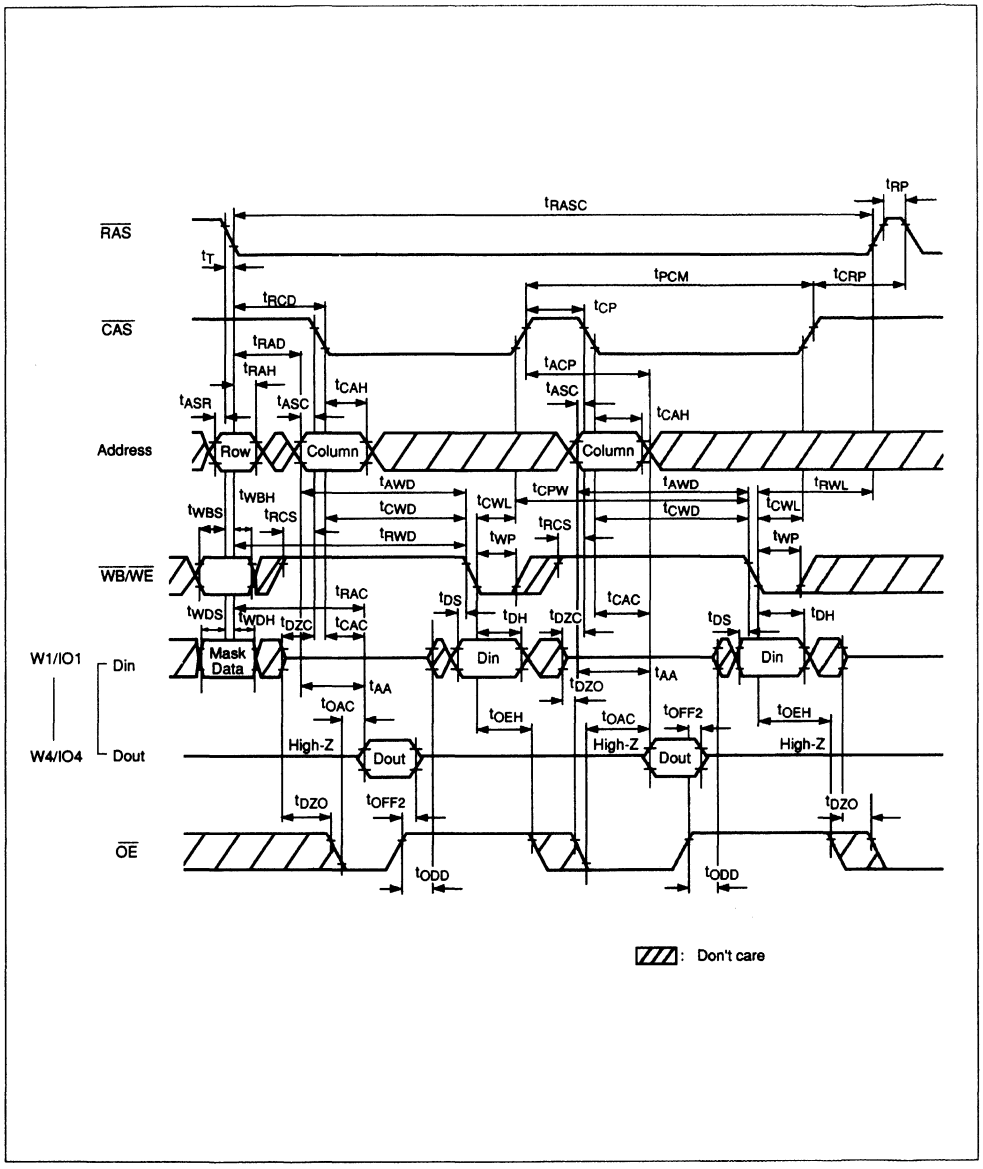
Fast Page Mode Early Write Cycle



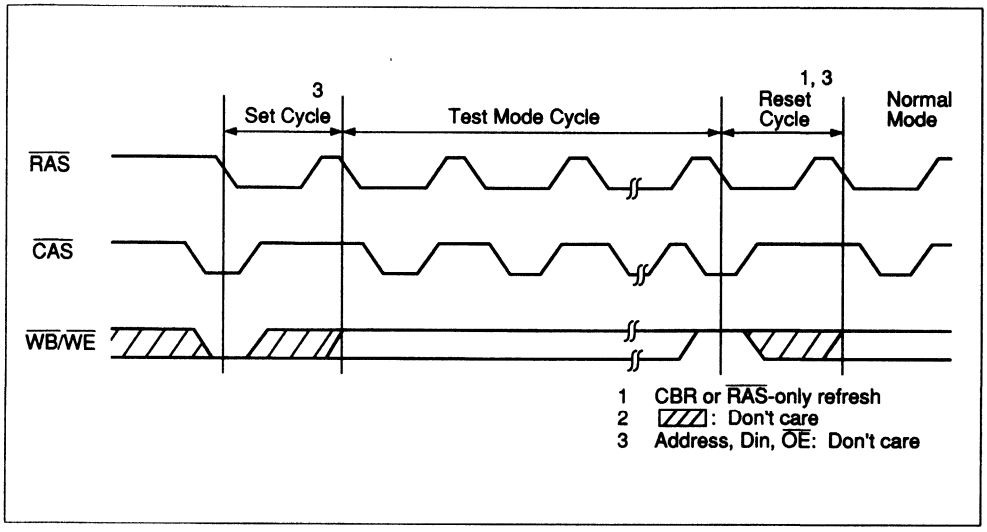
Fast Page Delayed Write Cycle



Fast Page Mode Read-Modify-Write Cycle

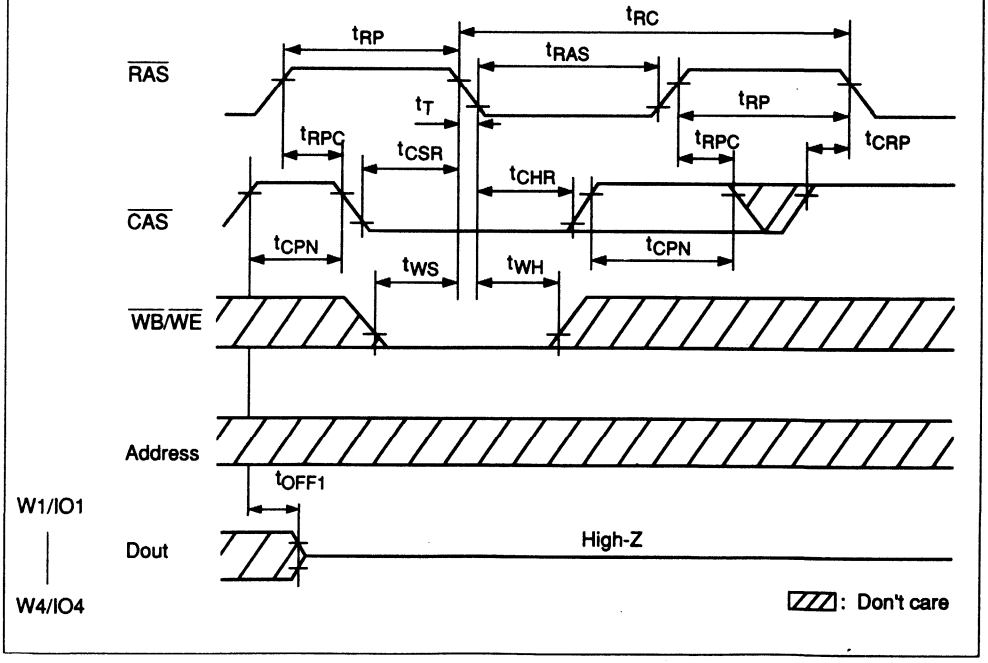


Test Mode Cycle



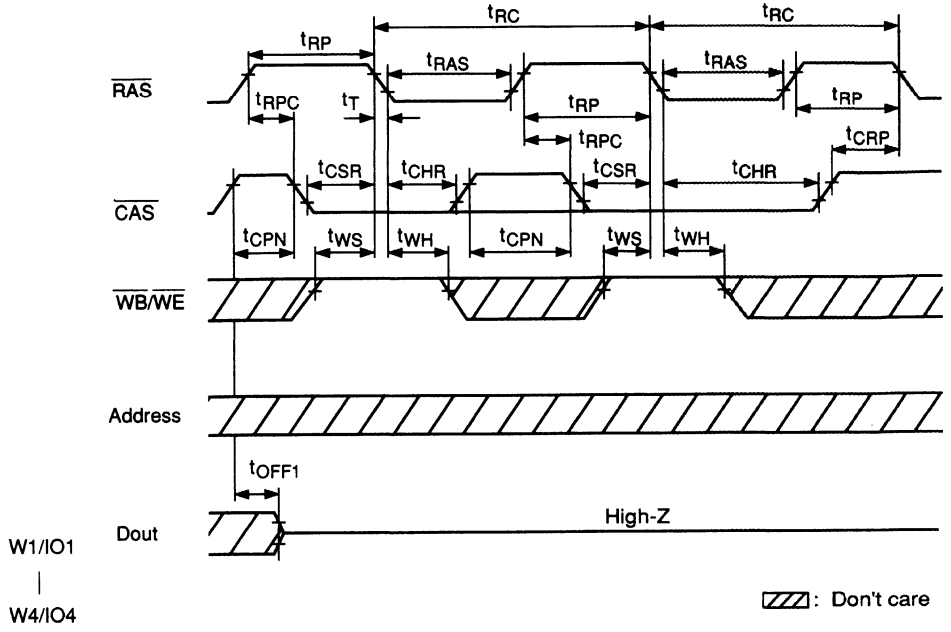
Test Mode Set Cycle

WE-And-CAS-Before-RAS Refresh Cycle

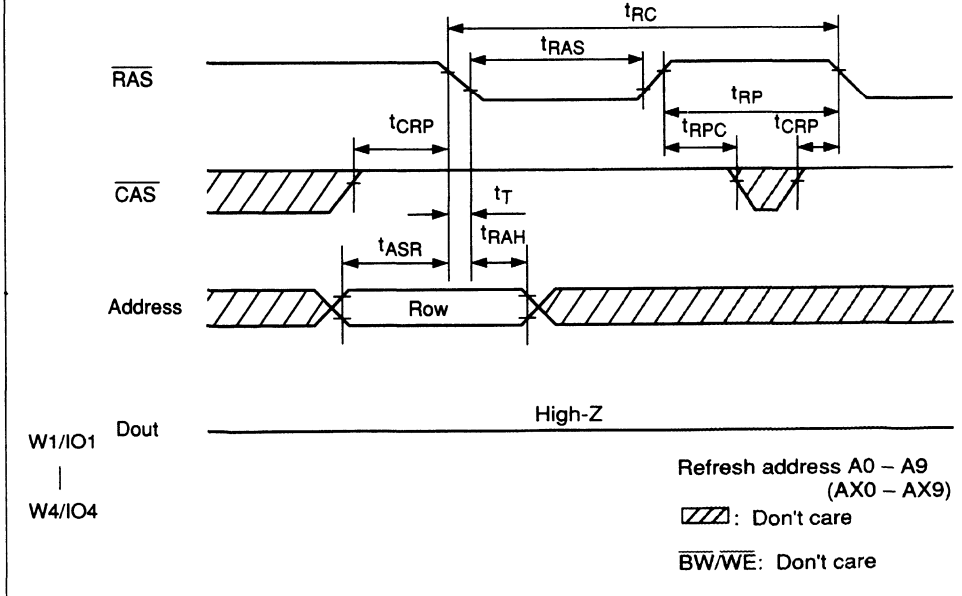


Test Mode Reset Cycle

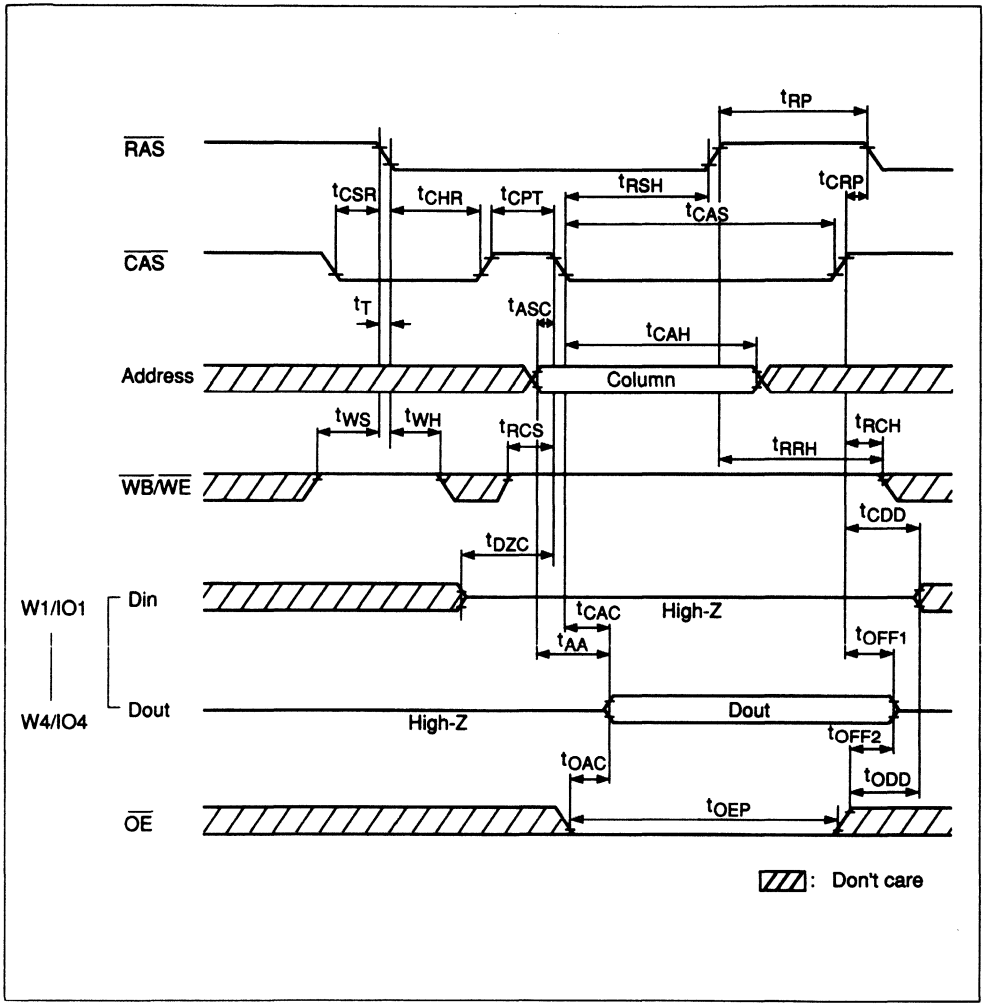
CAS-Before-RAS Refresh Cycle



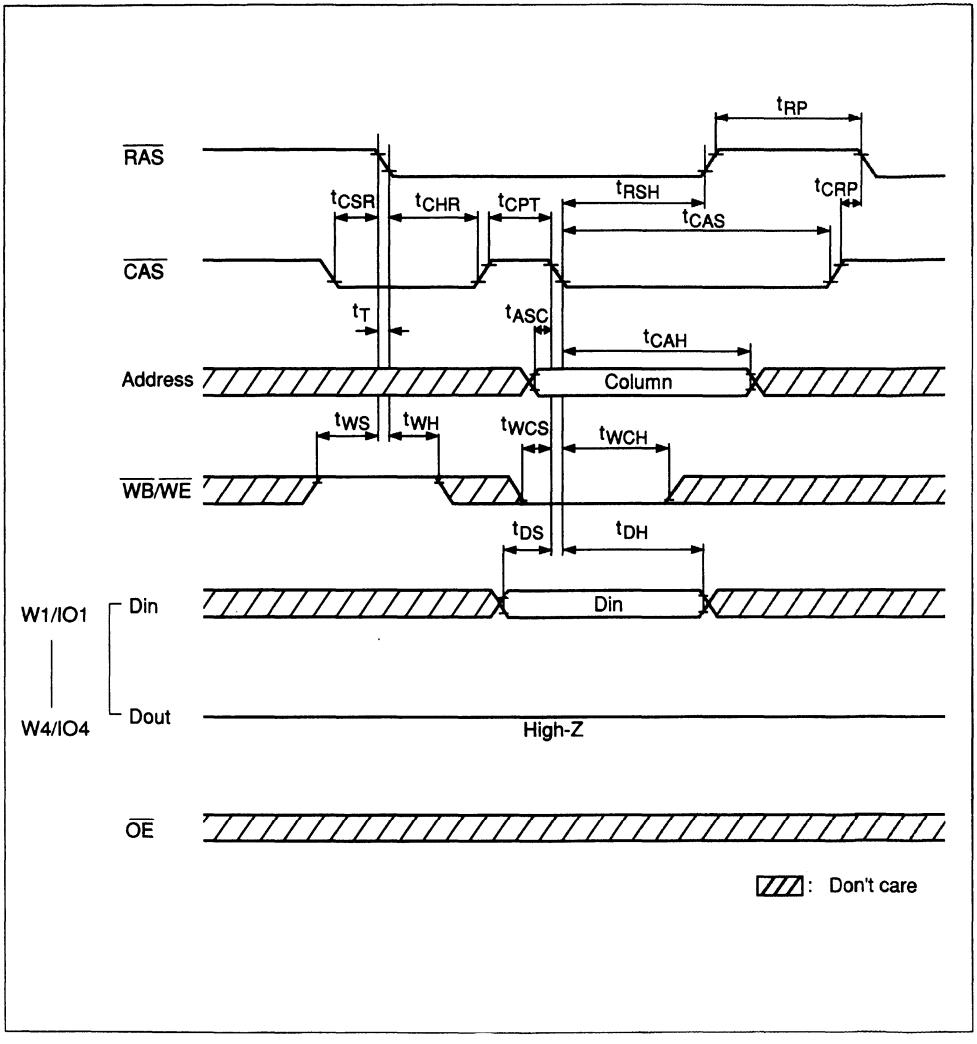
RAS-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514100 Series

4,194,304-Word × 1-Bit Dynamic RAM

The Hitachi HM514100 is a CMOS dynamic RAM organized 4,194,304-word × 1-bit. HM514100 has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514100 offers fast page mode as a high speed access mode.
Multiplexed address input permits the HM514100 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

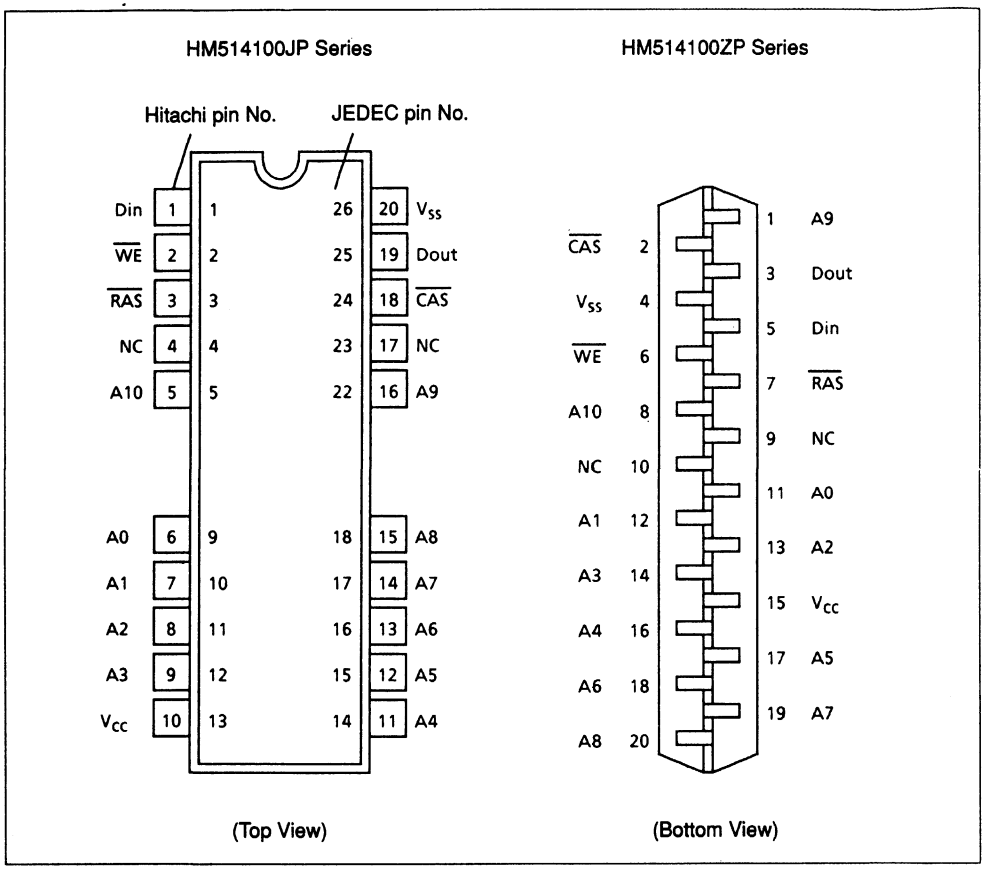
Ordering Information

Type No.	Access time	Package
HM514100JP-8	80 ns	350-mil 20-pin plastic SOJ (CP-20DA)
HM514100JP-10	100 ns	
HM514100JP-12	120 ns	
HM514100ZP-8	80 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514100ZP-10	100 ns	
HM514100ZP-12	120 ns	

Features

- Single 5 V (±10%)
- High speed
  - Access time
    80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode
    495 mW/440 mW/385 mW (max)
  - Standby mode 11 mW (max)
- Fast page mode capability
- 1,024 refresh cycles: (16 ms)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function

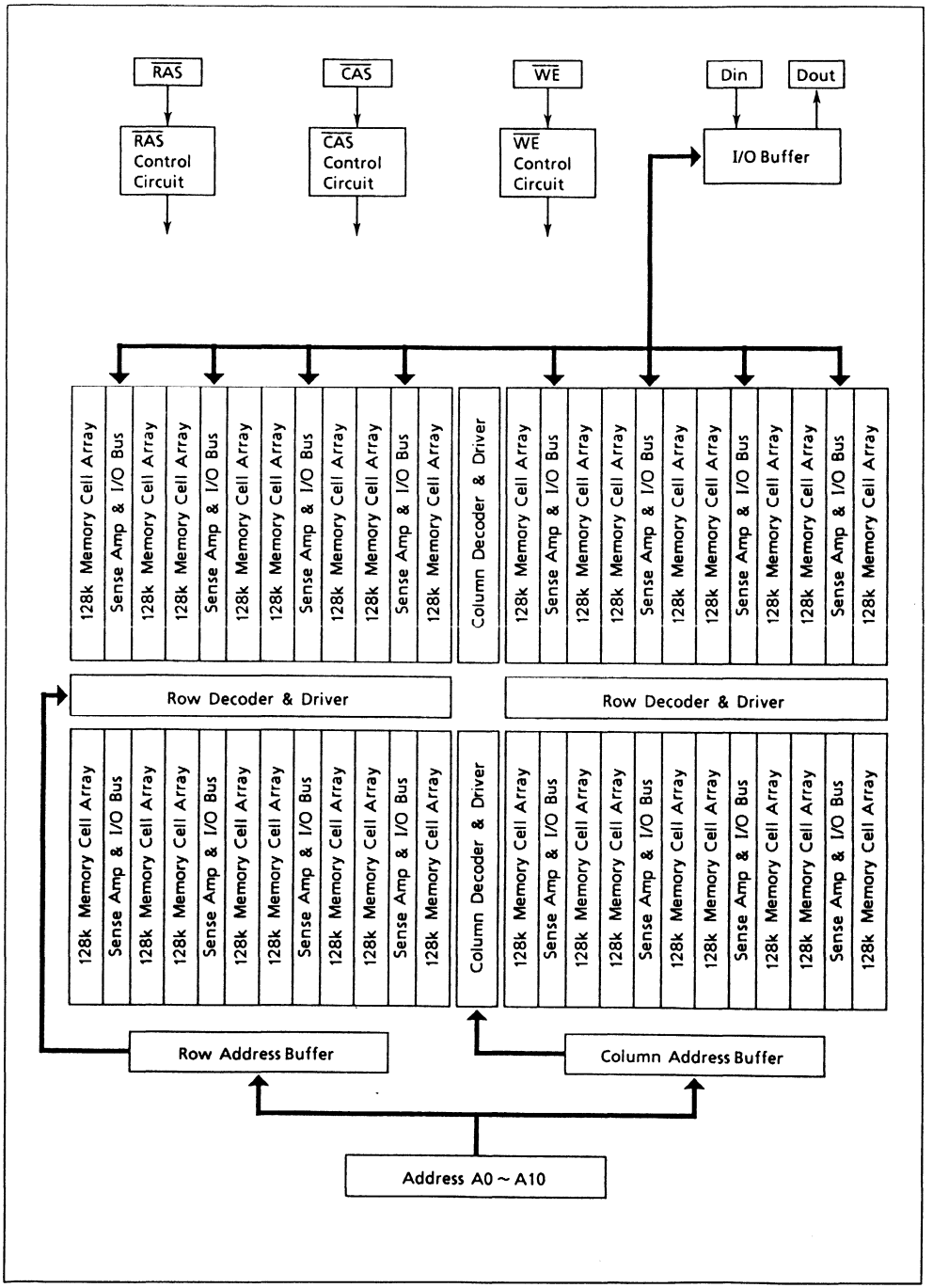
Pin Arrangement



Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A9	Refresh address input
Din	Data-in
Dout	Data-out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514100 -8		HM514100 -10		HM514100 -12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2 V Dout = High-Z	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514100 -8		HM514100 -10		HM514100 -12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1, 4
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	4
Fast page mode current	I_{CC7}	—	90	—	80	—	70	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address, data-in)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout

AC Characteristics (Ta = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*1,*12,*15

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM514100 -8		HM514100 -10		HM514100 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514100 -8 Min	HM514100 -8 Max	HM514100 -10 Min	HM514100 -10 Max	HM514100 -12 Min	HM514100 -12 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 16
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14, 16
Access time from address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 16
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HM514100 -8 Min	HM514100 -8 Max	HM514100 -10 Min	HM514100 -10 Max	HM514100 -12 Min	HM514100 -12 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514100 -8 Min	HM514100 -8 Max	HM514100 -10 Min	HM514100 -10 Max	HM514100 -12 Min	HM514100 -12 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	25	—	25	—	30	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514100 -8 Min	HM514100 -8 Max	HM514100 -10 Min	HM514100 -10 Max	HM514100 -12 Min	HM514100 -12 Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	15	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HM514100 -8 Min	HM514100 -8 Max	HM514100 -10 Min	HM514100 -10 Max	HM514100 -12 Min	HM514100 -12 Max	Unit	Notes
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	13

Fast Page Mode Cycle (cont)

		HM514100 -8		HM514100 -10		HM514100 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	3, 14, 16
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	

Fast Page Mode Read-Modify-Write Cycle

		HM514100 -8		HM514100 -10		HM514100 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Fast page mode read-modify-write cycle time	t_{PCM}	85	—	85	—	100	—	ns	
$\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	50	—	50	—	60	—	ns	10

Test Mode Cycle

		HM514100 -8		HM514100 -10		HM514100 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	20	—	20	—	20	—	ns	

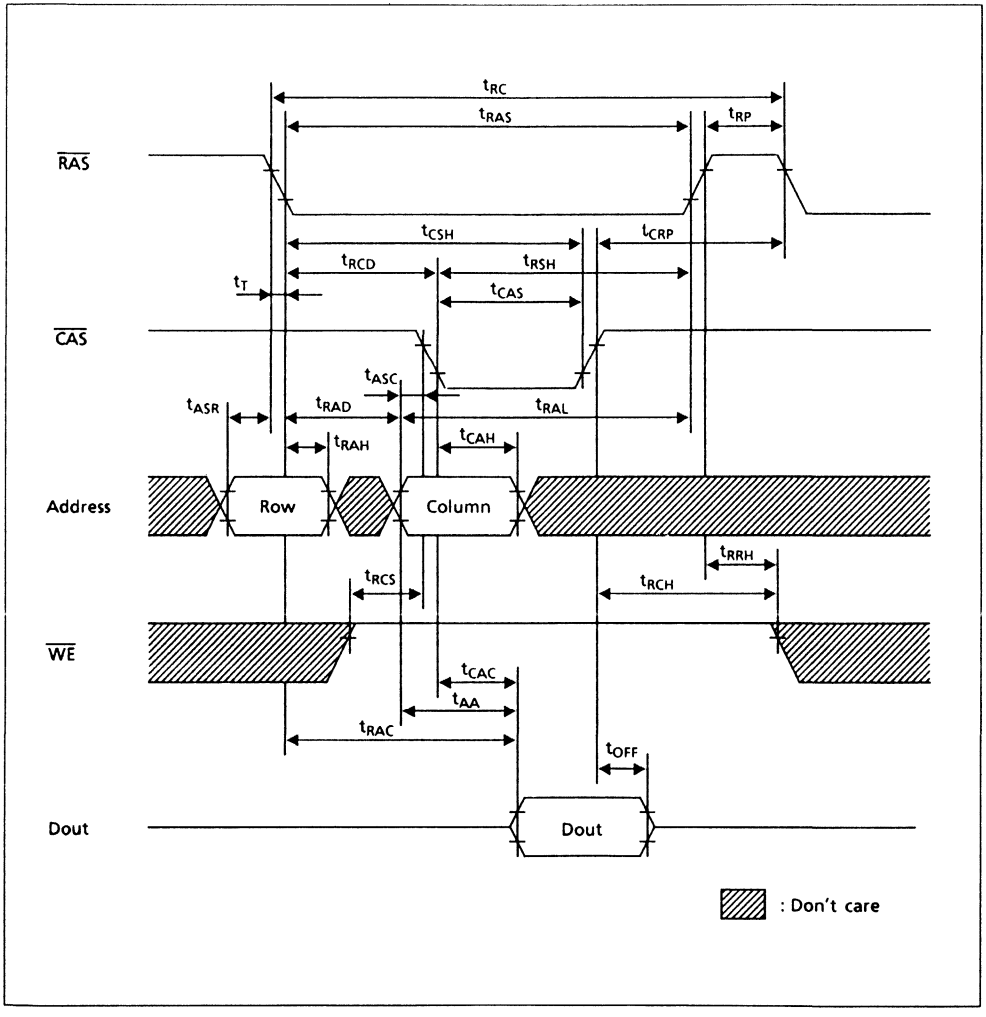
Counter Test Cycle

		HM514100 -8		HM514100 -10		HM514100 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	50	—	60	—	ns	

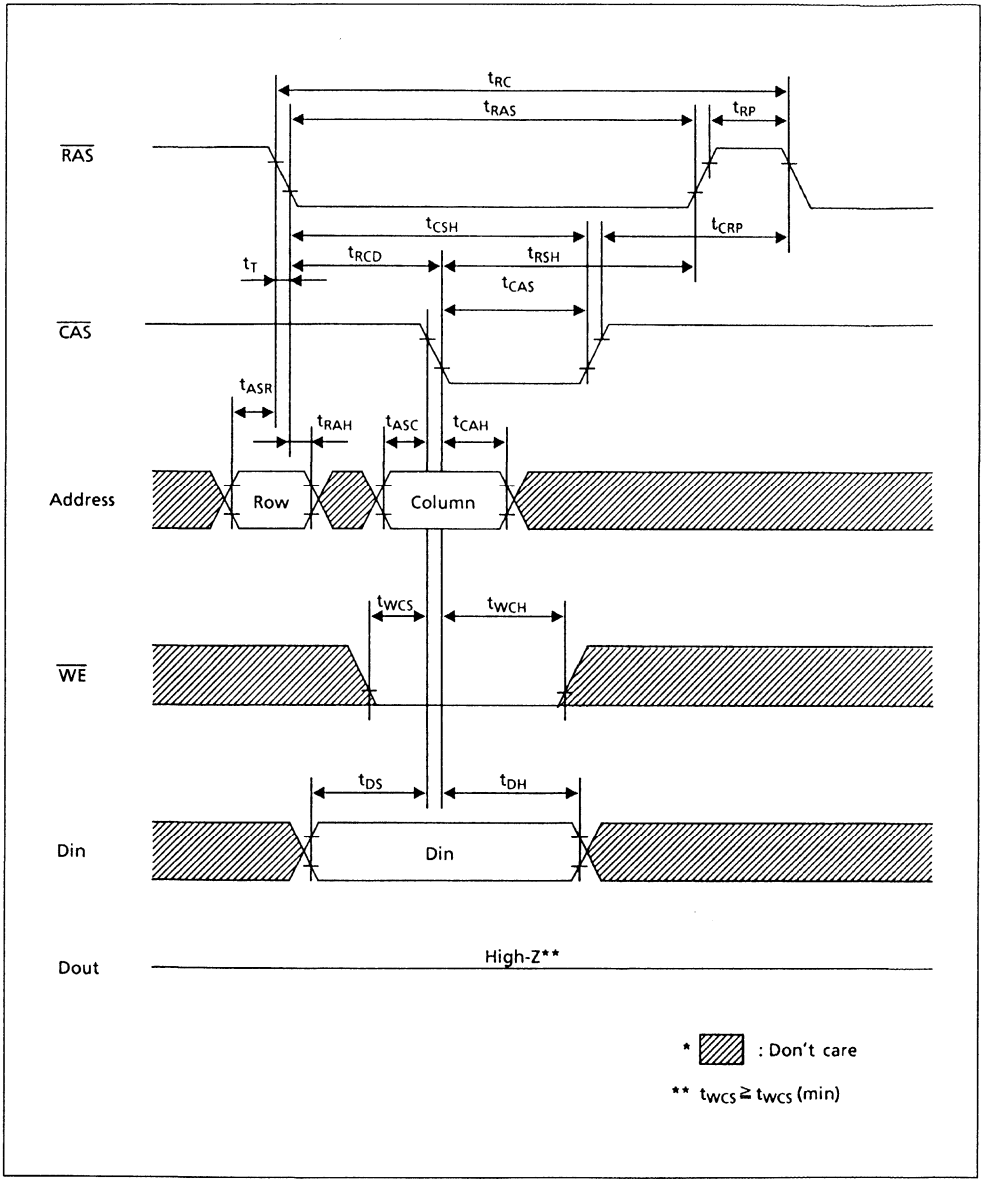
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min) the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performedby normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, t_{AA} t_{CAC} and t_{ACP} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

Timing Waveforms

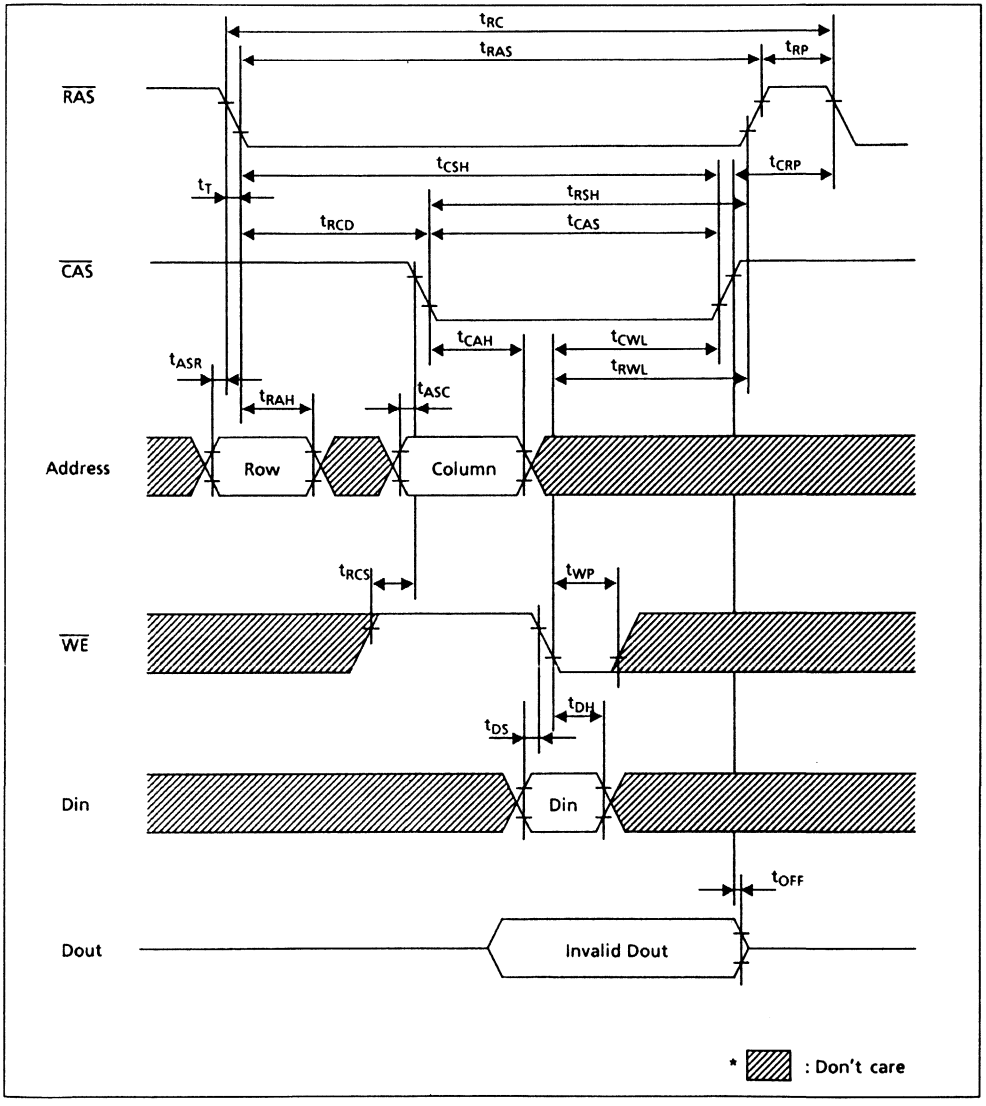
Read Cycle



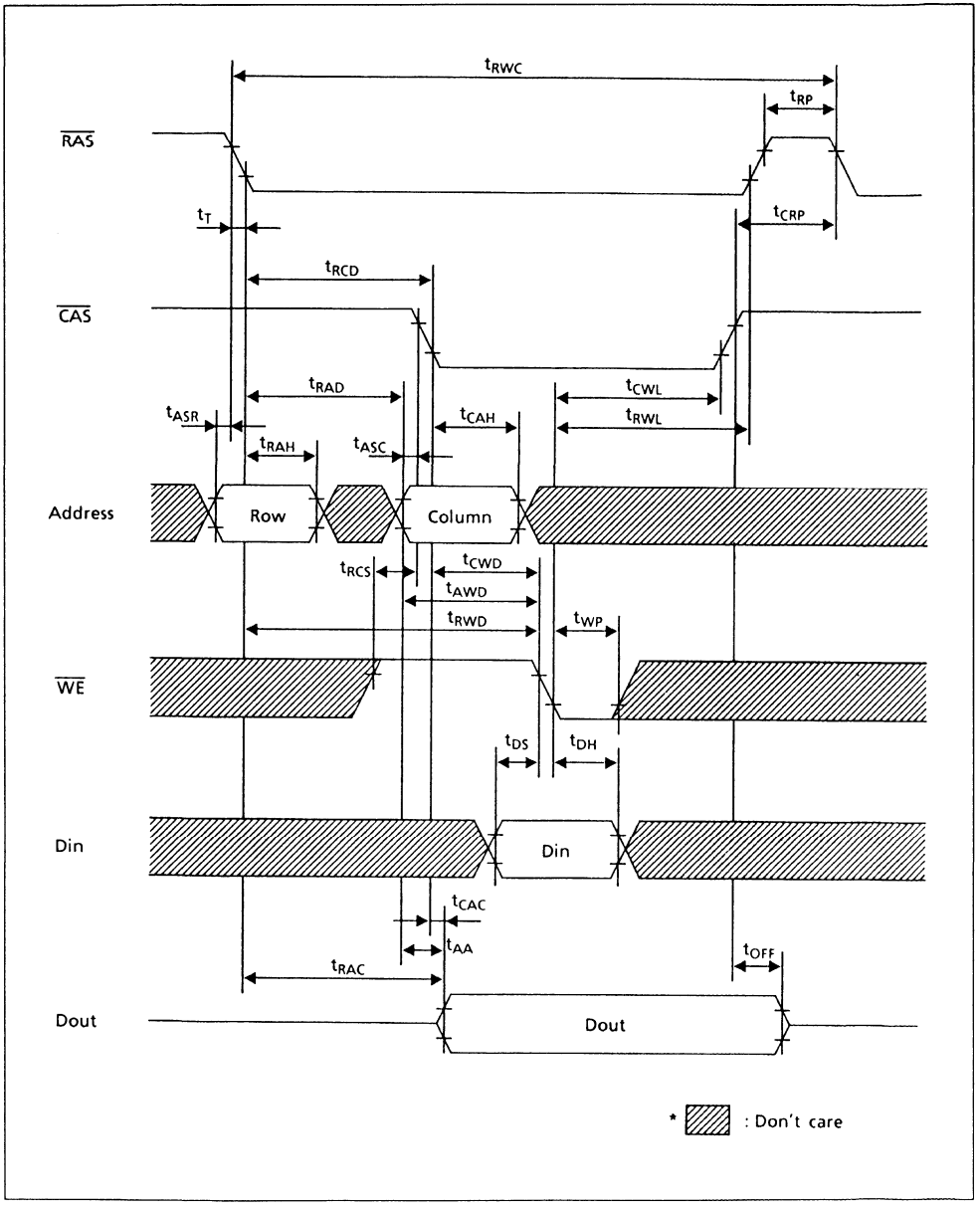
Early Write Cycle



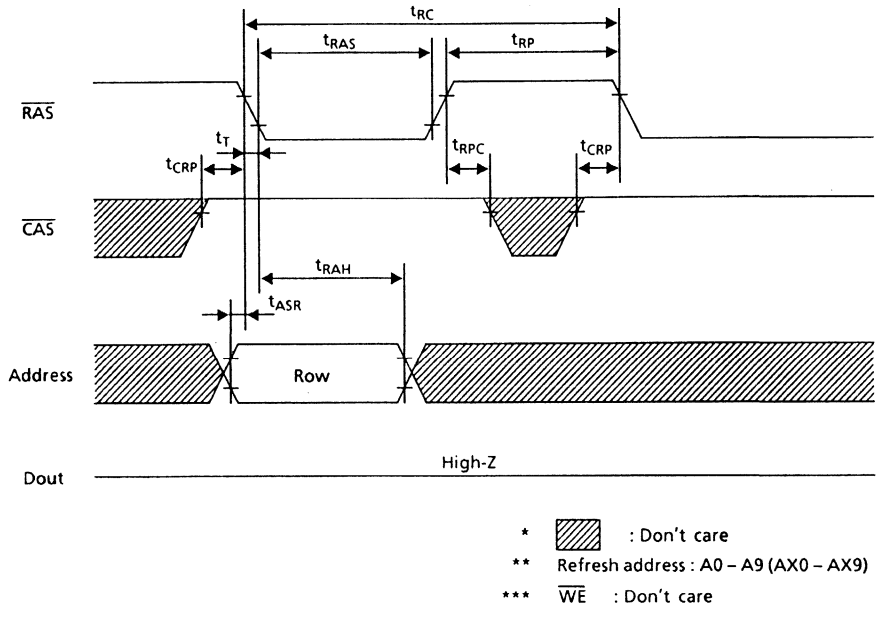
Delayed Write Cycle



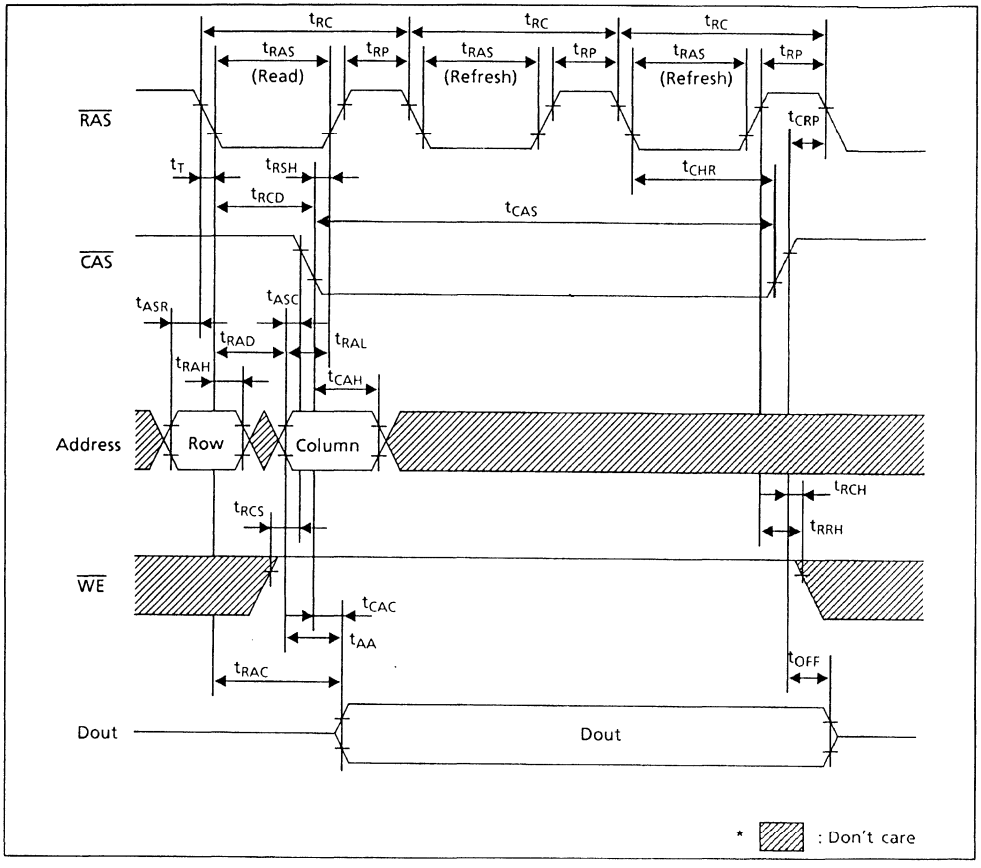
Read-Modify-Write Cycle



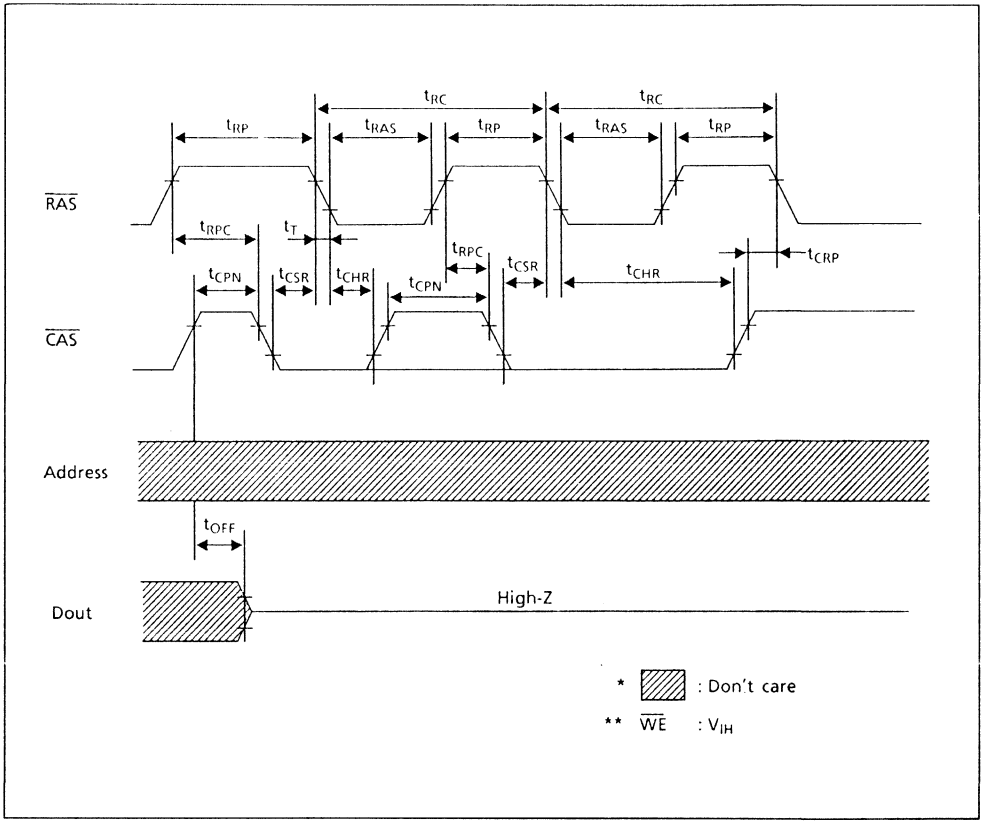
$\overline{RAS}$-Only Refresh Cycle



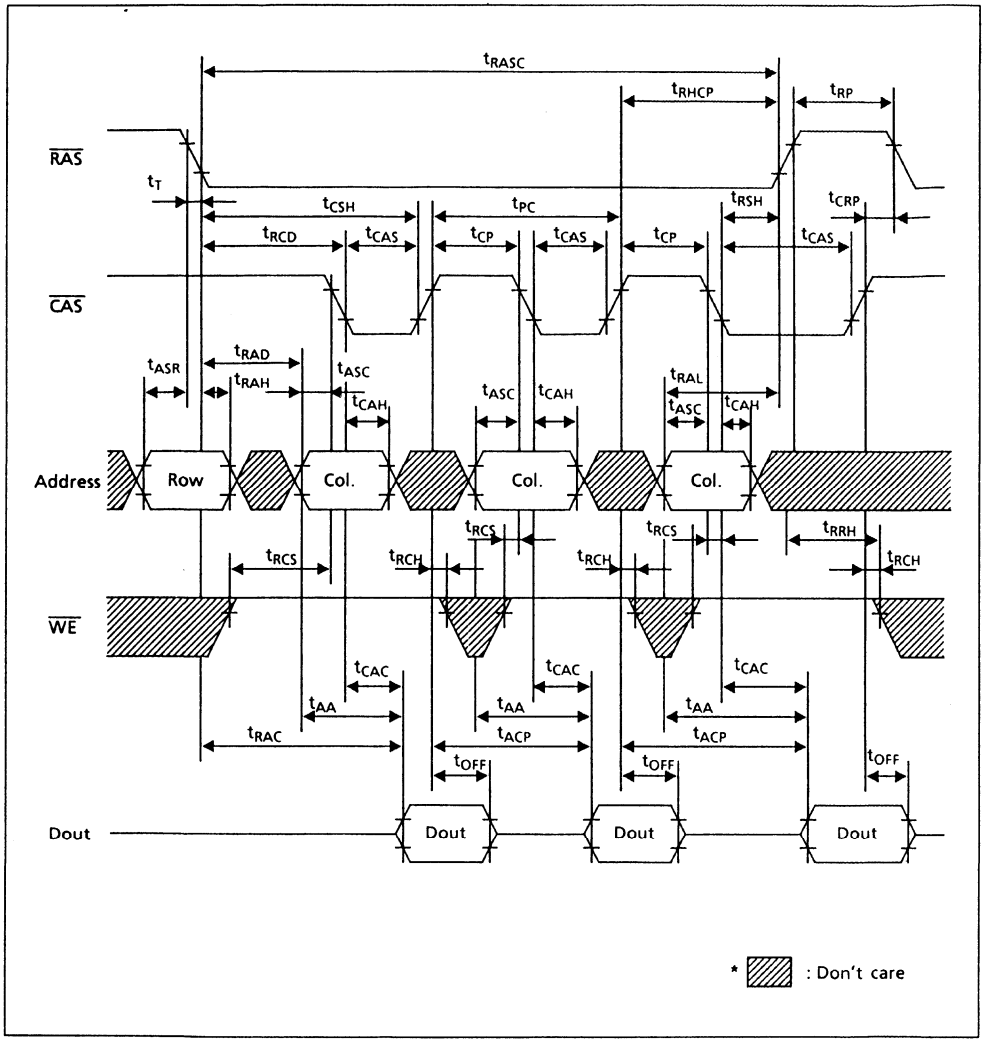
Hidden Refresh Cycle



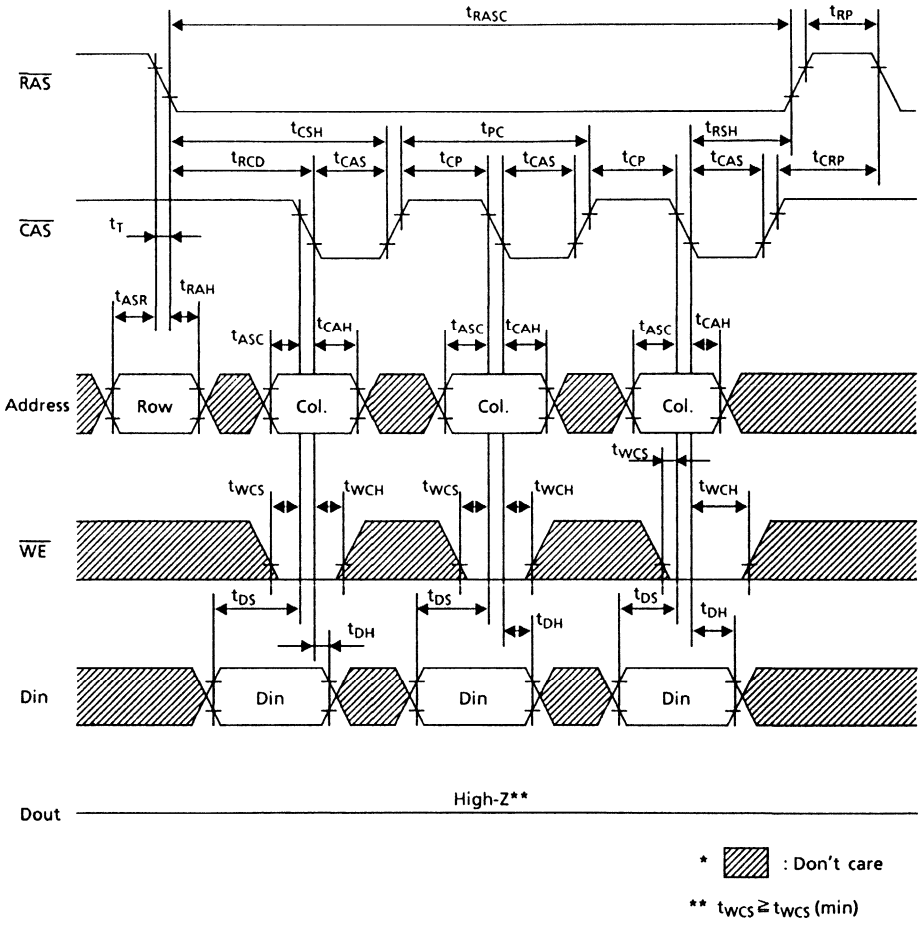
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



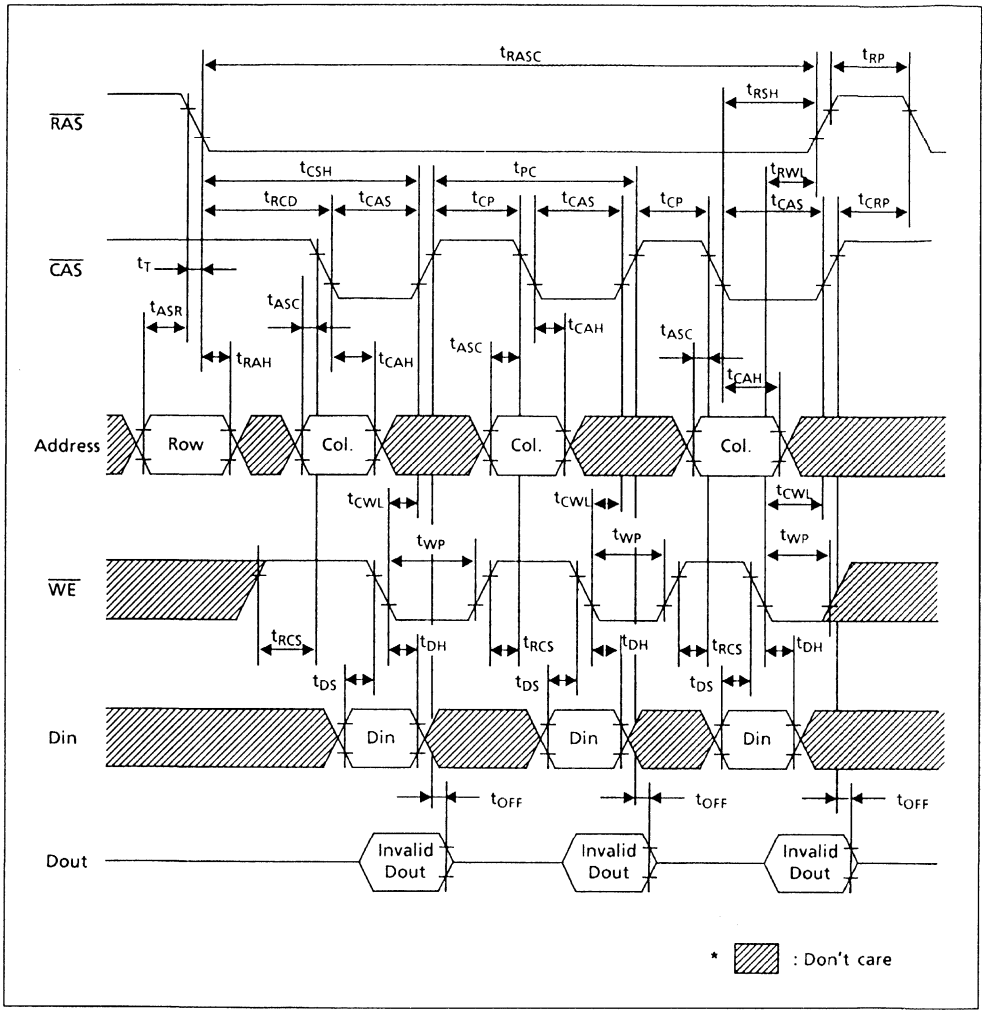
Fast Page Mode Read Cycle



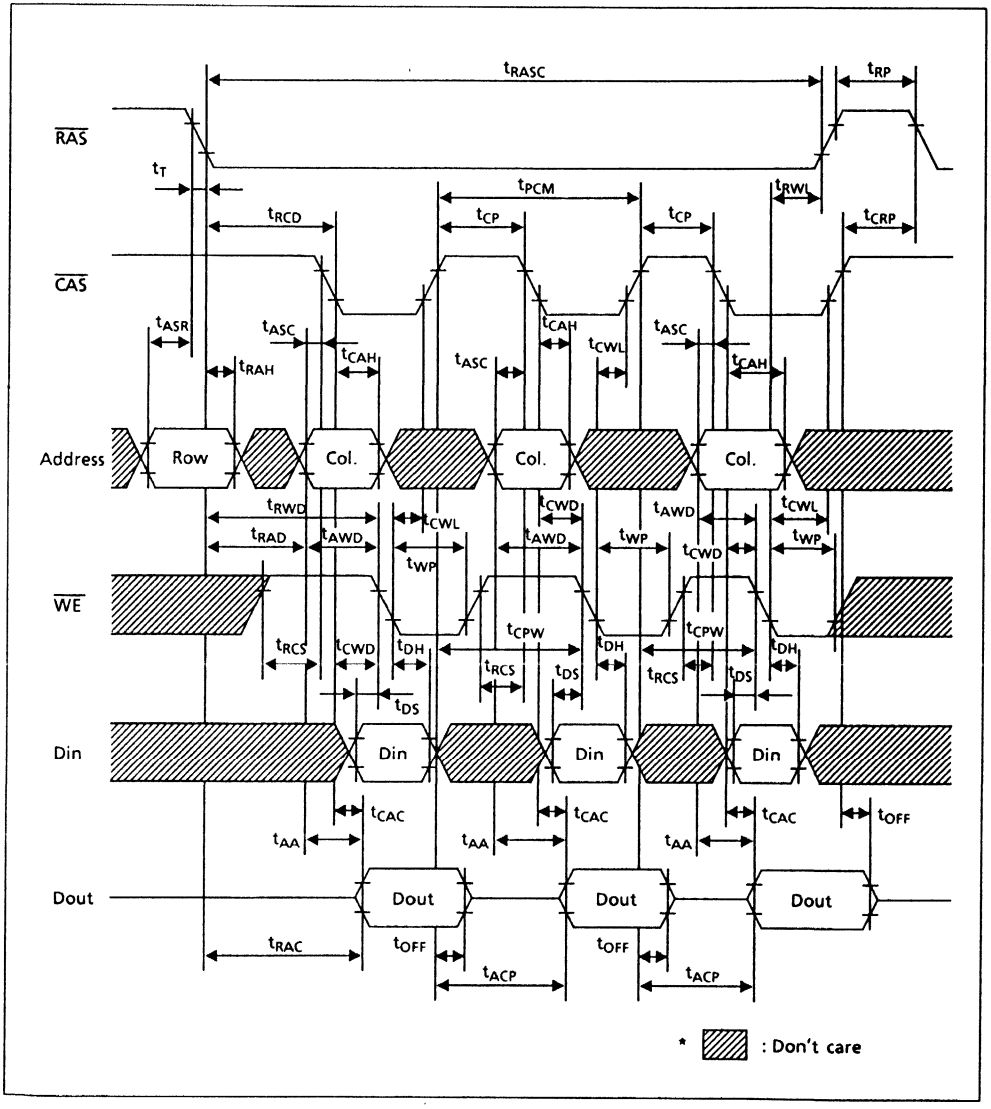
Fast Page Mode Early Write Cycle



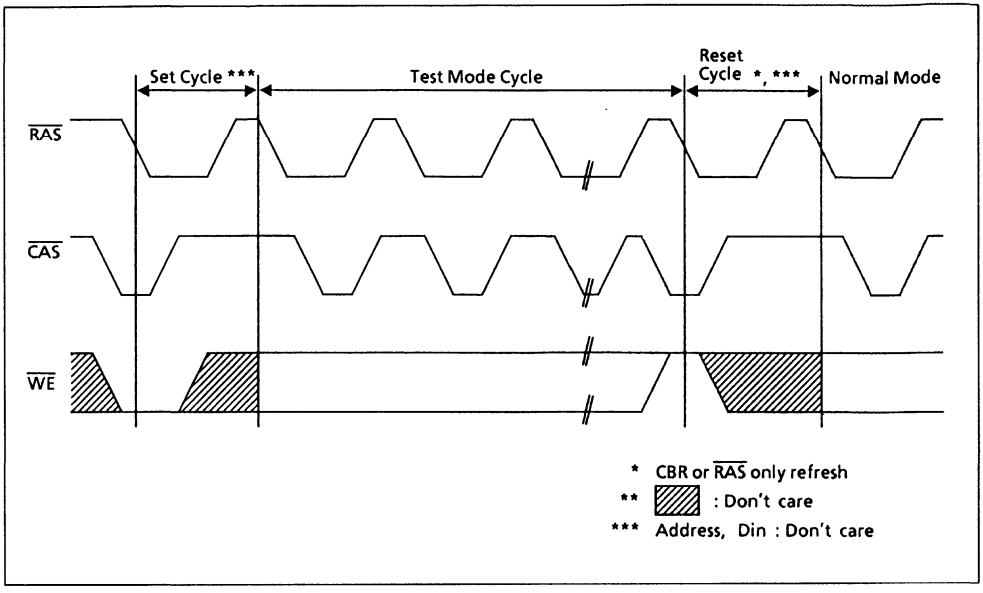
Fast Page Mode Delayed Write Cycle



Fast Page Mode Read-Modify-Write Cycle

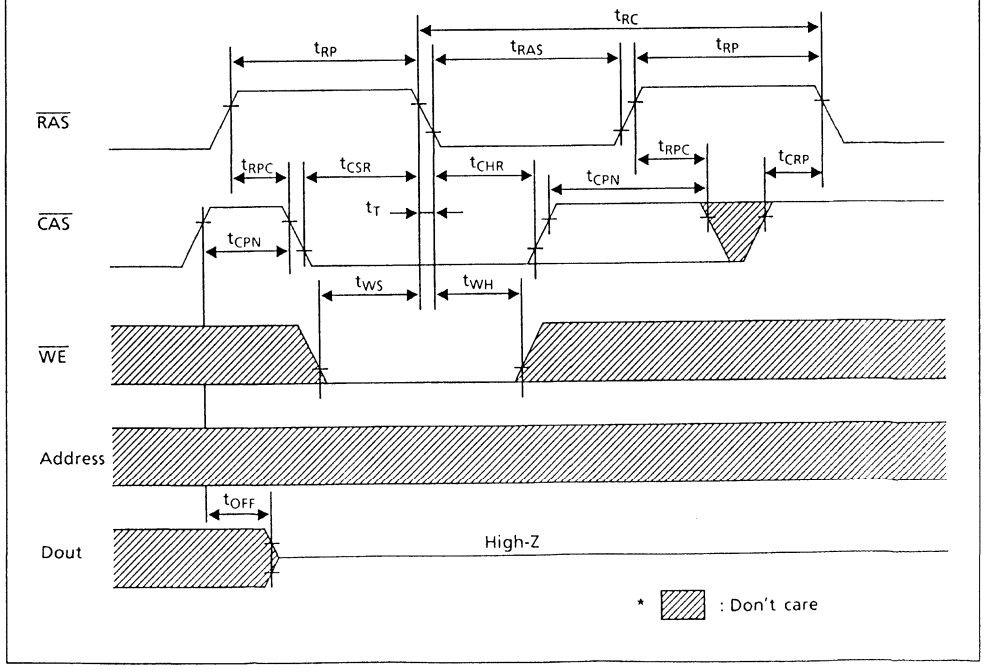


Test Mode Cycle



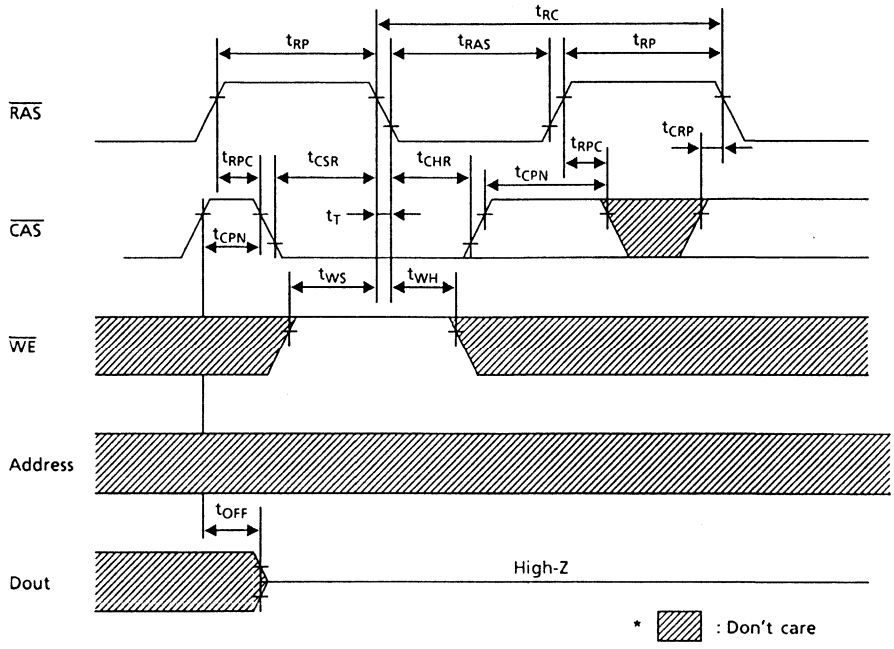
Test Mode Set Cycle

WE-And-CAS-Before-RAS Refresh Cycle

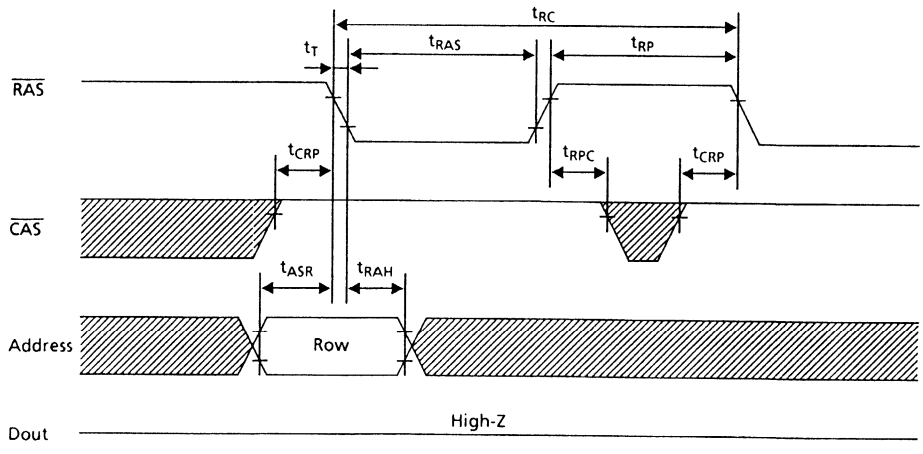


Test Mode Reset Cycle

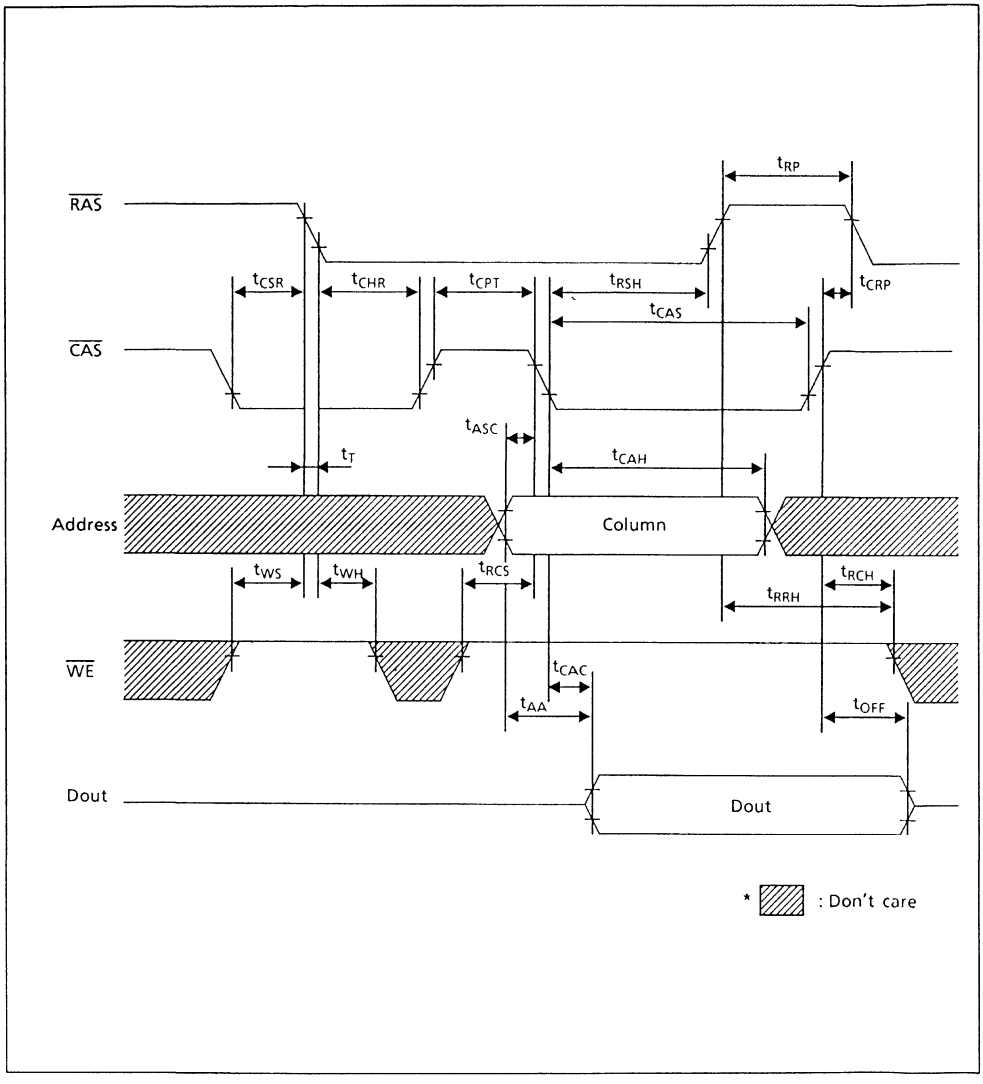
CAS-Before-RAS Refresh Cycle



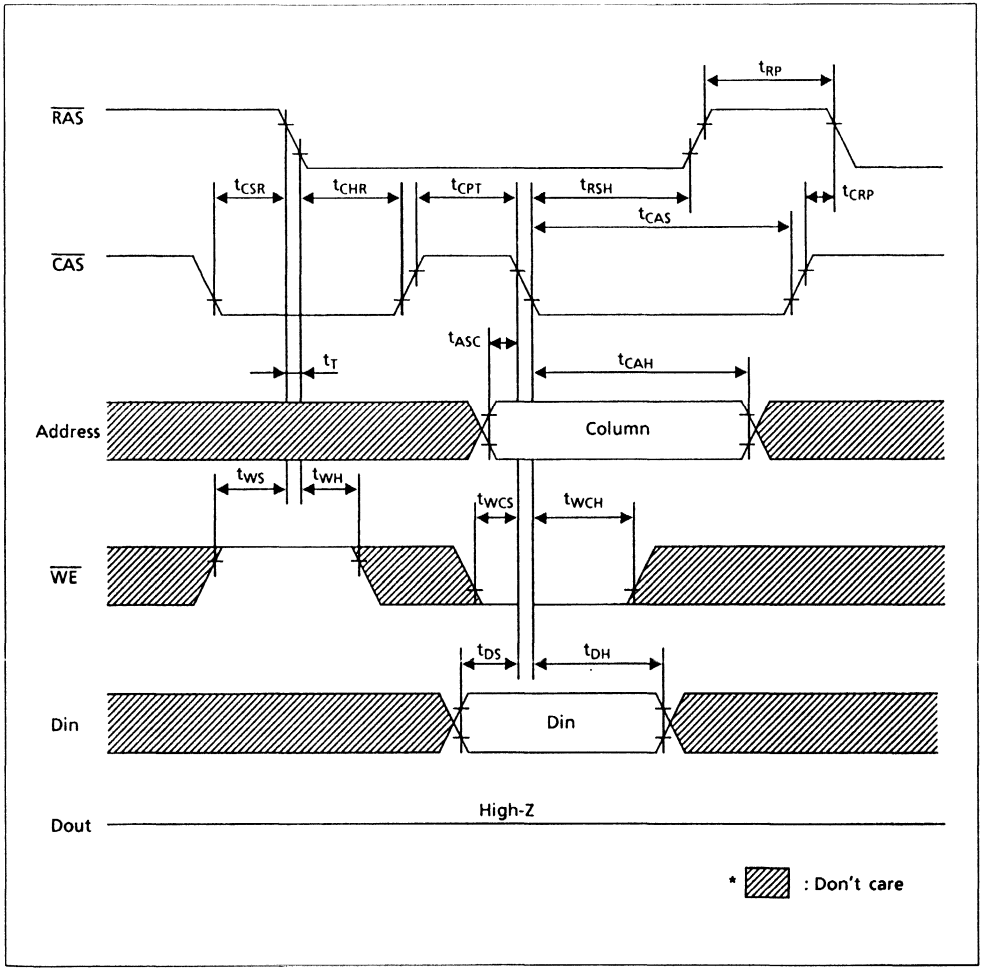
RAS-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514101 Series

4,194,304-Word × 1-Bit Dynamic RAM

The Hitachi HM514101 is a CMOS dynamic RAM organized 4,194,304-word × 1-bit. HM514101 has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514101 offers nibble mode as a high speed access mode.

Multiplexed address input permits the HM514101 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

Ordering Information

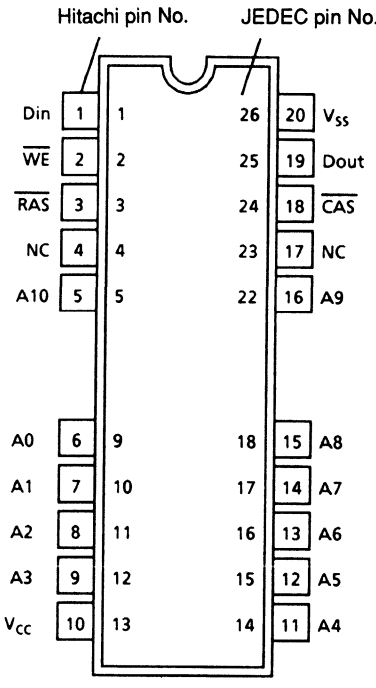
Type No.	Access time	Package
HM514101JP-8	80 ns	350-mil 20-pin plastic SOJ (CP-20DA)
HM514101JP-10	100 ns	
HM514101JP-12	120 ns	
HM514101ZP-8	80 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514101ZP-10	100 ns	
HM514101ZP-12	120 ns	

Features

- Single 5 V (±10%)
- High speed
  - Access time
    80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode
    495 mW/440 mW/385 mW (max)
  - Standby mode 11 mW (max)
- Nibble mode capability
- 1,024 refresh cycles: (16 ms)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function

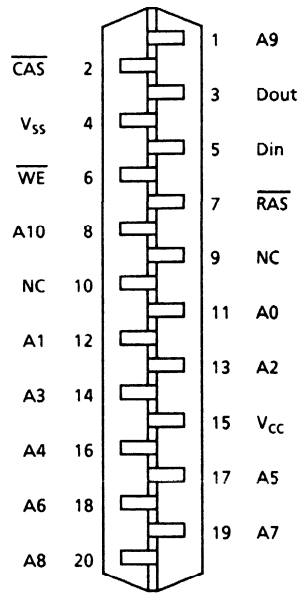
Pin Arrangement

HM514101JP Series



(Top View)

HM514101ZP Series



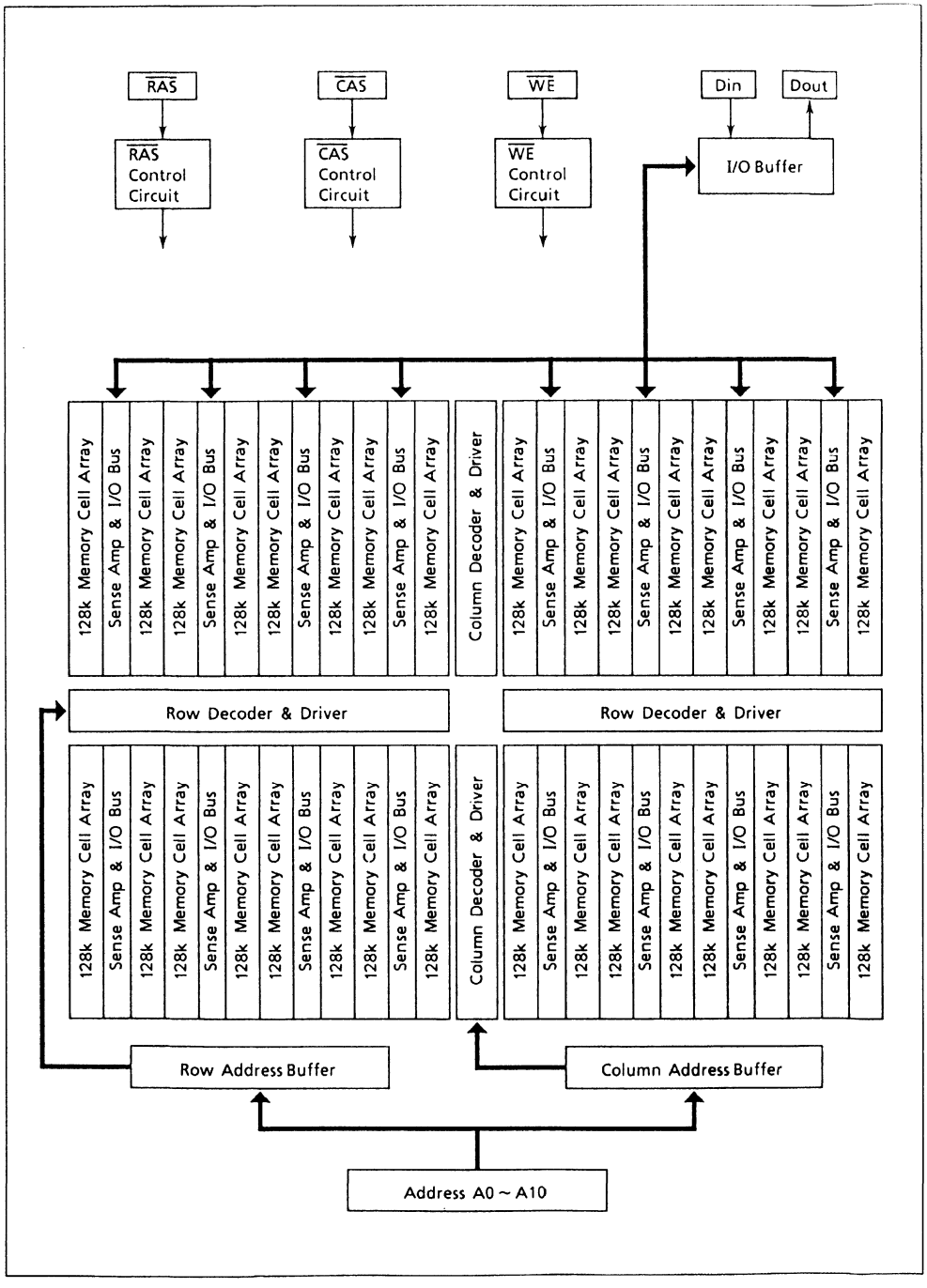
(Bottom View)

Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A9	Refresh address input
Din	Data-in
Dout	Data-out
$\overline{RAS}$	Row address strobe

Pin name	Function
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514101 -8		HM514101 -10		HM514101 -12				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} − 0.2 V Dout = High-Z	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514101 -8		HM514101 -10		HM514101 -12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1, 4
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	4
Nibble mode current	I_{CC8}	—	90	—	80	—	70	mA	t_{NC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address, data-in)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout

AC Characteristics (Ta = 0°C to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *12, *13

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM514101 -8		HM514101 -10		HM514101 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 14
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4, 14
Access time from address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	20	—	25	—	ns	11

Read-Modify-Write Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	25	—	25	—	30	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	40	—	45	—	55	—	ns	10

Refresh Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	15	—	ns	

Nibble Mode Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
Nibble mode access time	t_{NAC}	—	25	—	25	—	30	ns	14
Nibble mode cycle time	t_{NC}	45	—	45	—	55	—	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	10	—	10	—	15	—	ns	
Nibble mode $\overline{CAS}$ pulse width	t_{NCA}	25	—	25	—	30	—	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	25	—	25	—	30	—	ns	

Nibble Mode Read-Modify-Write Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
Nibble mode read-modify-write cycle time	t_{NRWC}	75	—	75	—	90	—	ns	
Nibble mode write command to $\overline{CAS}$ lead time	t_{NCWL}	25	—	25	—	30	—	ns	
Nibble mode $\overline{CAS}$ to $\overline{WE}$ delay time	t_{NCWD}	25	—	25	—	30	—	ns	10

Test Mode Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	20	—	20	—	20	—	ns	

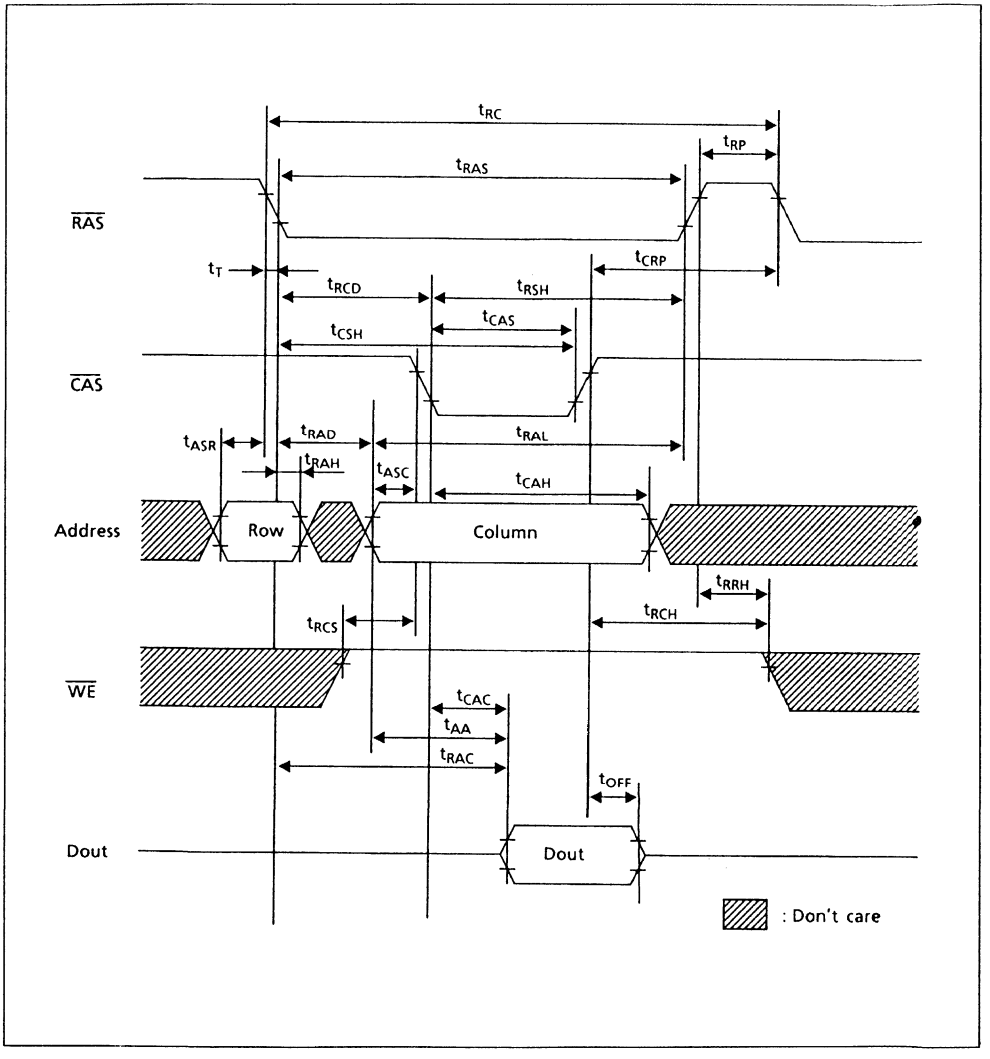
Counter Test Cycle

Parameter	Symbol	HM514101 -8 Min	HM514101 -8 Max	HM514101 -10 Min	HM514101 -10 Max	HM514101 -12 Min	HM514101 -12 Max	Unit	Notes
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	50	—	60	—	ns	

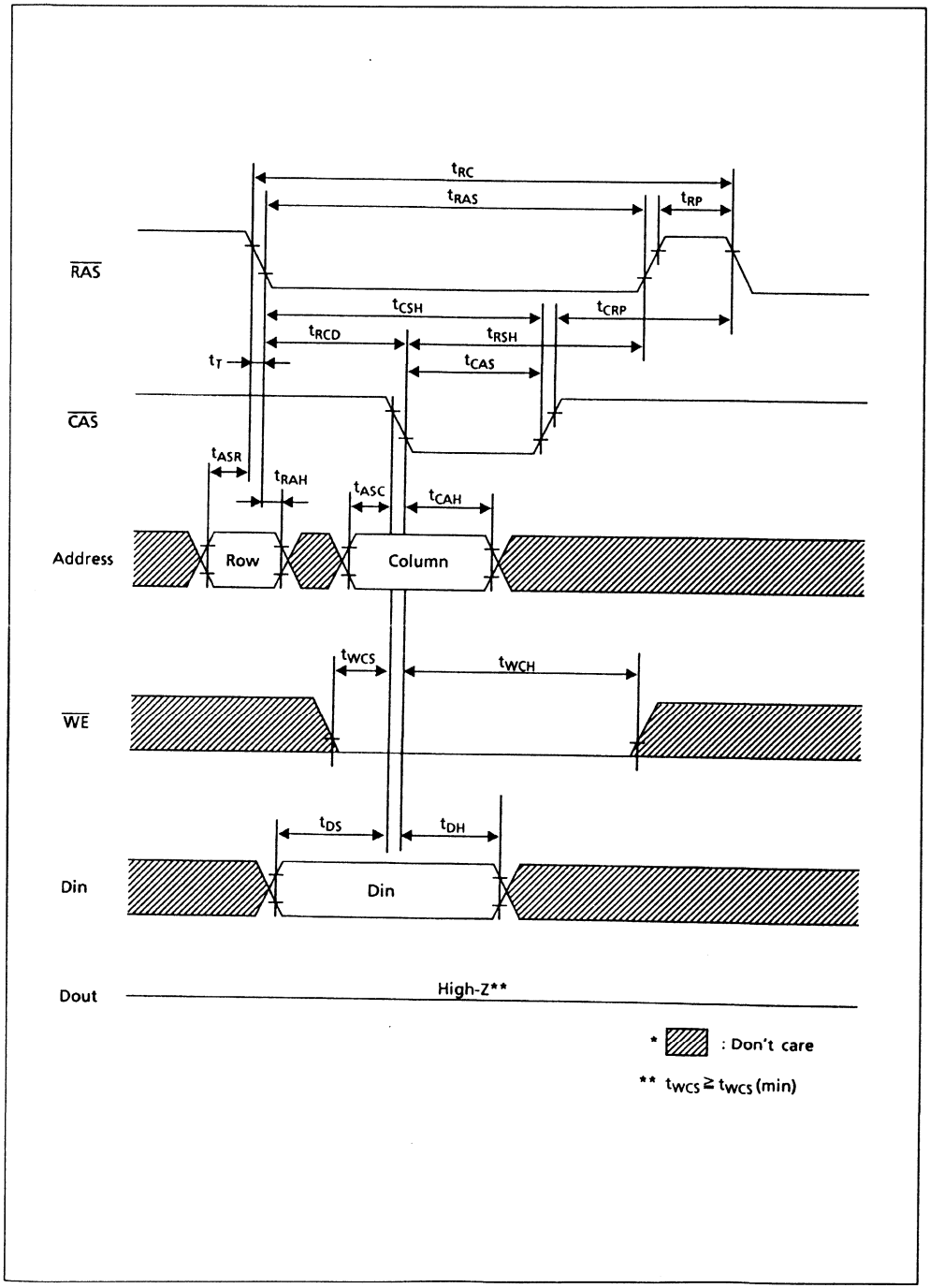
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{NCWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{NCWD} \geq t_{NCWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. An initial pause of 100 µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles is required. Clock voltages ($\overline{RAS}$ and $\overline{CAS}$) must be applied simultaneously with or prior to applying supply voltage.
13. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
14. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{NAC} is delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

Timing Waveforms

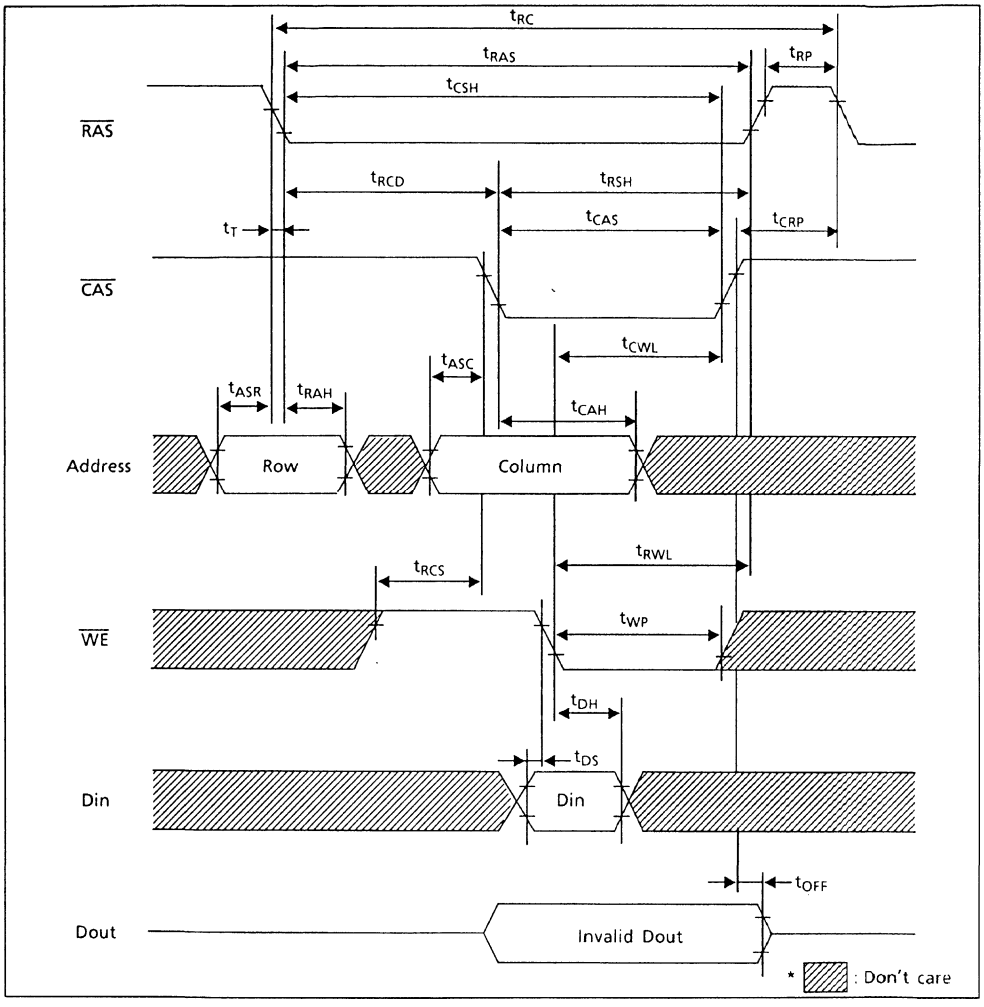
Read Cycle



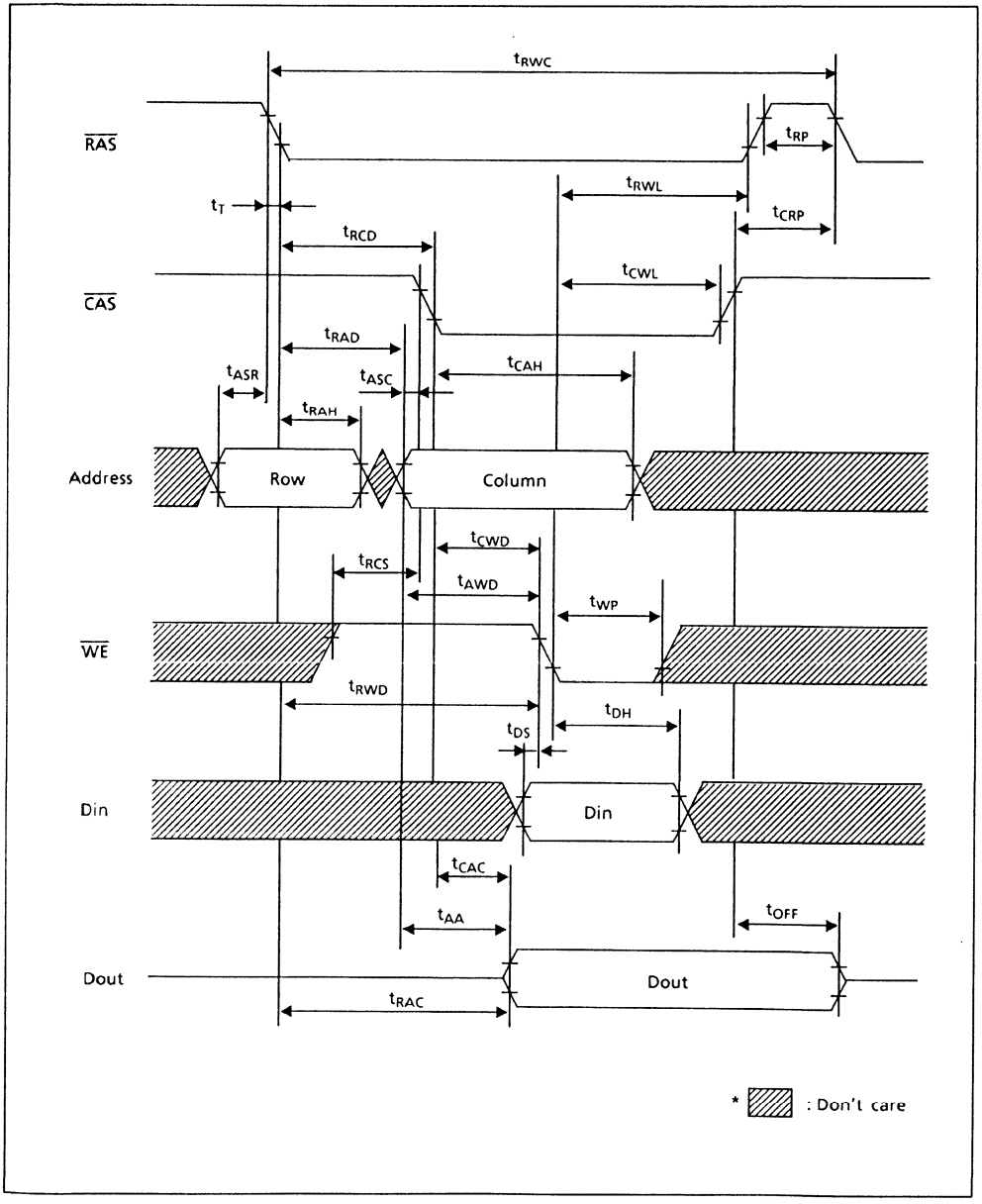
Early Write Cycle



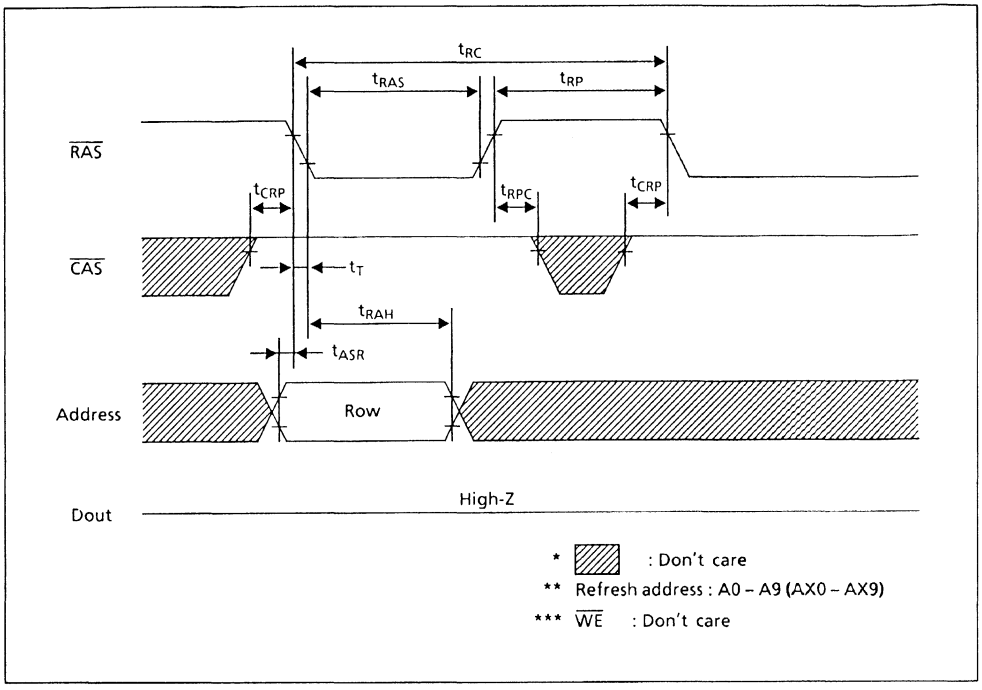
Delayed Write Cycle



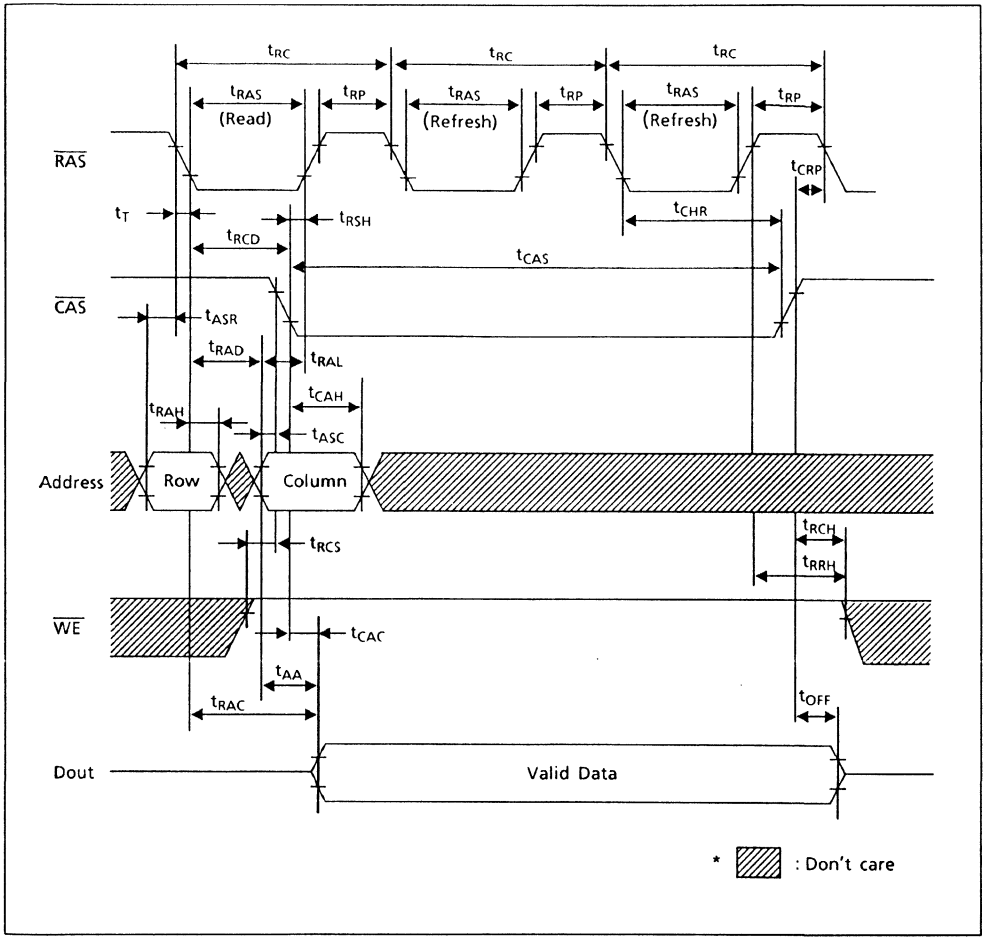
Read-Modify-Write Cycle



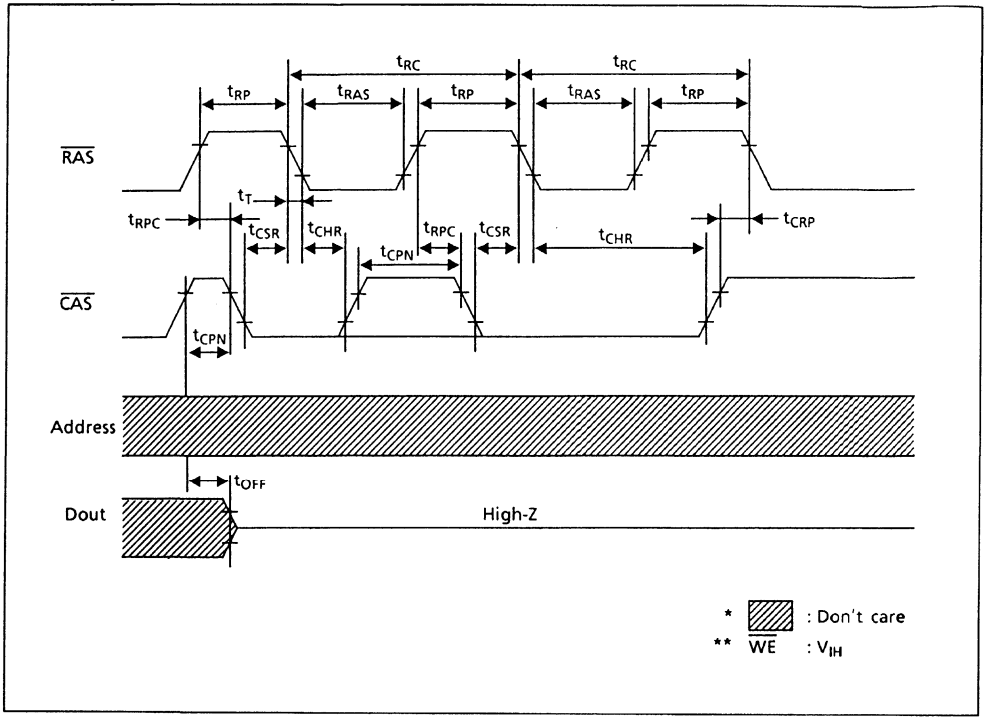
$\overline{RAS}$-Only Refresh Cycle



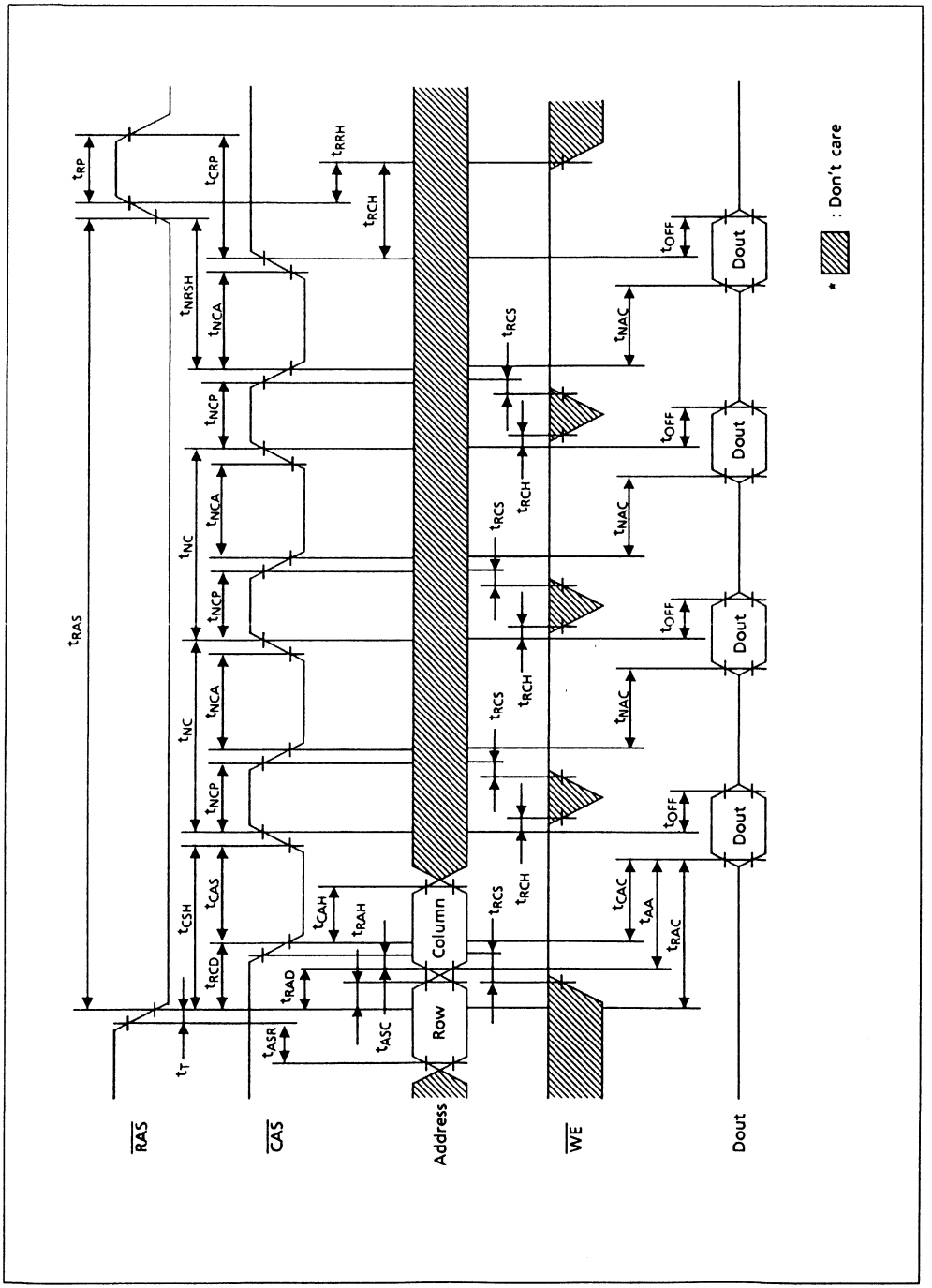
Hidden Refresh Cycle



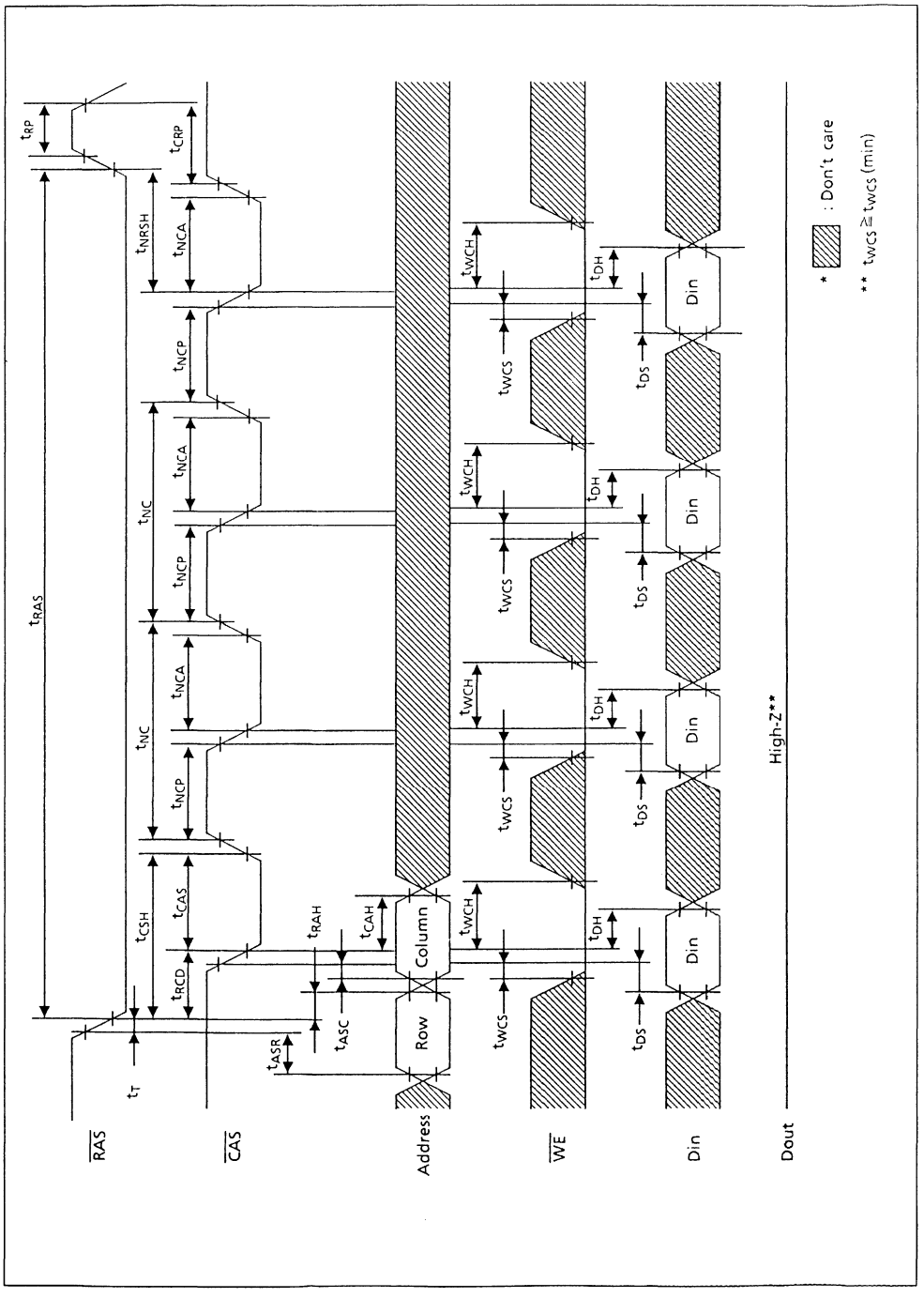
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



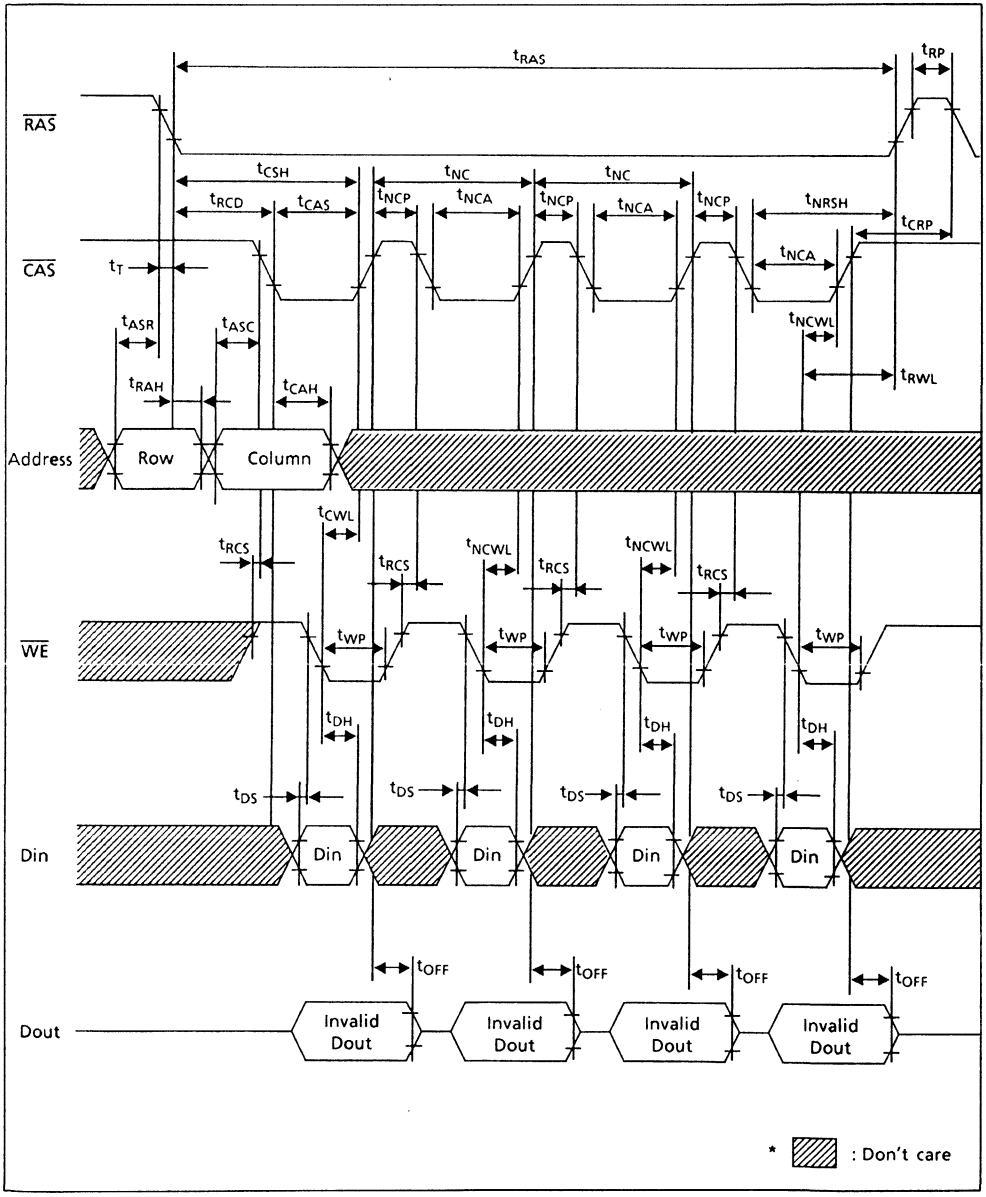
Nibble Mode Read Cycle



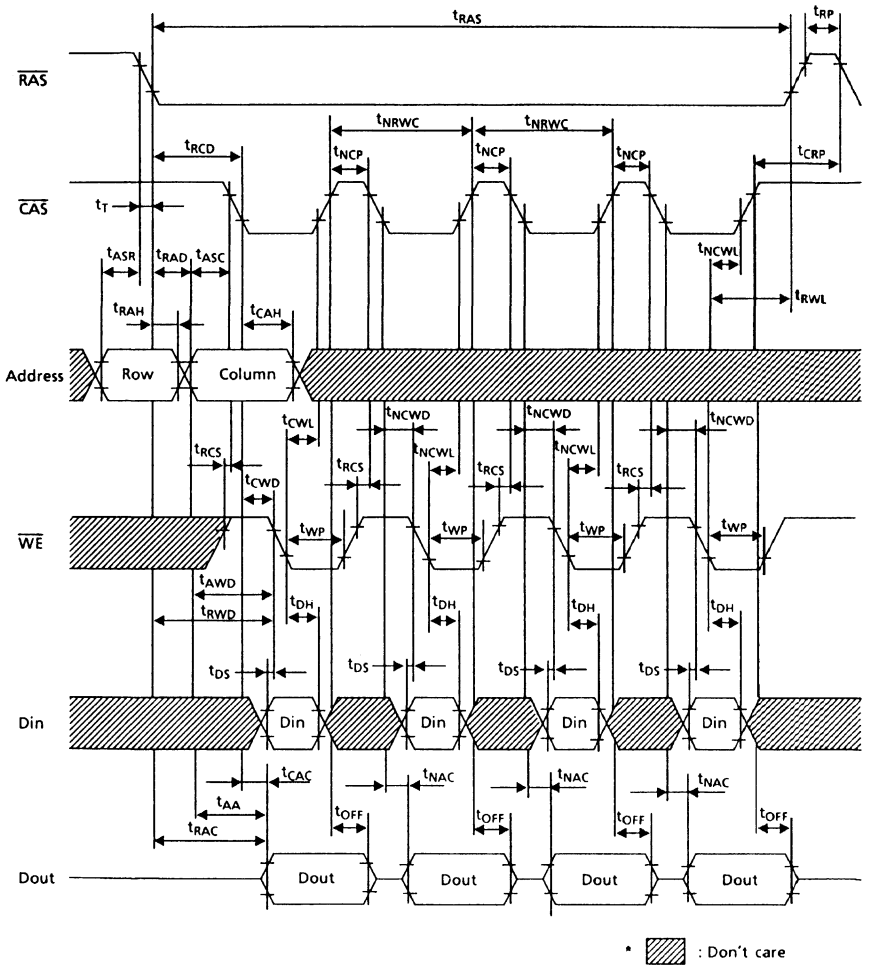
Nibble Mode Early Write Cycle



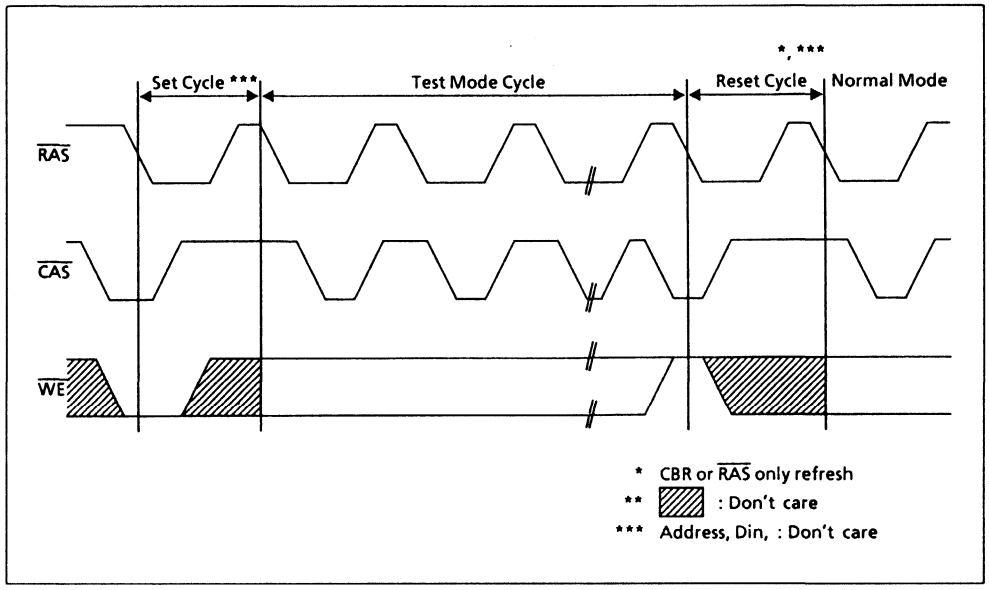
Nibble Mode Delayed Write Cycle



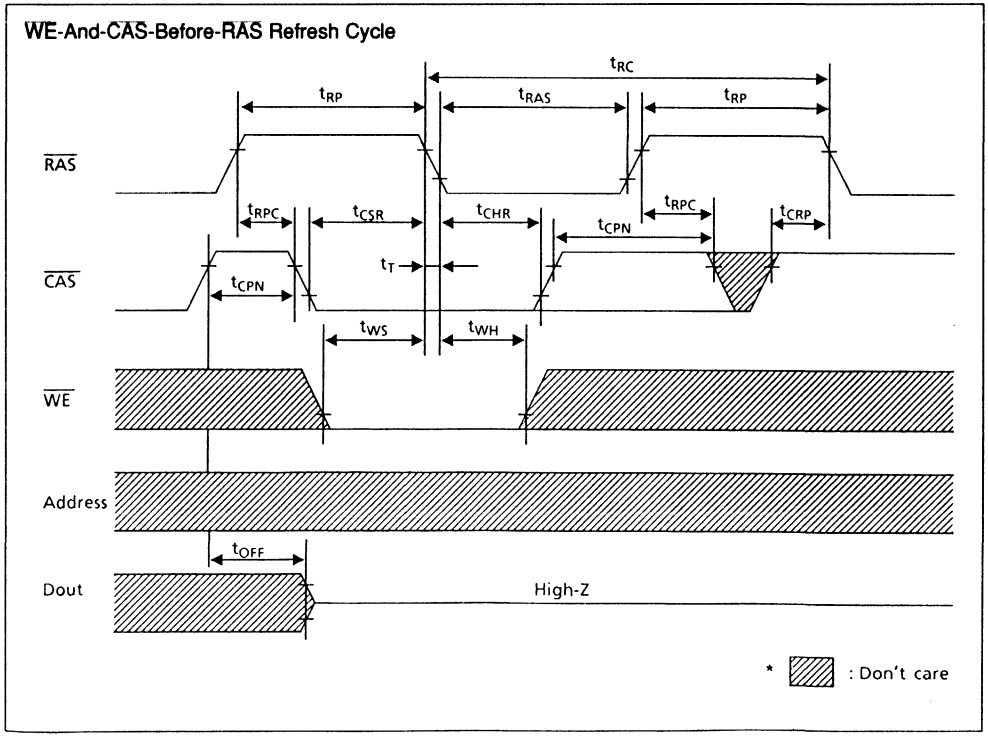
Nibble Mode Read-Modify-Write Cycle



Test Mode Cycle

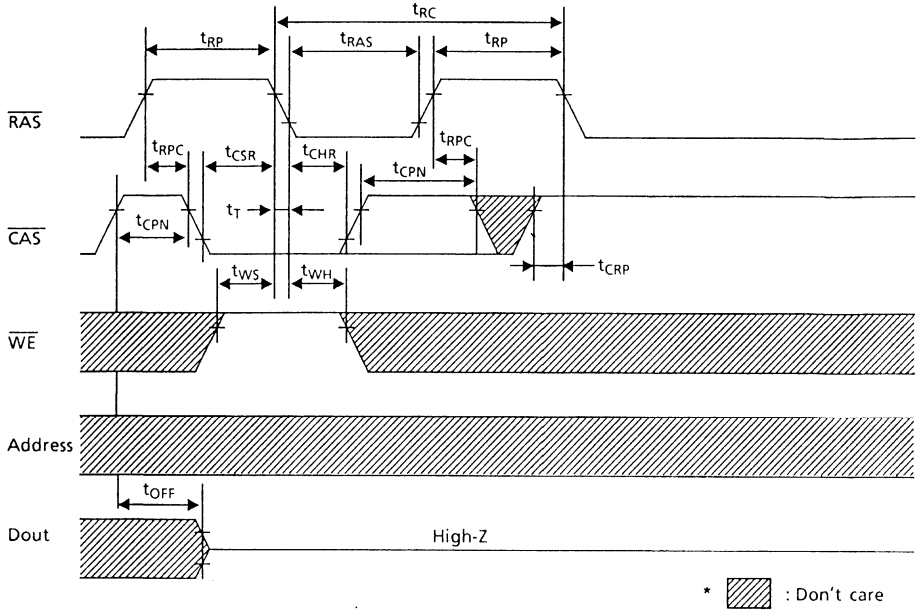


Test Mode Set Cycle

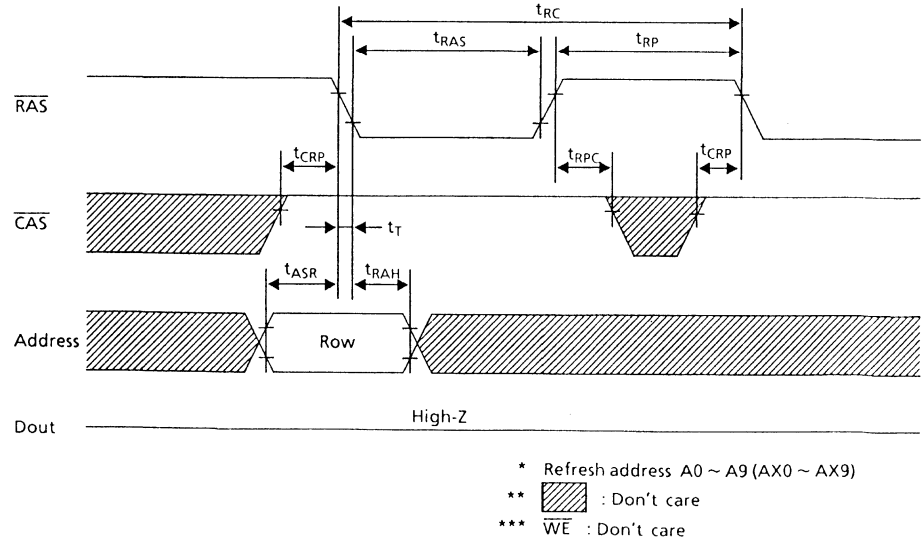


Test Mode Reset Cycle

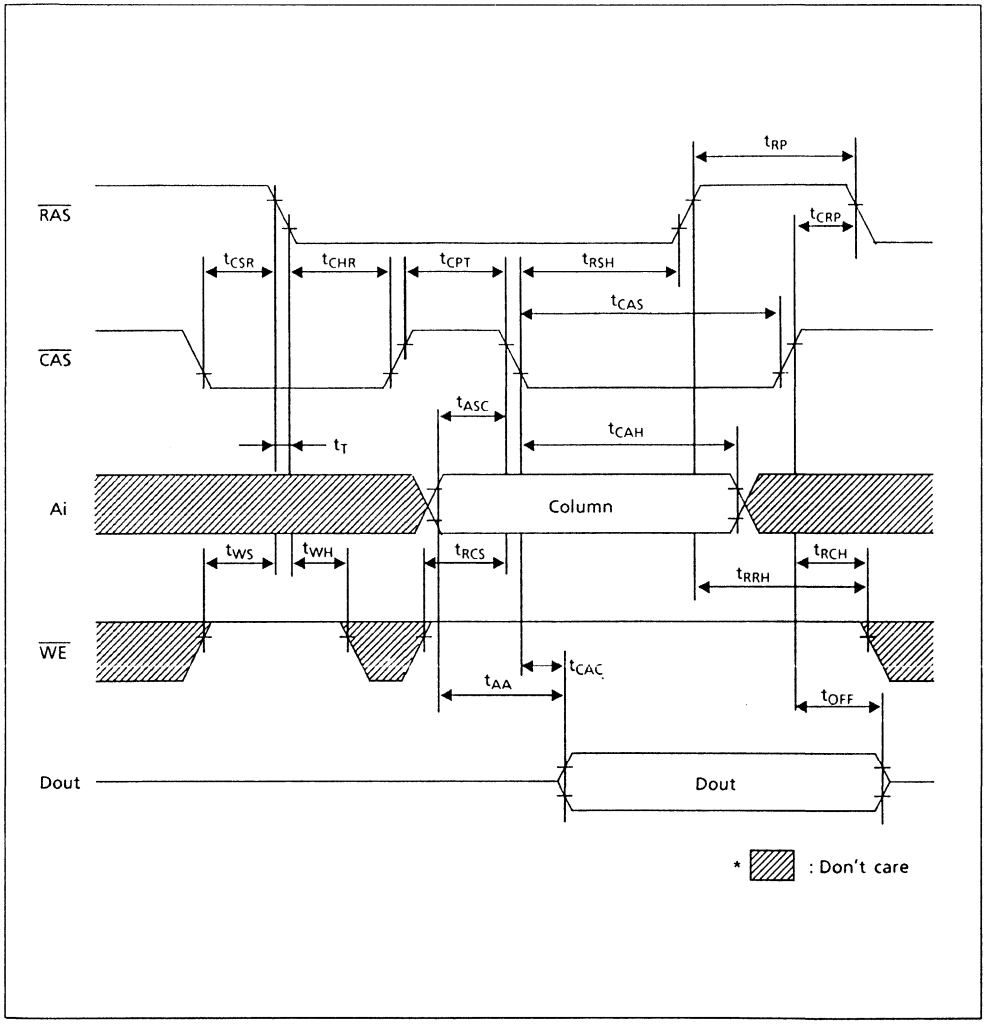
CAS-Before-RAS Refresh Cycle



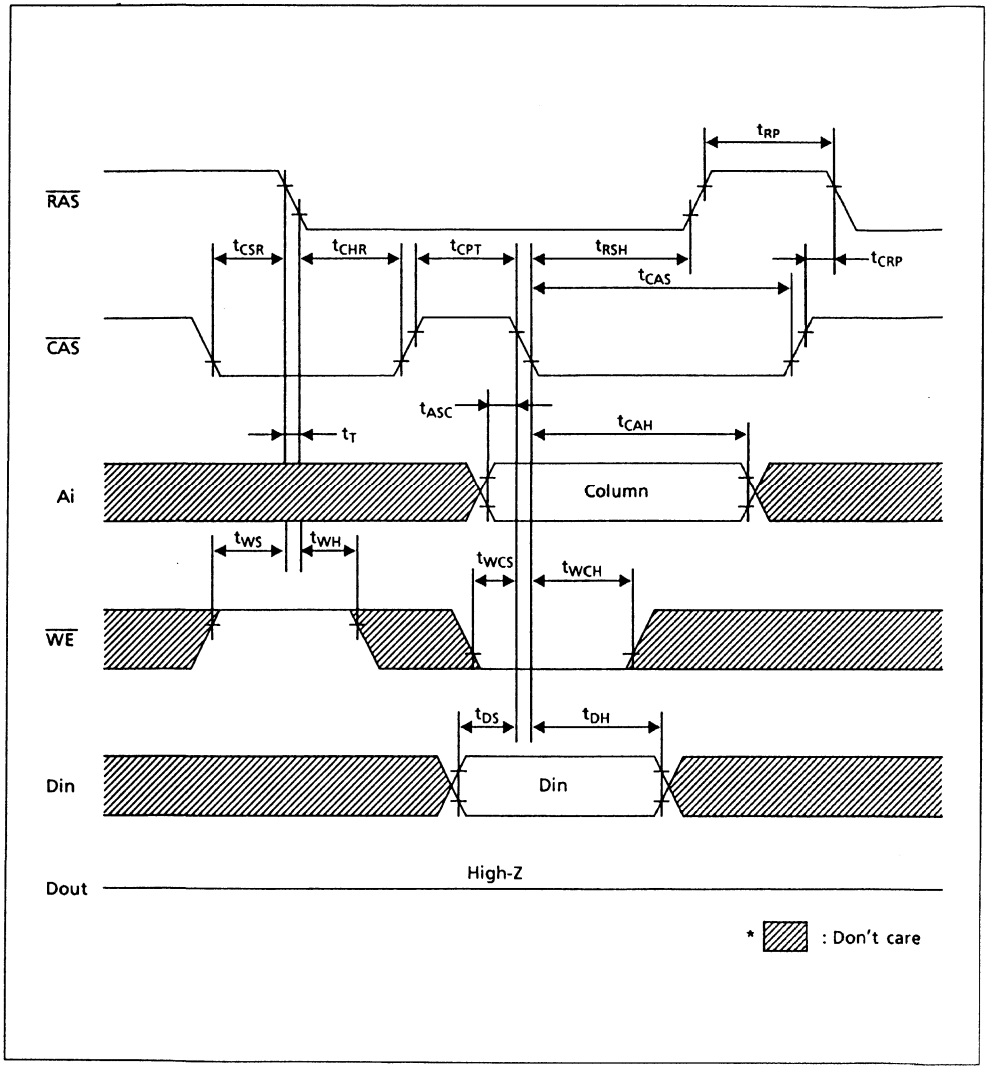
RAS-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM514102 Series

4,194,304-Word × 1-Bit Dynamic RAM

The Hitachi HM514102 is a CMOS dynamic RAM organized 4,194,304-word × 1-bit. HM514102 has realized higher density, higher performance and various functions by employing 0.8 µm CMOS process technology and some new CMOS circuit design technologies. The HM514102 offers static column mode as a high speed access mode.
Multiplexed address input permits the HM514102 to be packaged in standard 20-pin plastic SOJ and 20-pin plastic ZIP.

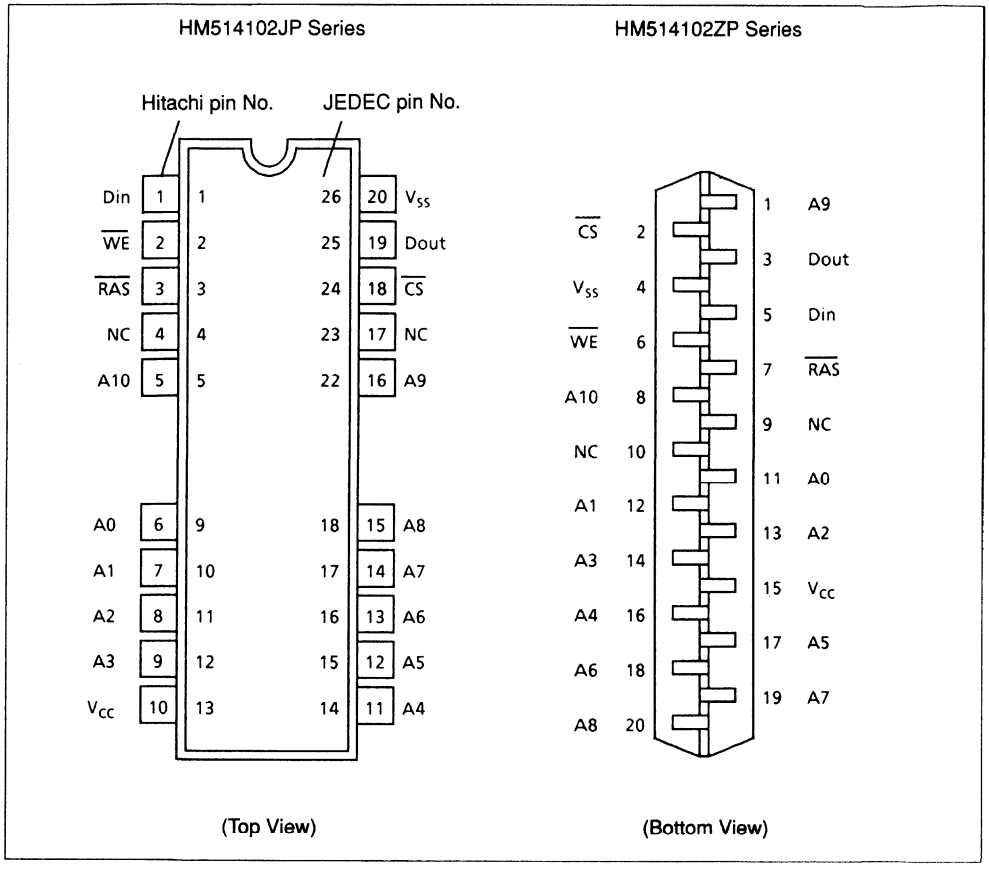
Ordering Information

Type No.	Access time	Package
HM514102JP-8	80 ns	350-mil 20-pin plastic SOJ (CP-20DA)
HM514102JP-10	100 ns	
HM514102JP-12	120 ns	
HM514102ZP-8	80 ns	400-mil 20-pin plastic ZIP (ZP-20)
HM514102ZP-10	100 ns	
HM514102ZP-12	120 ns	

Features

- Single 5 V (±10%)
- High speed
  - Access time
    80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode
    495 mW/440 mW/385 mW (max)
  - Standby mode 11 mW (max)
- Static column mode capability
- 1,024 refresh cycles: (16 ms)
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- Test function

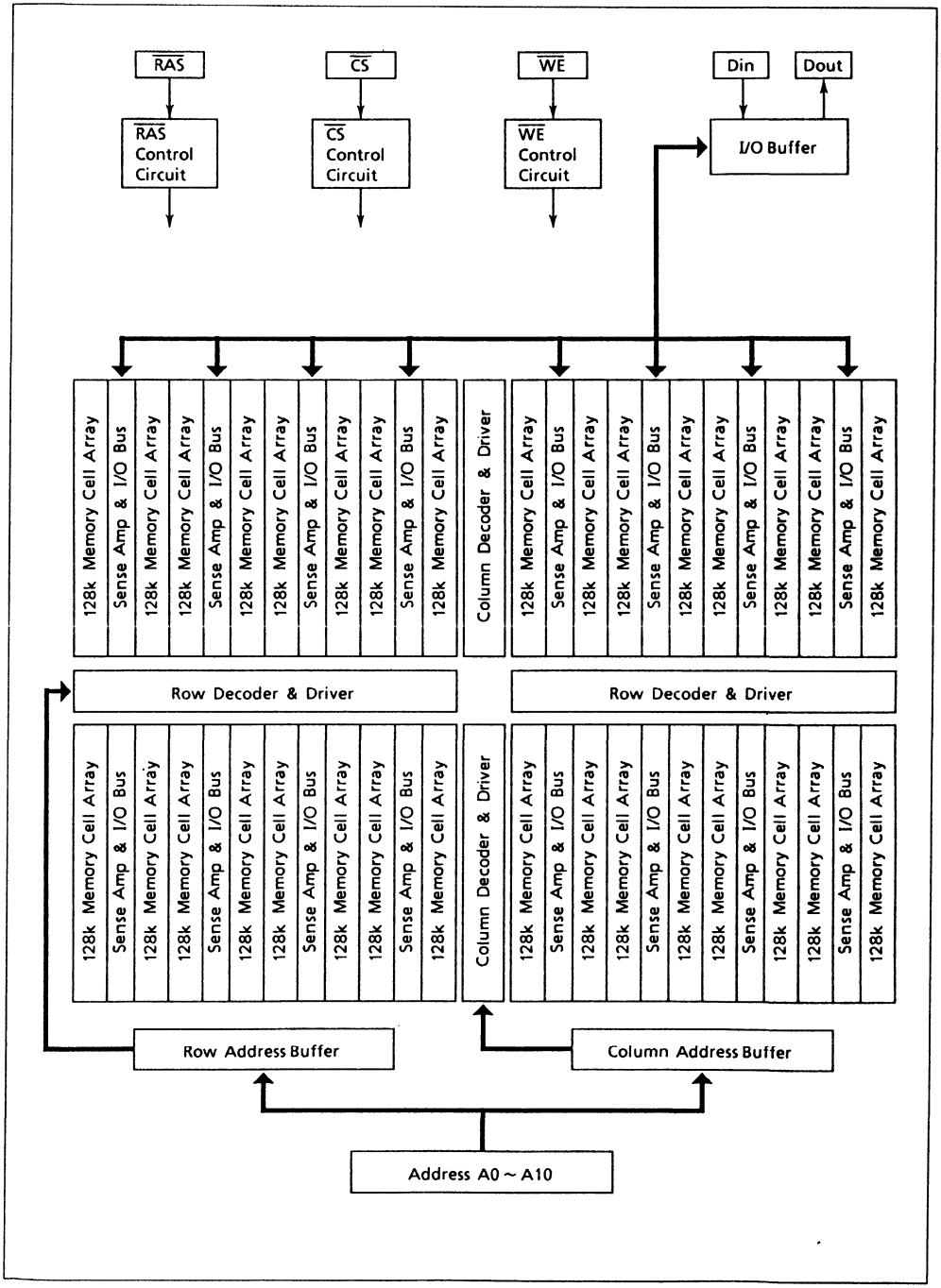
Pin Arrangement



Pin Description

Pin name	Function	Pin name	Function
A0 – A10	Address input	$\overline{CS}$	Chip select
A0 – A9	Refresh address input	$\overline{WE}$	Read/write enable
Din	Data-in	V_{CC}	Power (+5 V)
Dout	Data-out	V_{SS}	Ground
$\overline{RAS}$	Row address strobe	NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−2.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HM514102 -8		HM514102 -10		HM514102 -12				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	90	—	80	—	70	mA	$\overline{RAS}$, $\overline{CS}$ cycling t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z	
		—	1	—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC} − 0.2 V Dout = High-Z	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HM514102 -8		HM514102 -10		HM514102 -12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
$\overline{RAS}$-only refresh current	I_{CC3}	—	90	—	80	—	70	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IL} Dout = enable	1, 5
$\overline{CS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	90	—	80	—	70	mA	t_{RC} = min	5
Static column mode current	I_{CC9}	—	90	—	80	—	70	mA	t_{SC} = min	1, 3, 4
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = −5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.
4. Invalid address is prohibited during static column cycle.
5. Clock voltages ($\overline{RAS}$ and $\overline{CS}$) must be applied simultaneously with or prior to applying supply voltage.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	**Symbol**	**Typ**	**Max**	**Unit**	**Notes**
Input capacitance (Address, data-in)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-out)	C_O	—	7	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout

AC Characteristics (Ta = 0°C to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *17, *18

Test Conditions

Input rise and fall times: 5 ns
Input timing reference levels: 0.8 V, 2.4 V
Output load: 2 TTL gate + C_L (100 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM514102 -8		HM514102 -10		HM514102 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	150	—	180	—	210	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	60	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CS}$ pulse width	t_{SP}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASW}	0	—	0	—	0	—	ns	
Column address hold time	t_{AHW}	15	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CS}$ hold time	t_{CSH}	80	—	100	—	120	—	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{SRS}	5	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	

Read Cycle

Parameter	Symbol	HM514102 -8 Min	HM514102 -8 Max	HM514102 -10 Min	HM514102 -10 Max	HM514102 -12 Min	HM514102 -12 Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	120	ns	2, 3, 19
Access time from $\overline{CS}$	t_{ACS}	—	25	—	25	—	30	ns	3, 4, 19
Access time from address	t_{AA}	—	40	—	45	—	55	ns	3, 5, 14, 19
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	25	0	30	ns	6
$\overline{RAS}$ to column address hold time	t_{AHR}	15	—	15	—	15	—	ns	16
Output hold time from address	t_{AOH}	5	—	5	—	5	—	ns	
Column address hold time to $\overline{RAS}$ on read	t_{AR}	80	—	100	—	120	—	ns	

Write Cycle

		HM514102 -8		HM514102 -10		HM514102 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	20	—	25	—	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	70	—	95	—	115	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	25	—	25	—	30	—	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	25	—	25	—	30	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	20	—	25	—	ns	11
Data in hold time to $\overline{RAS}$	t_{DHR}	70	—	95	—	115	—	ns	
Column address hold time to $\overline{RAS}$ on write	t_{AWR}	70	—	95	—	115	—	ns	

Read-Modify-Write Cycle

		HM514102 -8		HM514102 -10		HM514102 -12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-modify-write cycle time	t_{RWC}	180	—	210	—	245	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	—	100	—	120	—	ns	10
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	25	—	25	—	30	—	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	40	—	45	—	55	—	ns	10, 13
Output hold time from $\overline{WE}$	t_{WOH}	0	—	0	—	0	—	ns	

Refresh Cycle

Parameter	Symbol	HM514102 -8 Min	HM514102 -8 Max	HM514102 -10 Min	HM514102 -10 Max	HM514102 -12 Min	HM514102 -12 Max	Unit	Notes
$\overline{CS}$ setup time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CS}$ hold time ($\overline{CS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CS}$ hold time	t_{ZRH}	10	—	10	—	10	—	ns	
$\overline{CS}$ precharge time in normal mode	t_{CPN}	10	—	10	—	15	—	ns	

Static Column Mode Cycle

Parameter	Symbol	HM514102 -8 Min	HM514102 -8 Max	HM514102 -10 Min	HM514102 -10 Max	HM514102 -12 Min	HM514102 -12 Max	Unit	Notes
Static column mode cycle time	t_{SC}	45	—	50	—	60	—	ns	
Static column mode $\overline{RAS}$ pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	
$\overline{RAS}$ to second $\overline{WE}$ delay time	t_{RSWD}	80	—	100	—	120	—	ns	
Static column mode $\overline{CS}$ precharge time	t_{SI}	10	—	10	—	15	—	ns	
Write invalid time	t_{WI}	10	—	10	—	15	—	ns	

Static Column Mode Read-Modify-Write and Mixed Cycle

Parameter	Symbol	HM514102 -8 Min	HM514102 -8 Max	HM514102 -10 Min	HM514102 -10 Max	HM514102 -12 Min	HM514102 -12 Max	Unit	Notes
Static column mode cycle time on read-modify-write	t_{SRW}	90	—	100	—	120	—	ns	12
Access time from previous $\overline{WE}$	t_{ALW}	—	80	—	90	—	110	ns	3, 13, 19
Previous $\overline{WE}$ to column address delay time	t_{LWAD}	20	40	25	45	30	55	ns	15
Column address hold time to previous $\overline{WE}$	t_{AHLW}	80	—	90	—	110	—	ns	
Output enable time from $\overline{WE}$	t_{OW}	—	30	—	30	—	35	ns	

Test Mode Cycle

Parameter	Symbol	HM514102 -8 Min	HM514102 -8 Max	HM514102 -10 Min	HM514102 -10 Max	HM514102 -12 Min	HM514102 -12 Max	Unit	Notes
Test mode $\overline{WE}$ setup time	t_{WS}	0	—	0	—	0	—	ns	
Test mode $\overline{WE}$ hold time	t_{WH}	20	—	20	—	20	—	ns	

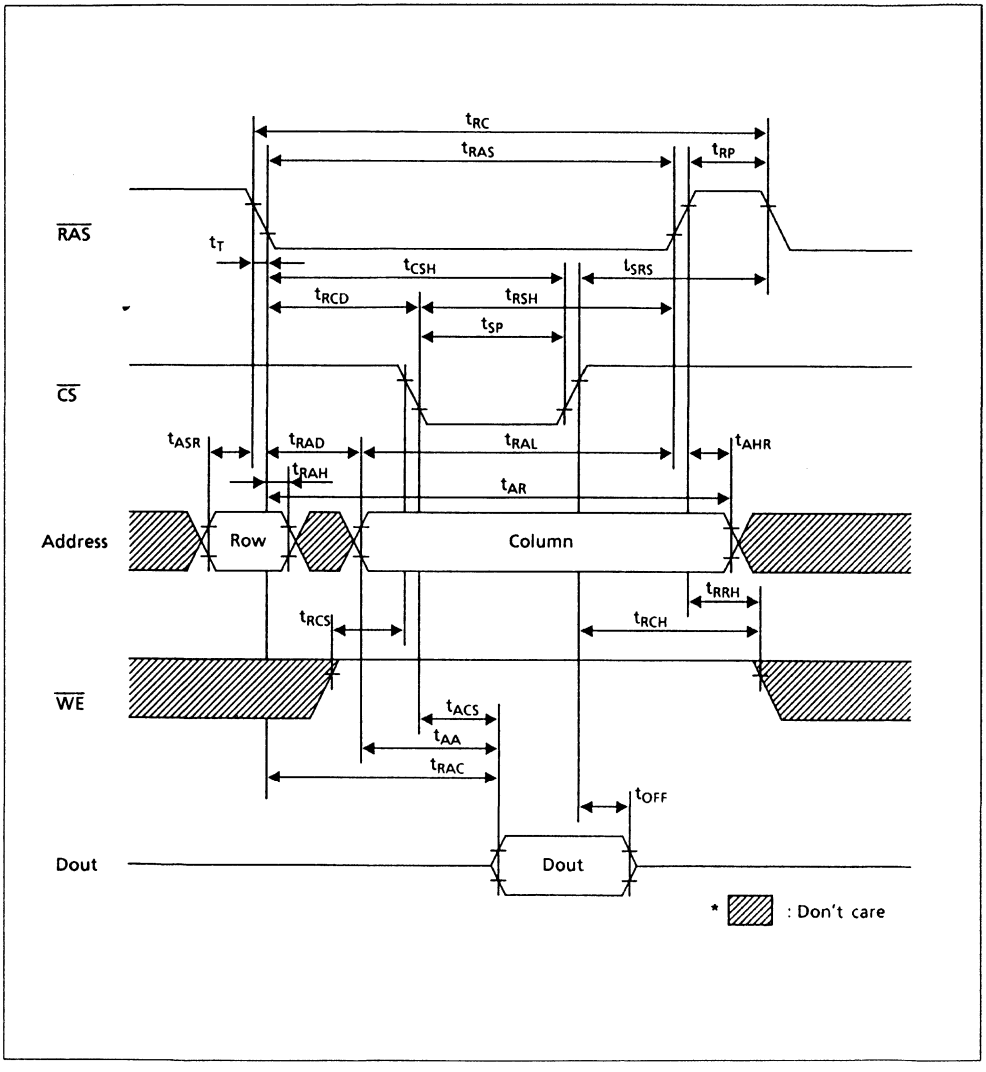
Counter Test Cycle

Parameter	Symbol	HM514102 -8 Min	HM514102 -8 Max	HM514102 -10 Min	HM514102 -10 Max	HM514102 -12 Min	HM514102 -12 Max	Unit	Notes
$\overline{CAS}$ precharge time in counter test cycle	t_{CPT}	40	—	50	—	60	—	ns	

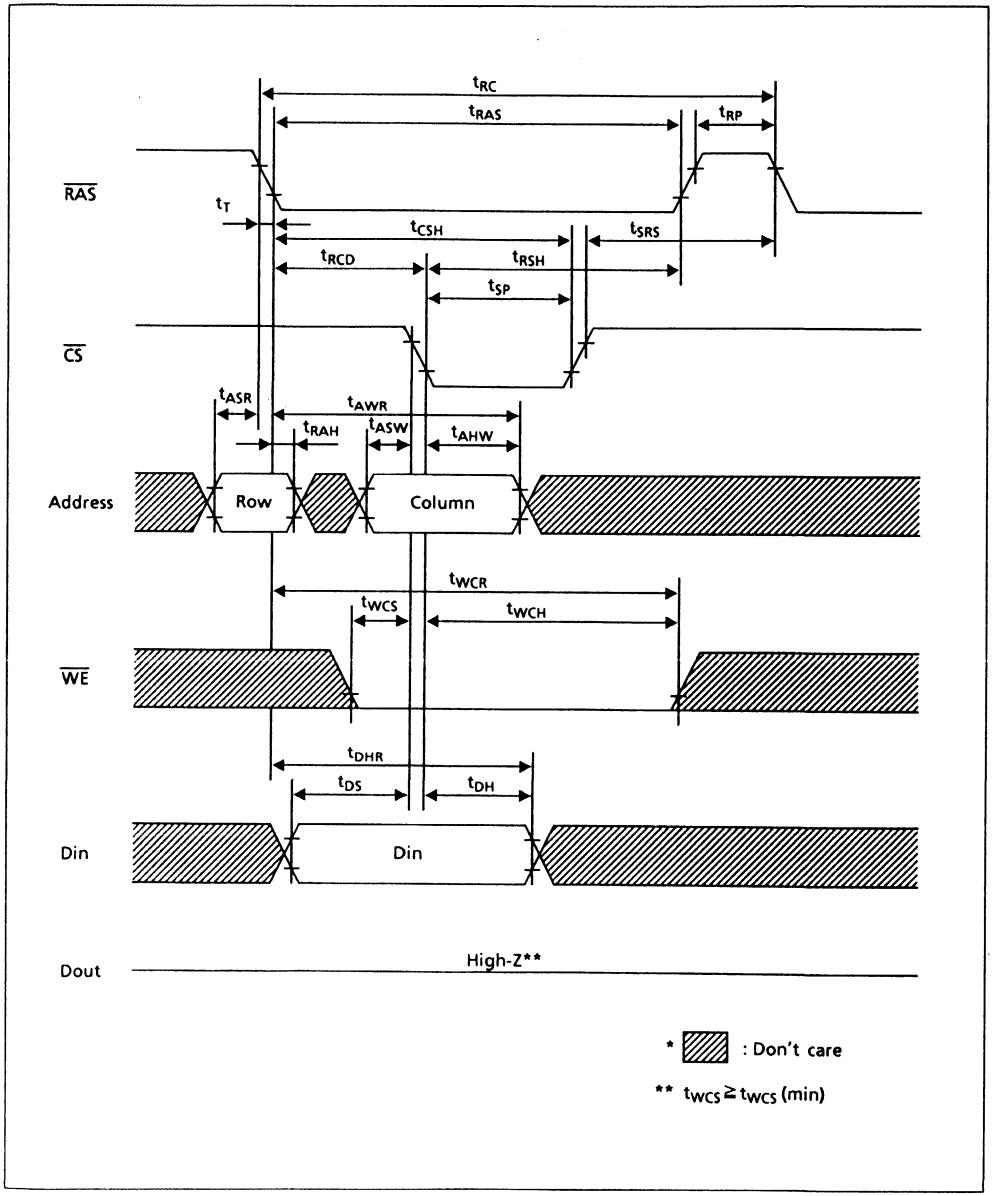
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{ACS}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CS}$ leading edge in an early write cycle and to $\overline{WE}$ leading edge in a delayed write or a read-modify-write cycle.
12. t_{SRW} (min) = t_{AWD} (min) + t_{LWAD} (max) + t_T
13. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{WAD} is greater than the maximum recommended value shown in this table, t_{ALW} exceeds the value shown.
14. Assumes that $t_{LWAD} \geq t_{LWAD}$ (max).
15. Operation with the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met, t_{LWAD} (max) is specified as a reference point only, if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AHR} defines the time at which the column address hold.
17. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CS}$-before-$\overline{RAS}$ refresh cycles is required. Clock voltages ($\overline{RAS}$ and $\overline{CS}$) must be applied simultaneously with or prior to applying supply voltage.
18. Test mode operation specified in this data sheet is 8-bit test function controlled by control address bits – RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$-and-$\overline{CS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is Dout and data input pin is Din. In order to end this test mode operation, perform a $\overline{RAS}$-only refresh cycle or a $\overline{CS}$-before-$\overline{RAS}$ refresh cycle.
19. In a test mode read cycle, the value of t_{RAC}, t_{ACS}, t_{AA}, t_{OW} and t_{ALW} are delayed for 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

Timing Waveforms

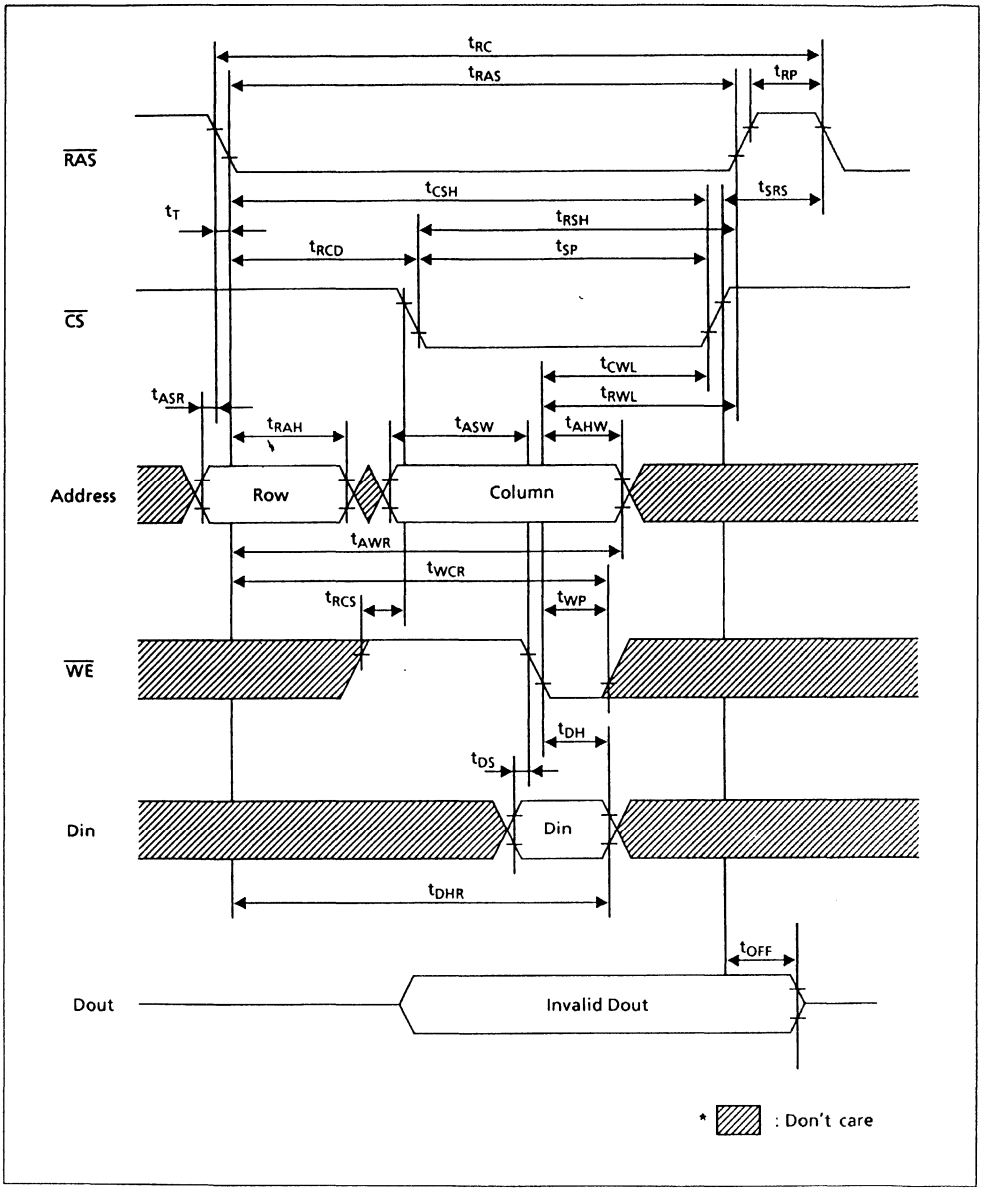
Read Cycle



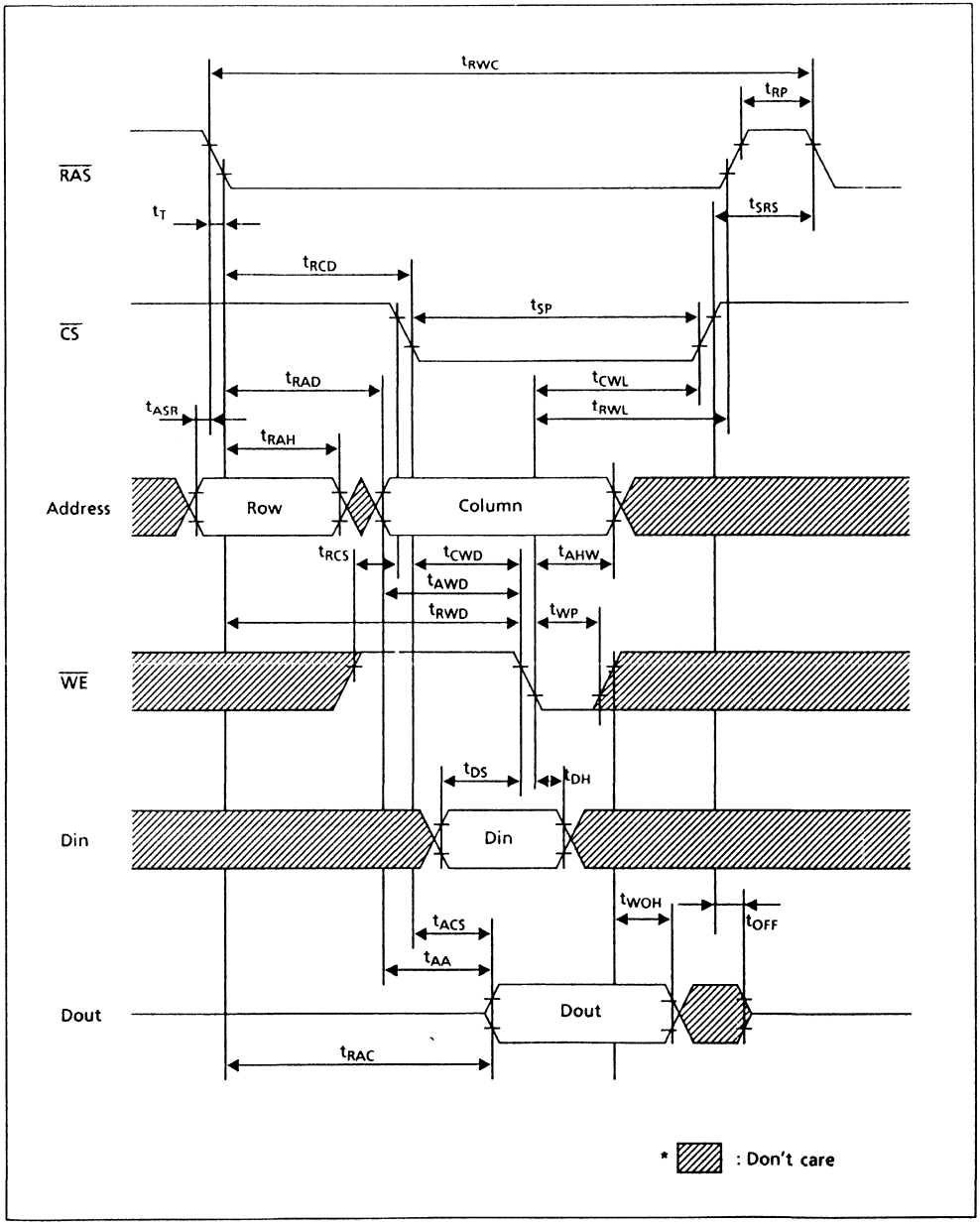
Early Write Cycle



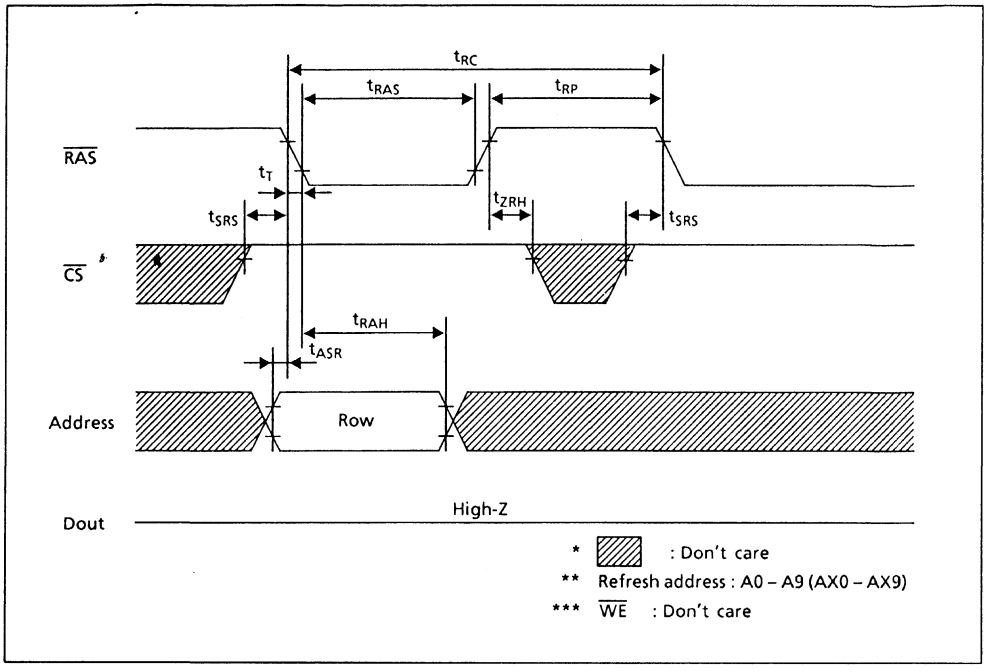
Delayed Write Cycle



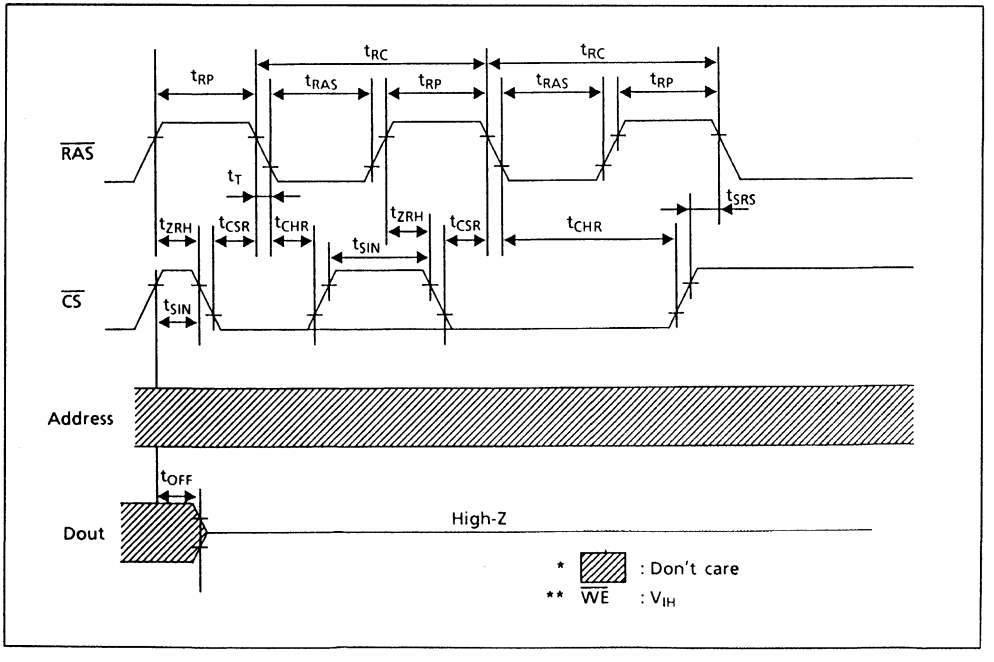
Read-Modify-Write Cycle



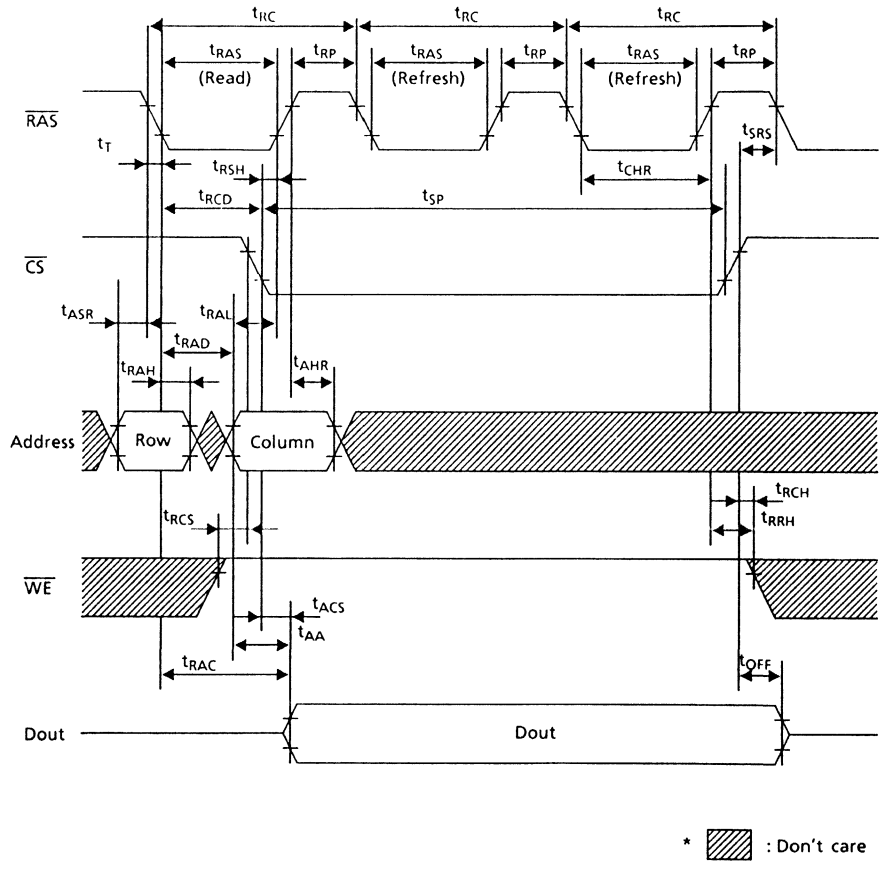
$\overline{RAS}$-Only Refresh Cycle



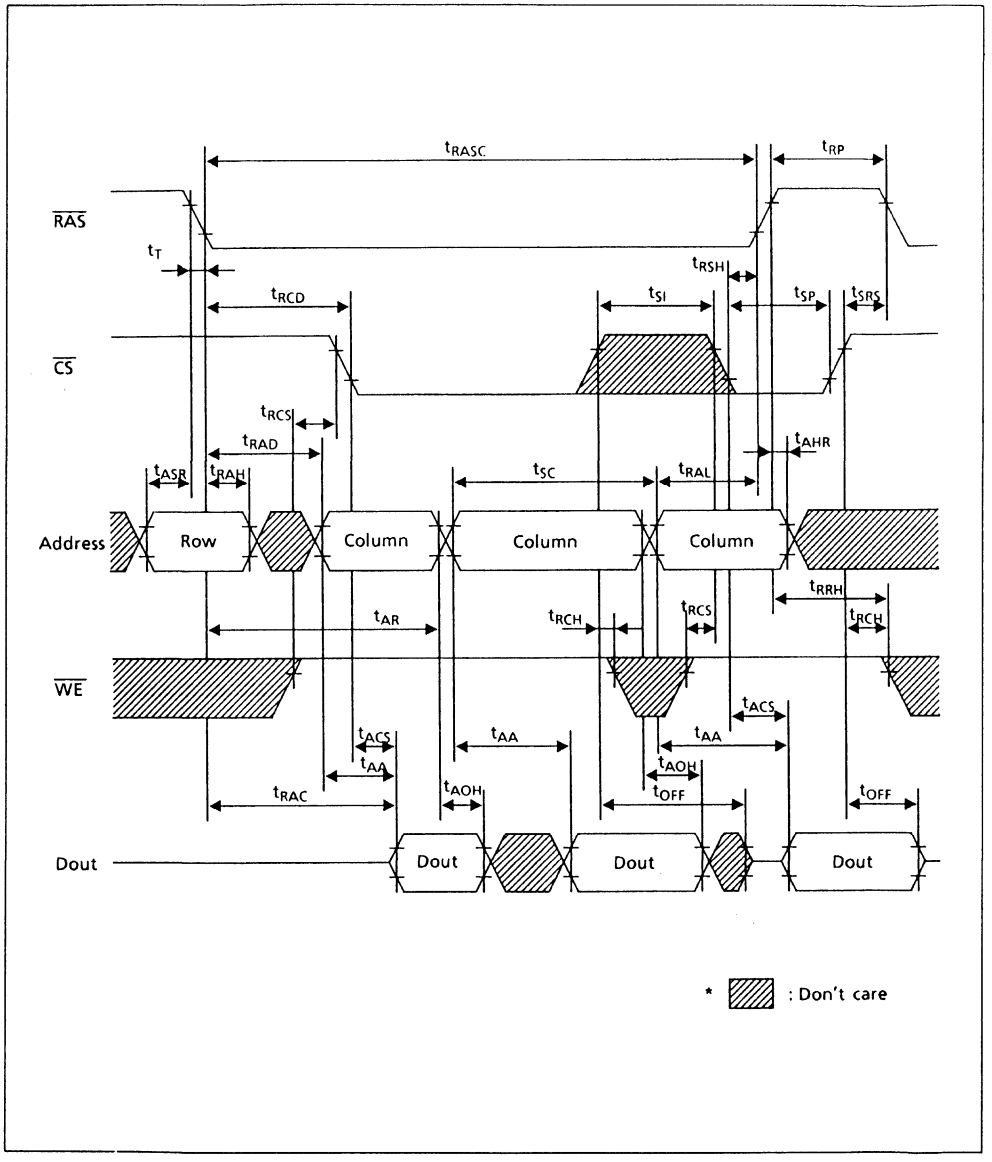
$\overline{CS}$-Before-$\overline{RAS}$ Refresy Cycle



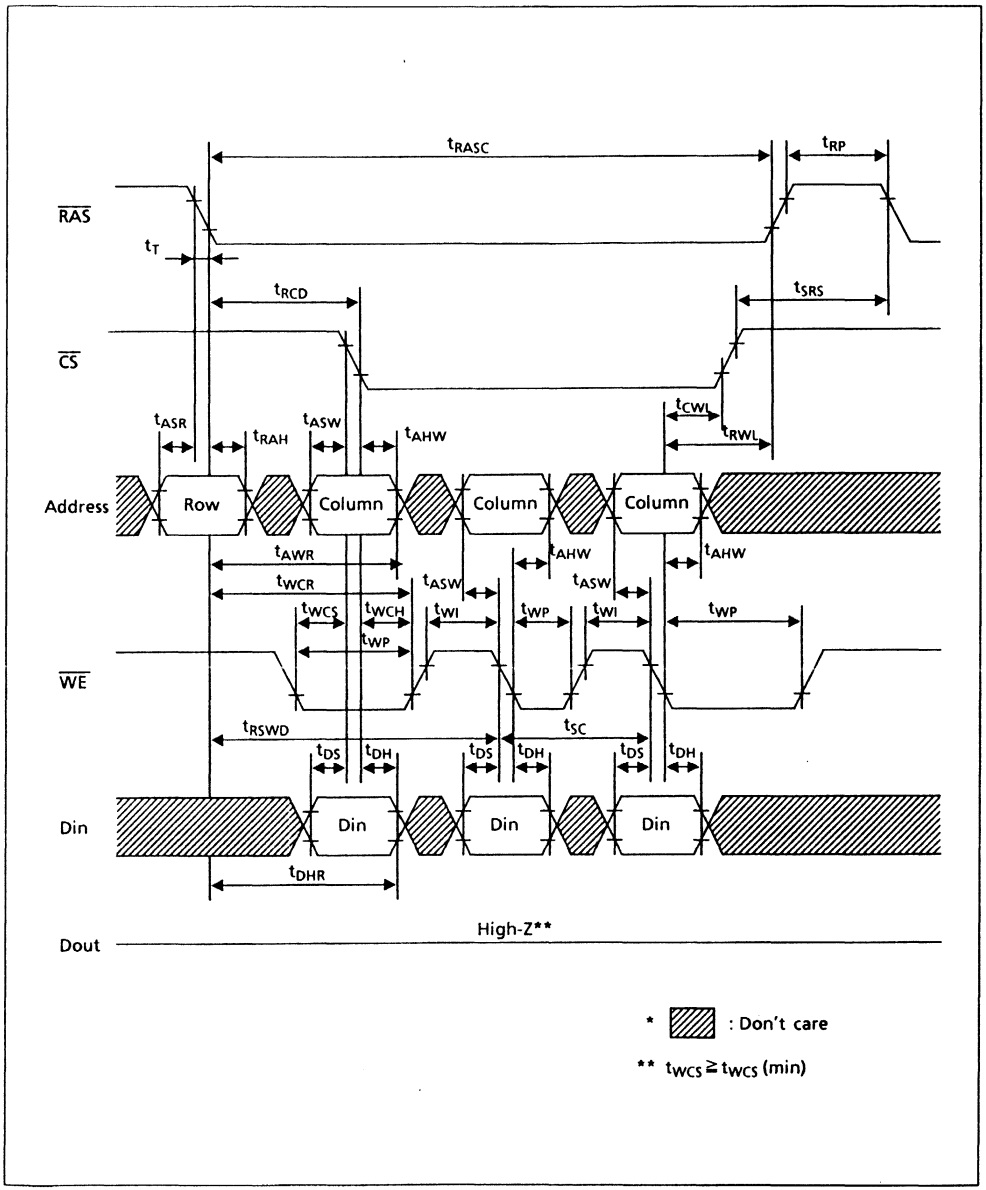
Hidden Refresh Cycle



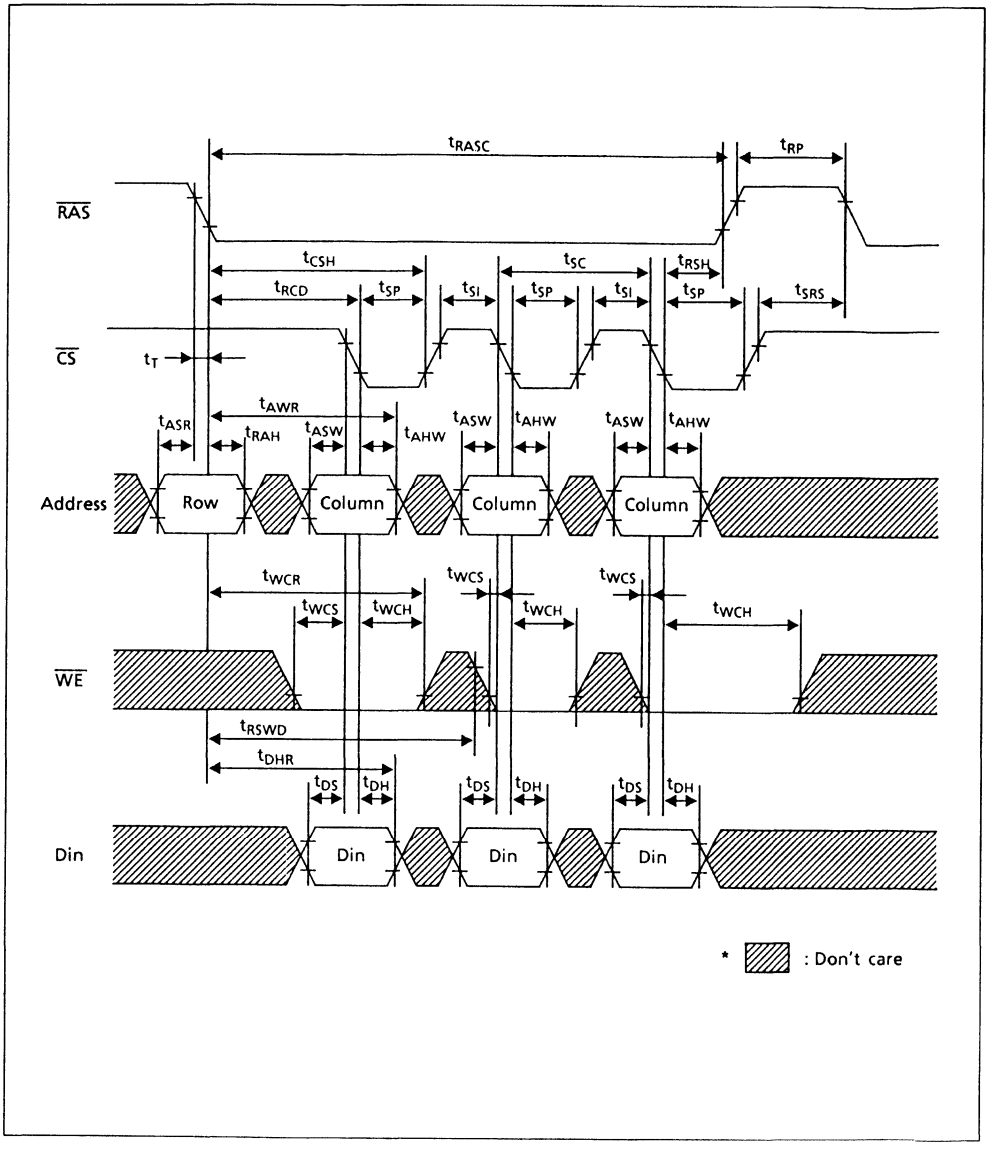
Static Column Mode Read Cycle



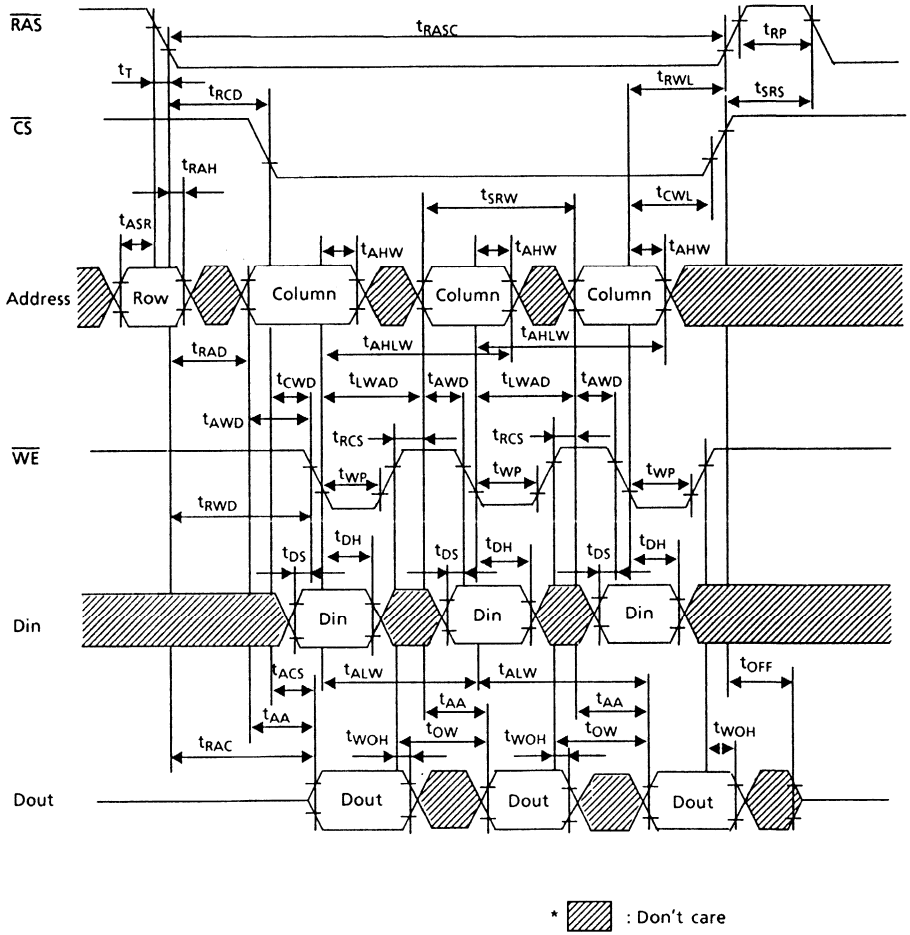
Static Column Mode Write Cycle (1)



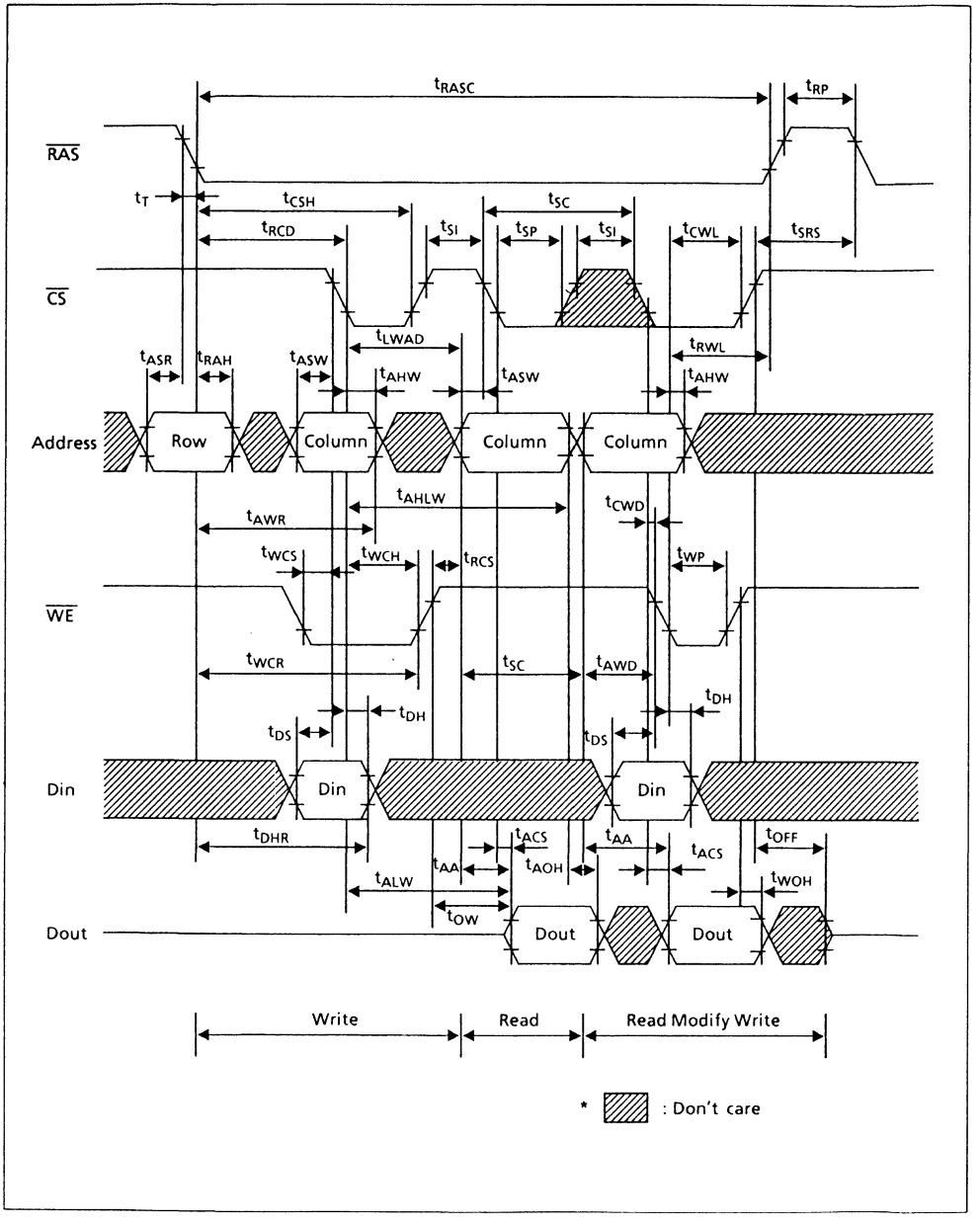
Static Column Mode Write Cycle (2)



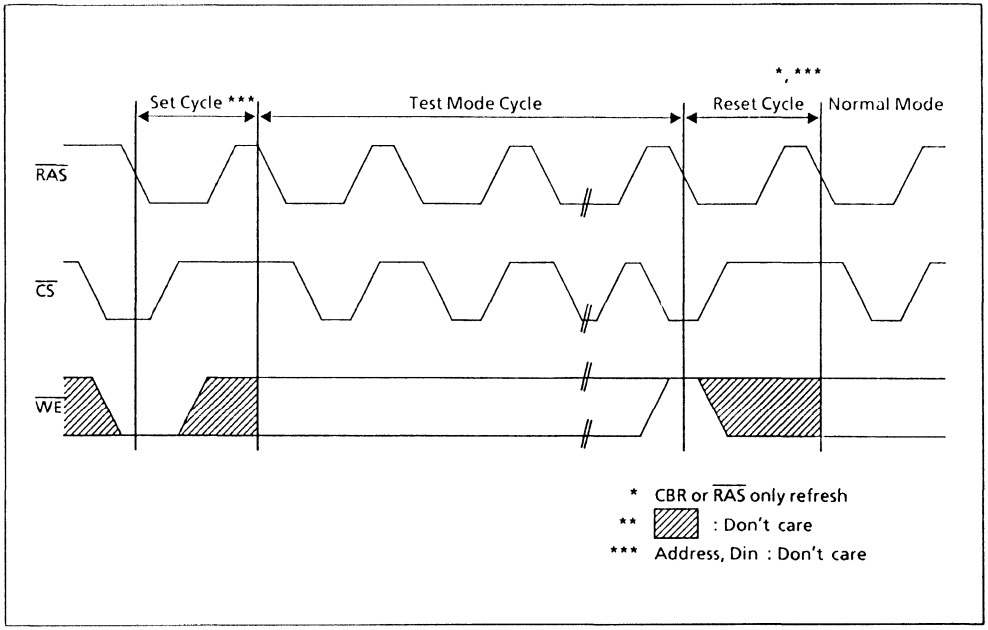
Static Column Mode Read-Modify-Write Cycle



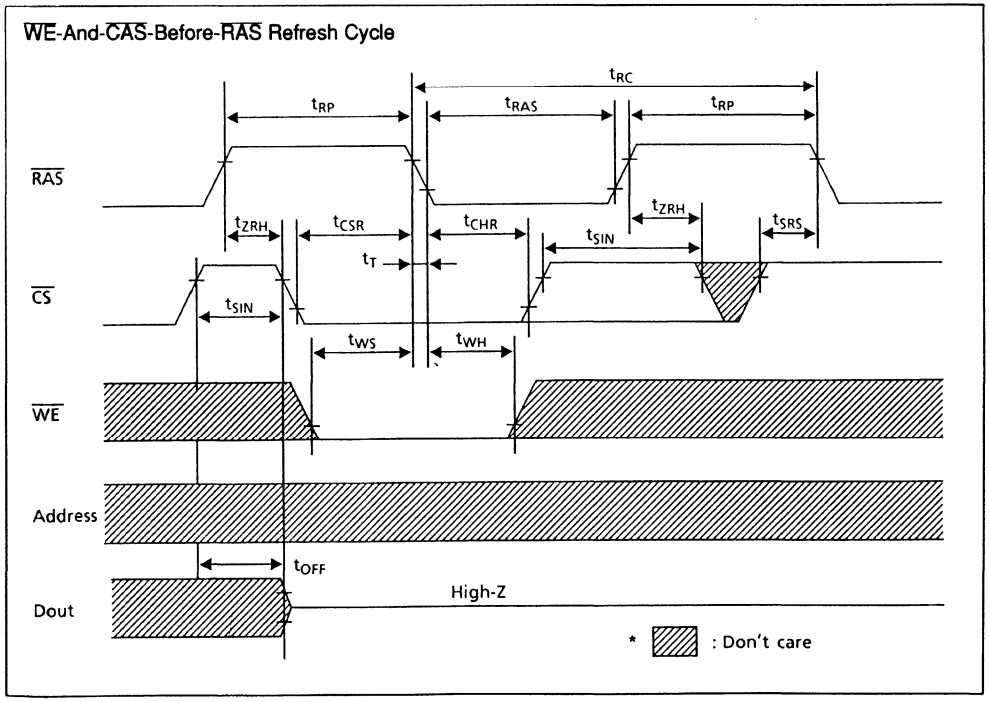
Static Column Mode Mixed Cycle



Test Mode Cycle

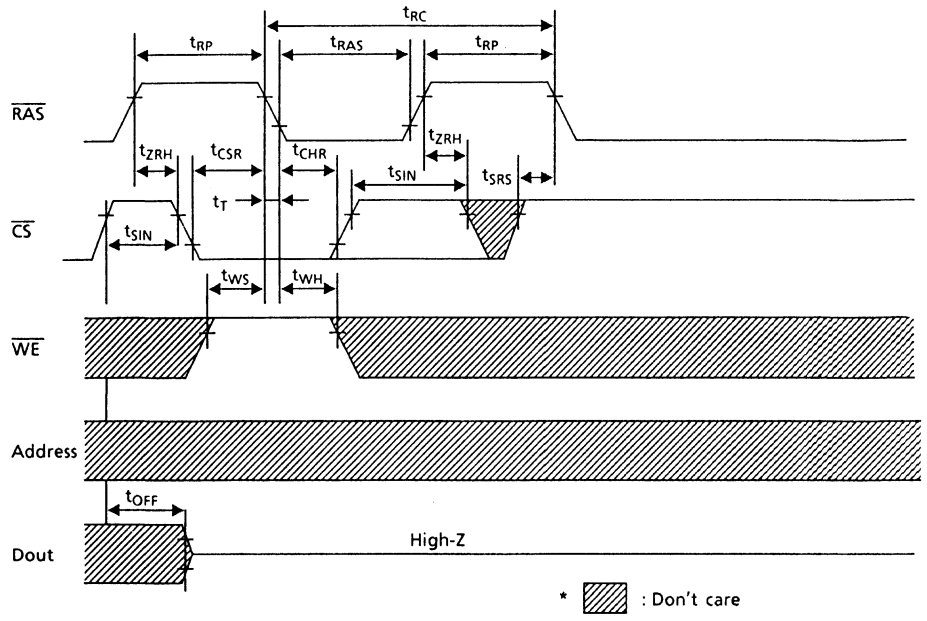


Test Mode Set Cycle

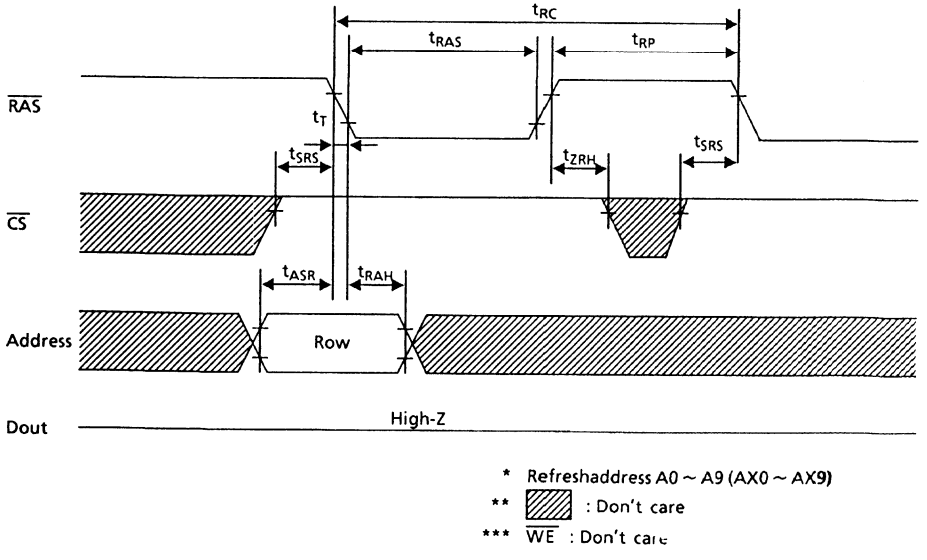


Test Mode Reset Cycle

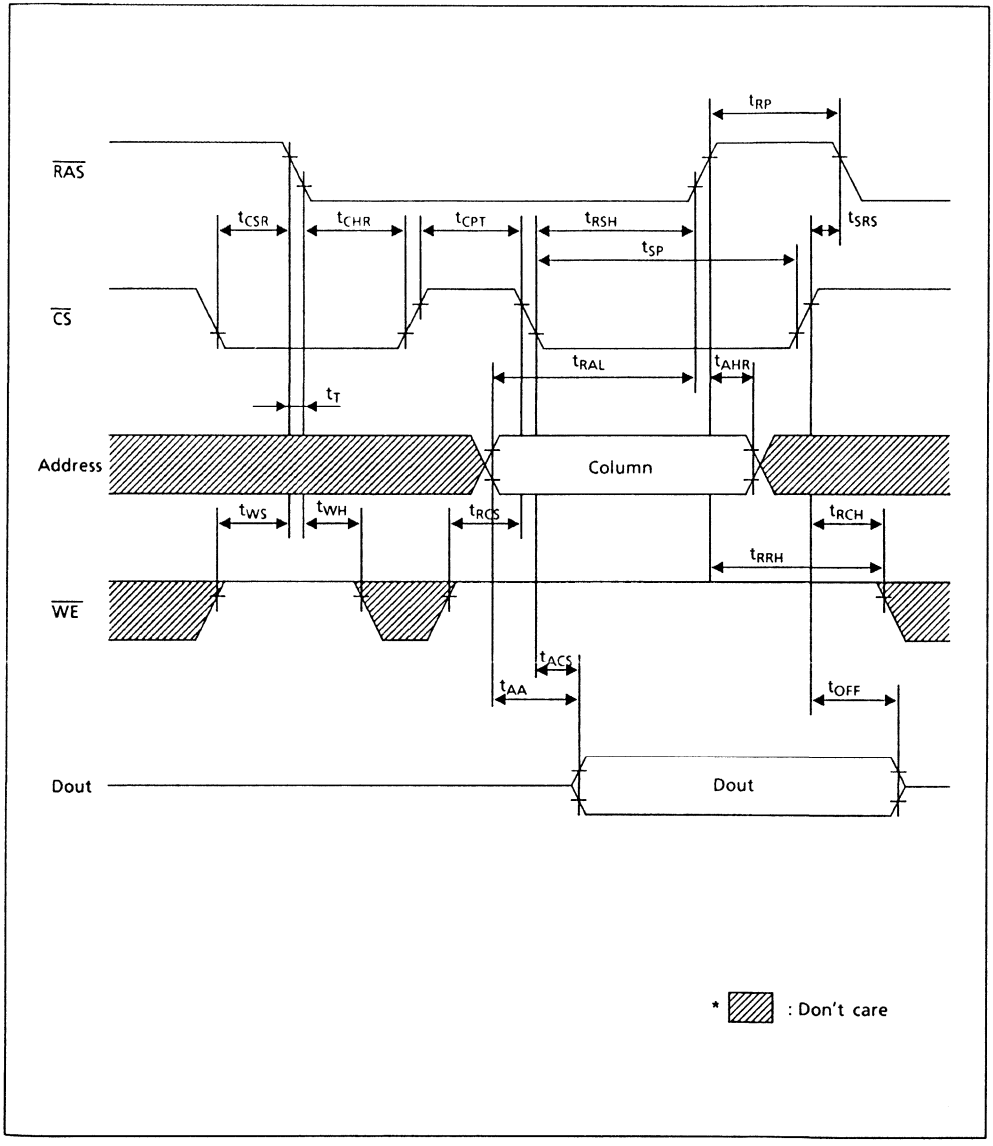
$\overline{CS}$-Before-$\overline{RAS}$ Refresh Cycle



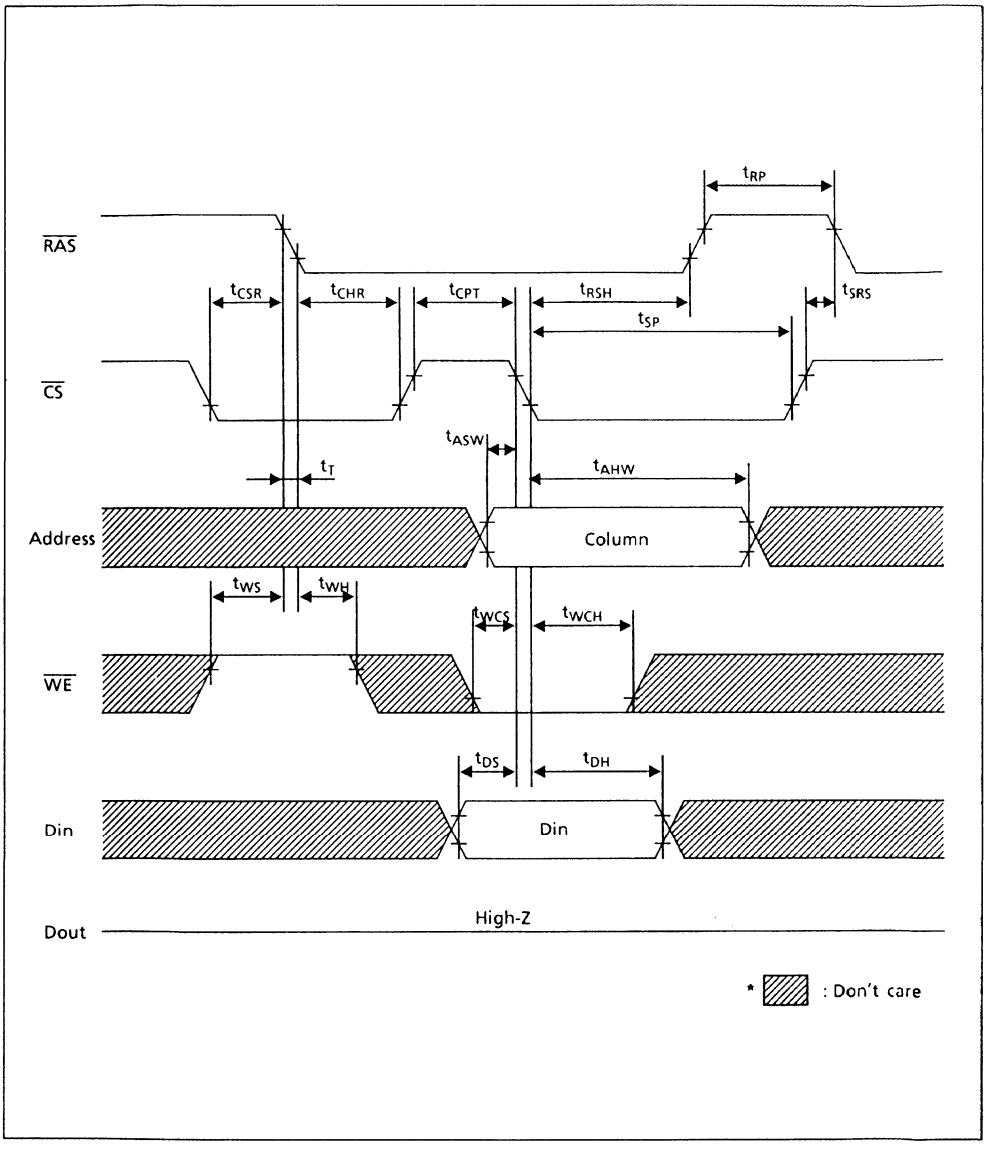
$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Read)



$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Check Cycle (Write)



HM574256 Series — Preliminary

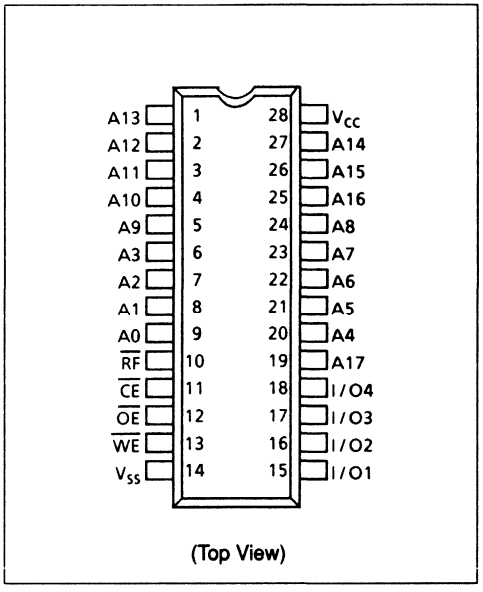
262,144 -Word × 4-Bit High Speed Dynamic Random Access Memory

The Hitachi HM574256 is a super high speed dynamic RAM organized 262,144-word × 4-bit. HM574256 has realized higher density, higher performance and various functions by employing 1.3 µm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM574256 offers 2 bits static column mode as a high speed access mode.

Features

- Single 5 V (± 10%) for HM574256JP-40/45
  5 V (± 5%) for HM574256JP-35R
- High speed
  - Access time: 35 ns/40 ns/45 ns (max)
- 512 refresh cycles: 4 ms
- 2 variations of refresh
  - $\overline{CE}$ refresh
  - Automatic refresh
- 2 bits static column mode

Pin Arrangement



(Top View)

Ordering Information

Type No.	Access time	Package
HM574256JP-35R	35 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM574256JP-40	40 ns	
HM574256JP-45	45 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Description

Pin name	Function
A0 – A8	Address input for $\overline{CE}$ refresh
A9 – A16	Address input
A17	Address input for static column mode
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Read/write enable
I/O1 – I/O4	Data in/data out
$\overline{RF}$	Refresh control
V_{CC}	Power (+5 V)
V_{SS}	Ground

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_T	0.8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	-35R -40/45	V_{CC}	4.75 4.50	5.0	5.25 5.50	V	1
Input high voltage		V_{IH}	2.4	—	6.5	V	1, 3
Input low voltage		V_{IL}	−1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the −2 V level with a maximum pulse width of 20 ns at the −1.5 V level. (See figure 1.)
3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC} +0.5 V.

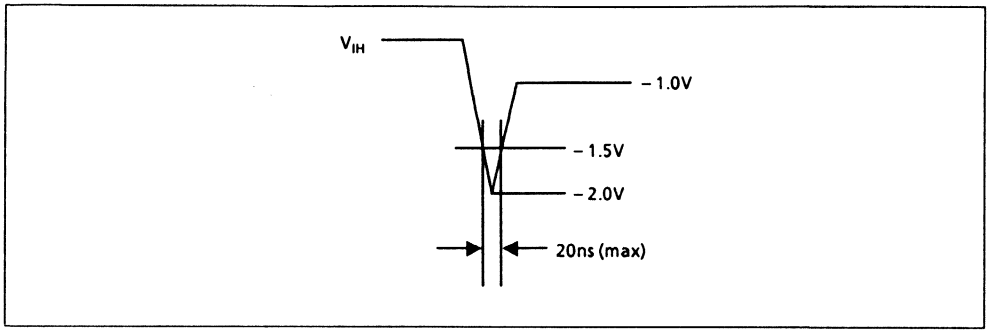


Figure 1 Undershoot of input voltage

DC Characteristics

(Ta = 0 to +70°C, V_{SS} = 0 V, V_{CC} = 5 V ± 10% for HM574256JP-40/45,
V_{CC} = 5 V ± 5% for HM574256JP-35R)

		HM574256-35R		HM574256-40		HM574256-45				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Normal operating current	I_{CCA}	—	TBD	—	TBD	—	TBD	mA		1
Refresh current	I_{CCR}	—	TBD	—	TBD	—	TBD	mA		1
Standby current	I_{CCS}	—	5	—	5	—	5	mA		
Input leakage current	I_{LI}	−10	10	−10	10	−10	10	µA	0 V < Vin < 7 V	
Output leakage current	I_{LO}	−10	10	−10	10	−10	10	µA	0 V < Vout < 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = −4 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 8 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10% for HM574256JP-40/45, V_{CC} = 5 V ± 5% for HM574256JP-35R)

Parameter		Symbol	Typ	Max	Unit	Note
Input capacitance	Address, data-in	Cin1	—	5	pF	1
	Clock ($\overline{CE}$, $\overline{OE}$)	Cin2	—	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	Cin3	—	7	pF	1
Output capacitance (data-in/data-out)		$C_{I/O}$	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable Dout.

AC Characteristics *1 (Ta = 0 to +70°C, V_{SS} = 0 V, V_{CC} = 5 V ± 10% for HM574256JP-40/45, V_{CC} = 5 V ± 5% for HM574256JP-35R)

Test Conditions

- Input pulse levels: V_{IH} = 3.0 V, V_{IL} = 0 V
- Transition time: t_T = 3 ns
- Input timing reference levels: high = 2.4 V, low = 0.8 V (See figure 2.)
- Output timing reference levels: high = 2.4 V, low = 0.4 V
- Output load: See figure 3.

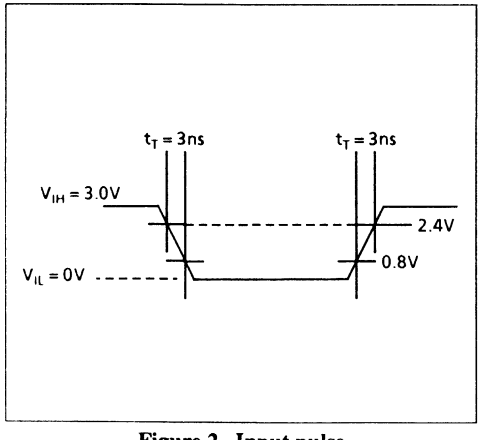


Figure 2 Input pulse

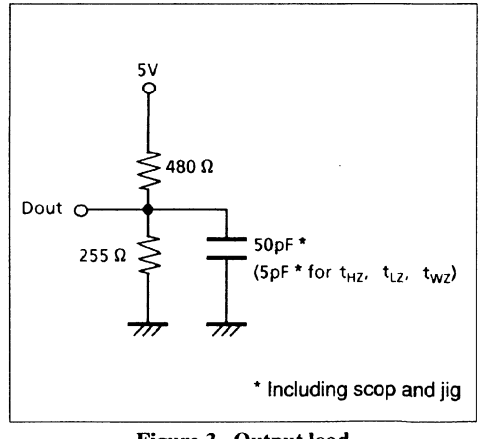


Figure 3 Output load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM574256-35R		HM574256-40		HM574256-45			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read/write cycle time	t_{CC}	75	—	85	—	90	—	ns	
$\overline{CE}$ pulse width	t_{CE}	35	5000	40	5000	45	5000	ns	
$\overline{CE}$ precharge time	t_{CP}	34	—	39	—	39	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	
Address hold time	t_{AH}	5	—	5	—	5	—	ns	
Transition time (rise and fall)	t_T	1	10	1	10	1	10	ns	
Refresh period	t_{REF}	—	4	—	4	—	4	ms	

Read Cycle

		HM574256-35R		HM574256-40		HM574256-45			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address access time	t_{AA}	—	25	—	30	—	30	ns	
Access time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup time on read	t_{RS}	0	—	0	—	0	—	ns	
Hold time on read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ setup time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ enable to output in low-Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ disable to output in high-Z	t_{HZ}	—	15	—	20	—	20	ns	
Output hold time from address	t_{AOH}	3	—	3	—	3	—	ns	
Output hold time from $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ precharge time	t_{COP}	10	—	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Notes
Data setup time	t_{DW}	20	—	25	—	30	—	ns	
Data hold time	t_{DH}	5	—	5	—	5	—	ns	
Setup time on early write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ pulse width	t_{WP}	25	—	30	—	35	—	ns	
Write hold time from $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ enable to output in high-Z	t_{WZ}	—	15	—	20	—	20	ns	
$\overline{OE}$ to Din delay time	t_{ODD}	15	—	20	—	20	—	ns	
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	15	—	20	—	20	—	ns	
$\overline{CE}$ setup time from Din	t_{DZC}	0	—	0	—	0	—	ns	

Read-Modify-Write Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Notes
$\overline{WE}$ delay time from $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

Refresh Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Notes
$\overline{RF}$ setup time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ hold time	t_{FH}	15	—	15	—	15	—	ns	
Mode selection setup time	t_{MS}	0	—	0	—	0	—	ns	
Mode selection hold time	t_{MH}	15	—	20	—	20	—	ns	
Setup time on $\overline{CE}$ refresh	t_{CRS}	15	—	20	—	20	—	ns	

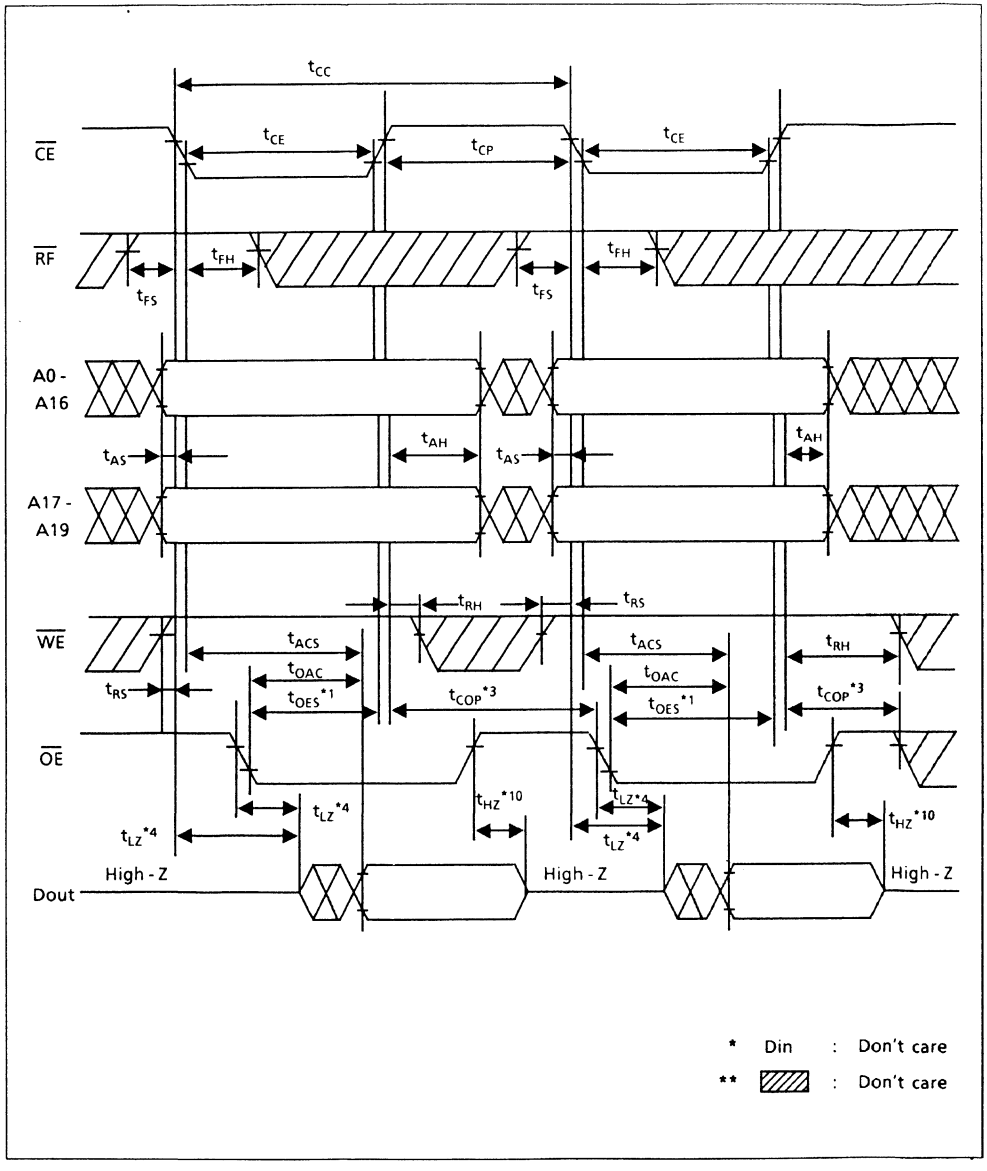
Static Column Mode Cycle

Parameter	Symbol	HM574256-35R Min	HM574256-35R Max	HM574256-40 Min	HM574256-40 Max	HM574256-45 Min	HM574256-45 Max	Unit	Notes
Static column address setup time	t_{ASZ}	20	—	25	—	25	—	ns	
Address setup time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address hold time from $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

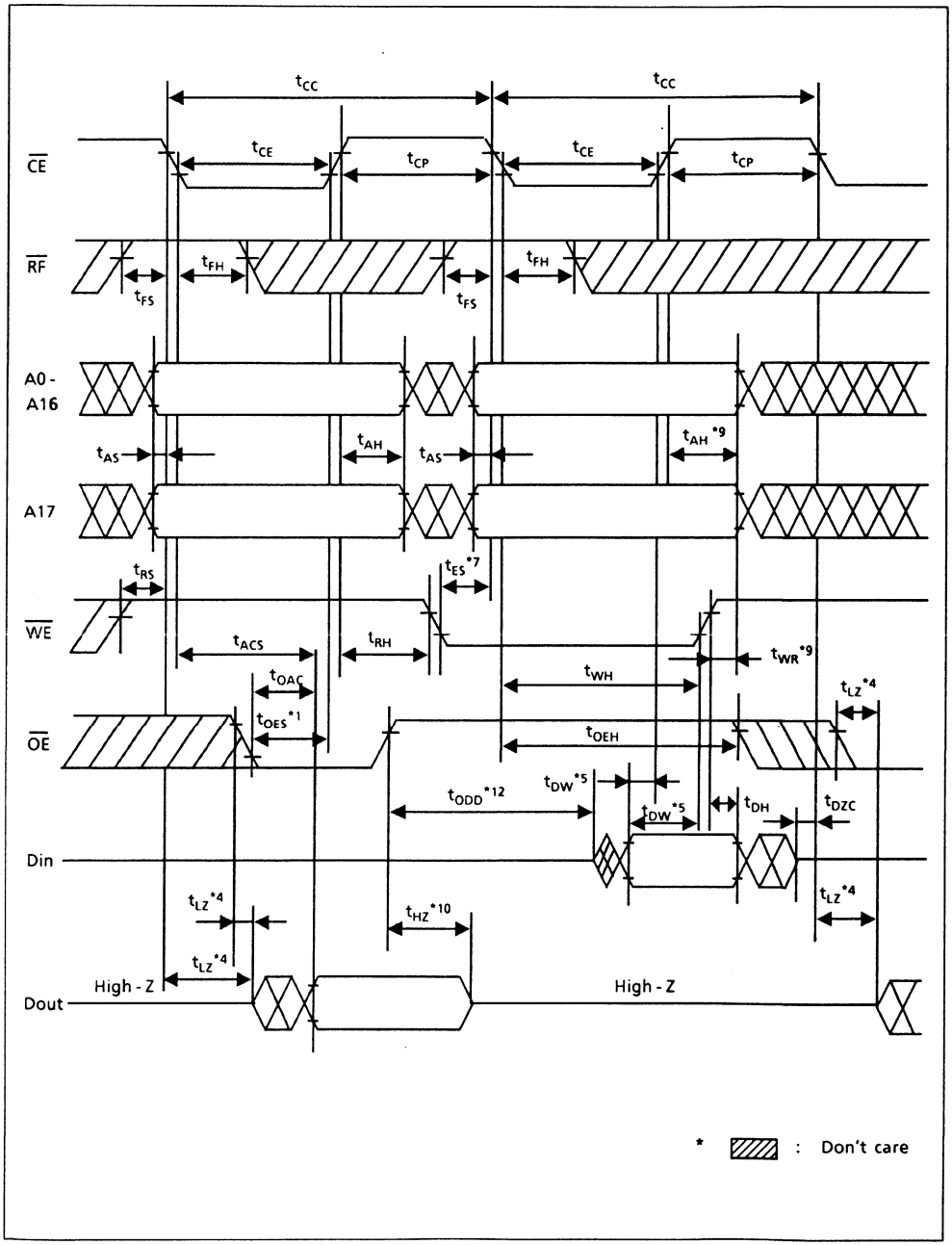
Notes:
1. If $t_{OES} > t_{OES}$ (min) and $\overline{OE}$ is held at low level, Dout will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisfied for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min), Dout cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.
6. When $\overline{WE}$ goes low, Dout becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, Dout is controlled by $\overline{CE}$. t_{WZ} is defined as the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min), the cycle is early write and Dout is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisfied for a write cycle.
10. t_{HZ} is defined as the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. When I/O pins are in the output state, data-in shall not be applied to I/O pins. So, in all write cycles (early write, delayed write and read-modify-write), $\overline{OE}$ must go to high level to disable the output buffer prior to applying data to the device.
13. In static column mode cycle, there must not be any invalid address inputs for static column mode (A17) which are less than t_{AA}.

Timing Waveforms

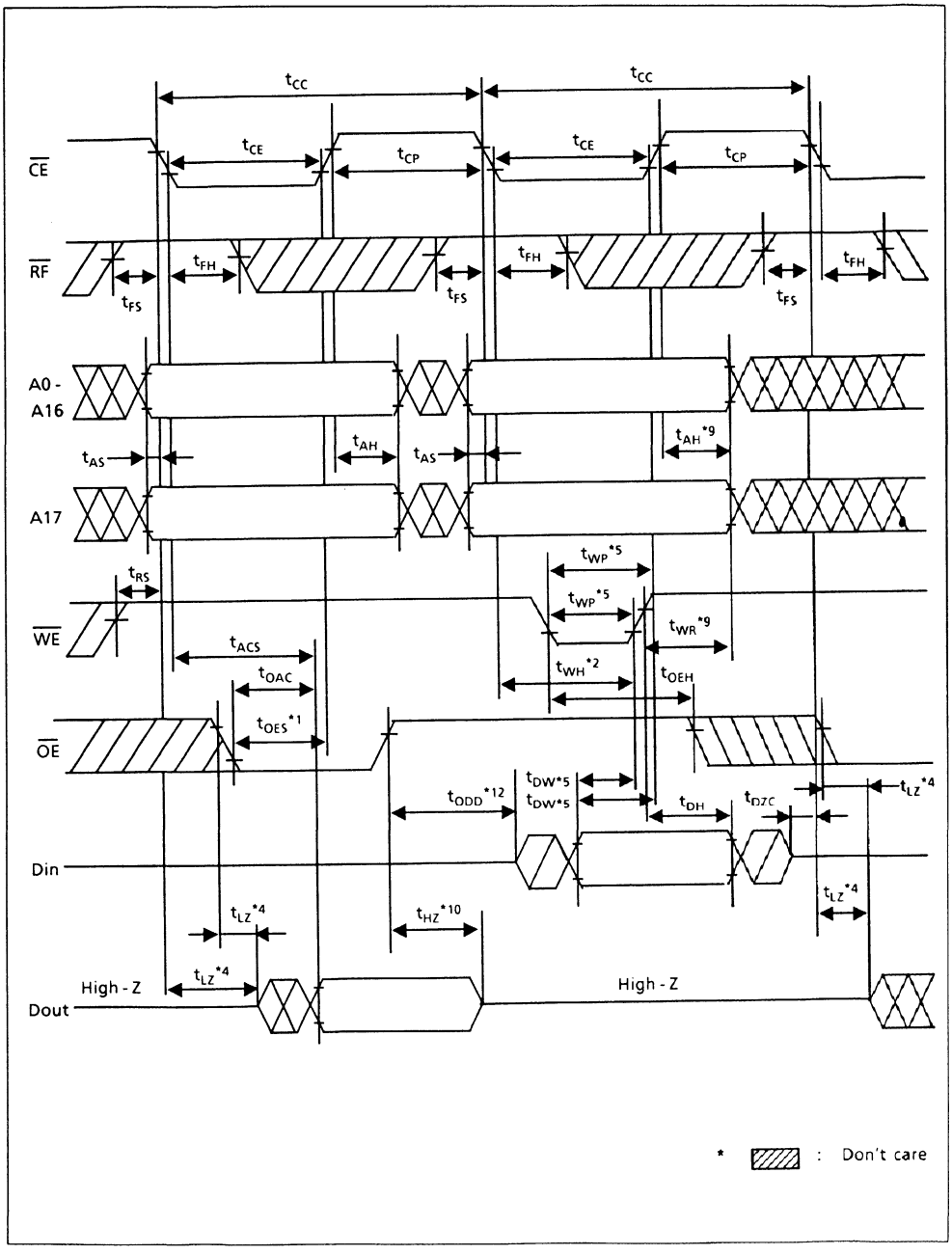
Read/Read Cycle



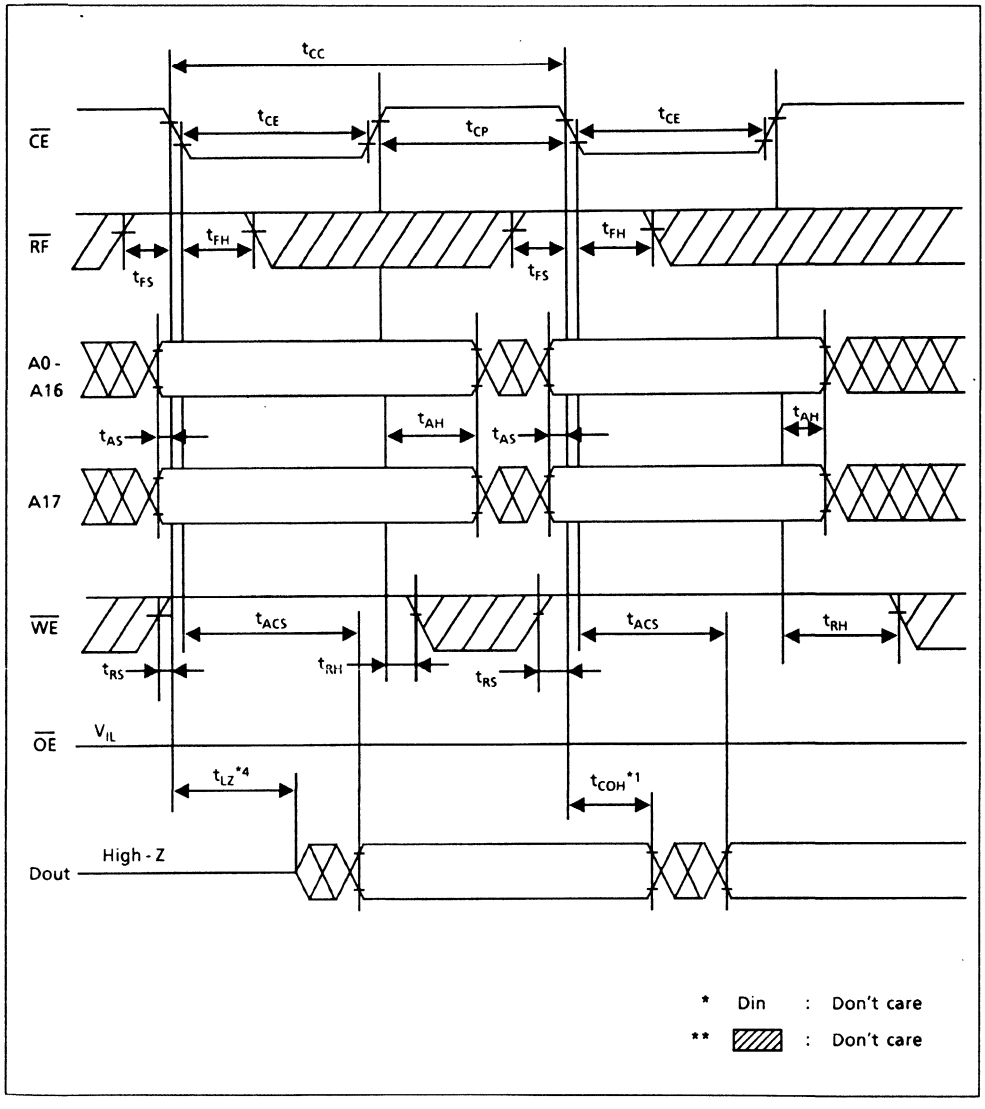
Read/Early Write Cycle



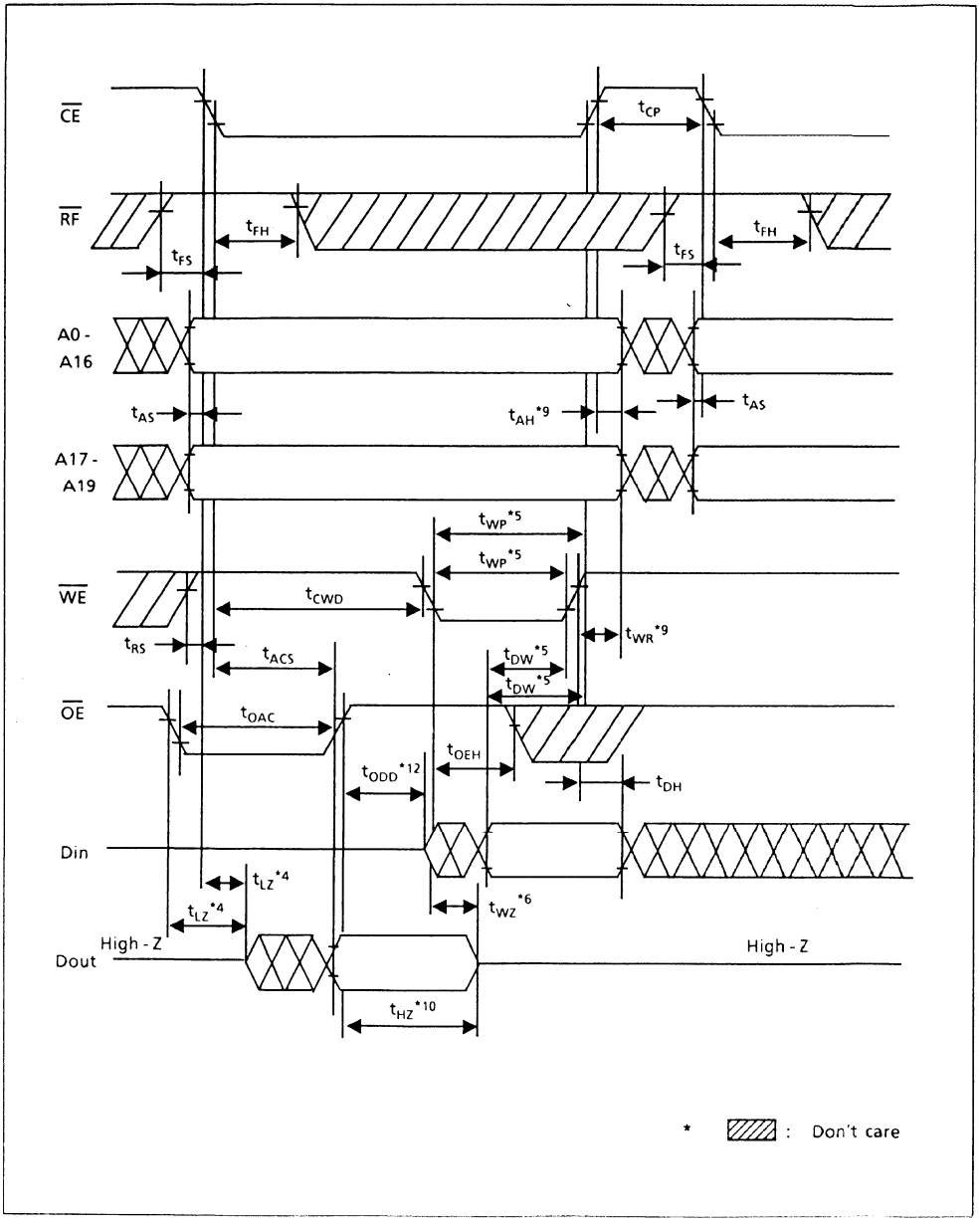
Read/Delayed Write Cycle



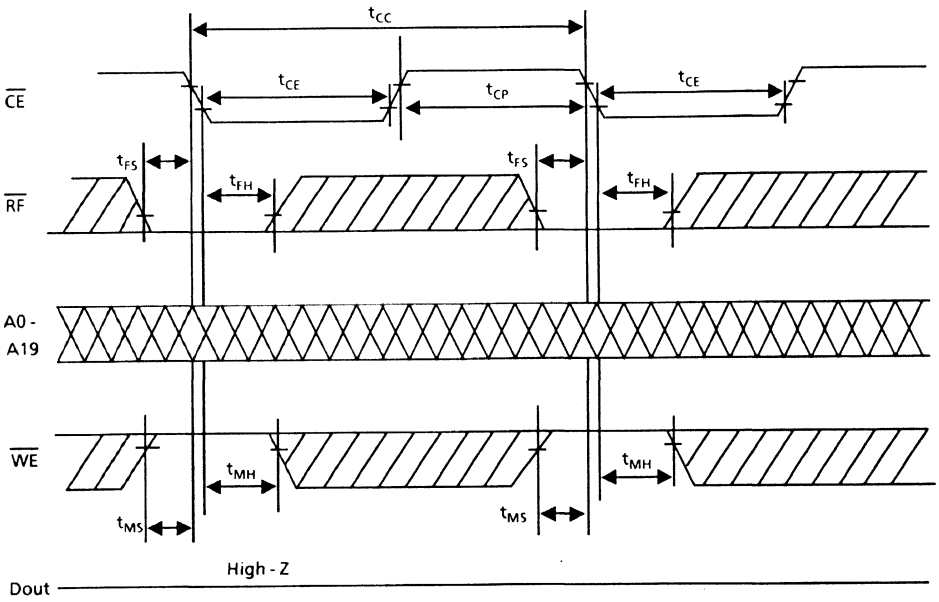
Read/Read Cycle ($\overline{OE}$ = V_{IL})



Read-Modify-Write Cycle



Automatic Refresh Cycle

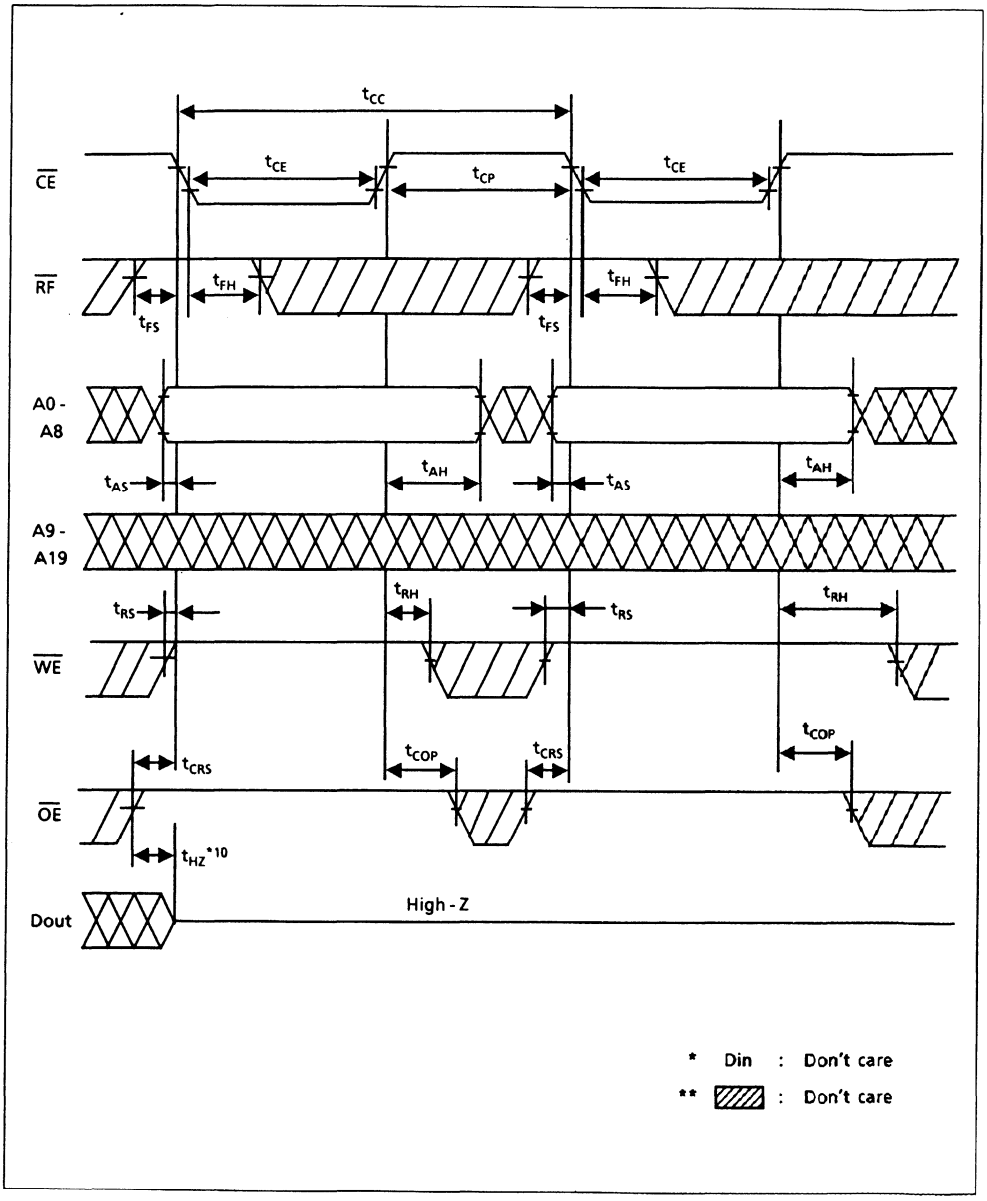


* A0 - A19 : Don't care

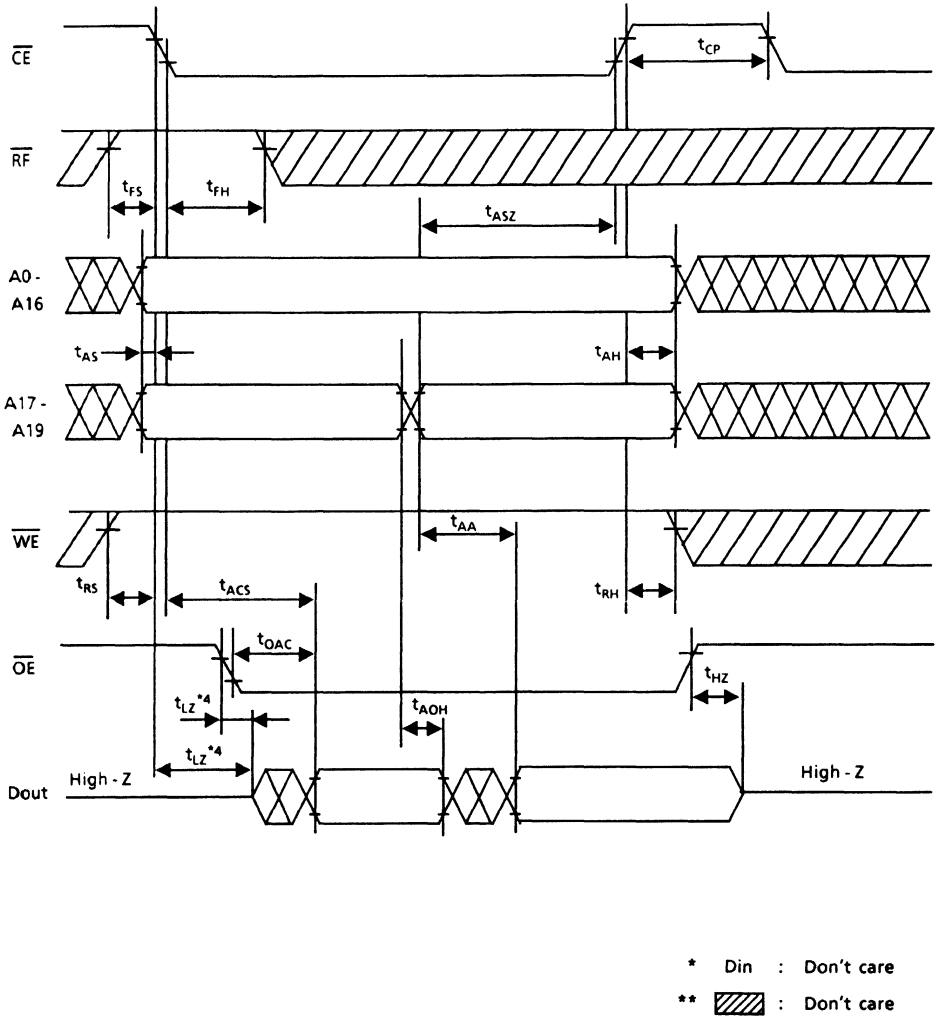
** $\overline{OE}$, Din : Don't care

*** ▨ : Don't care

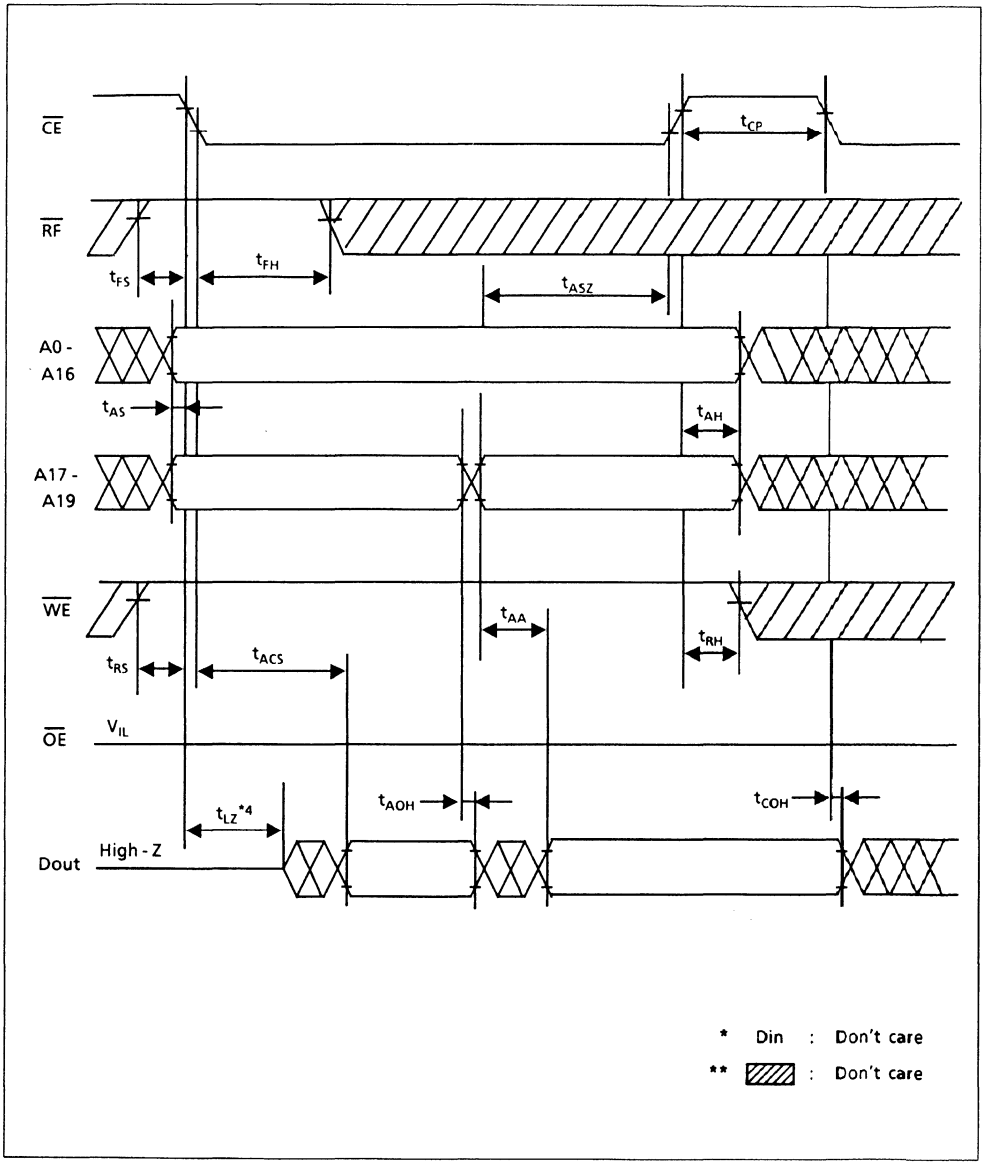
$\overline{CE}$ Refresh Cycle



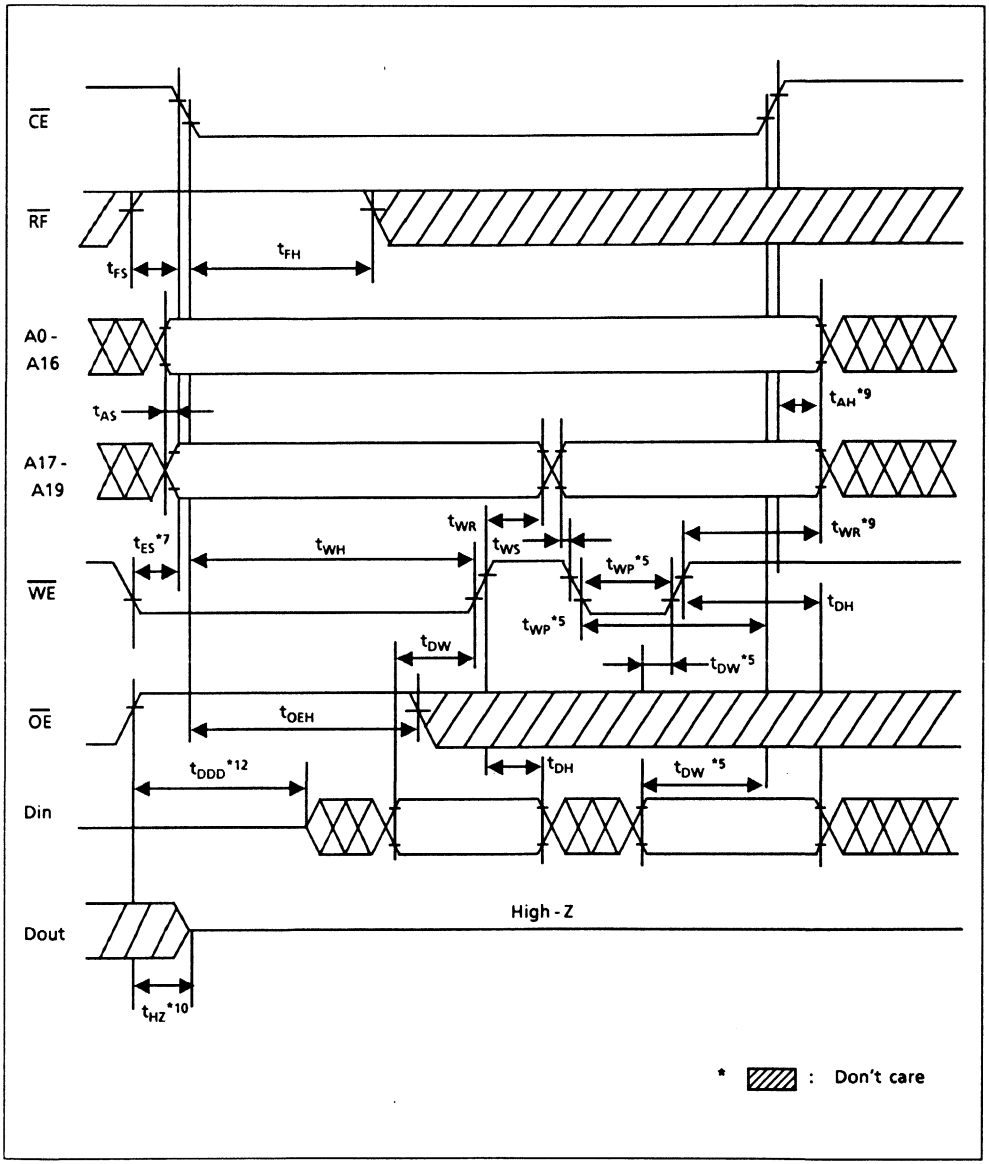
Static Column Mode Read Cycle



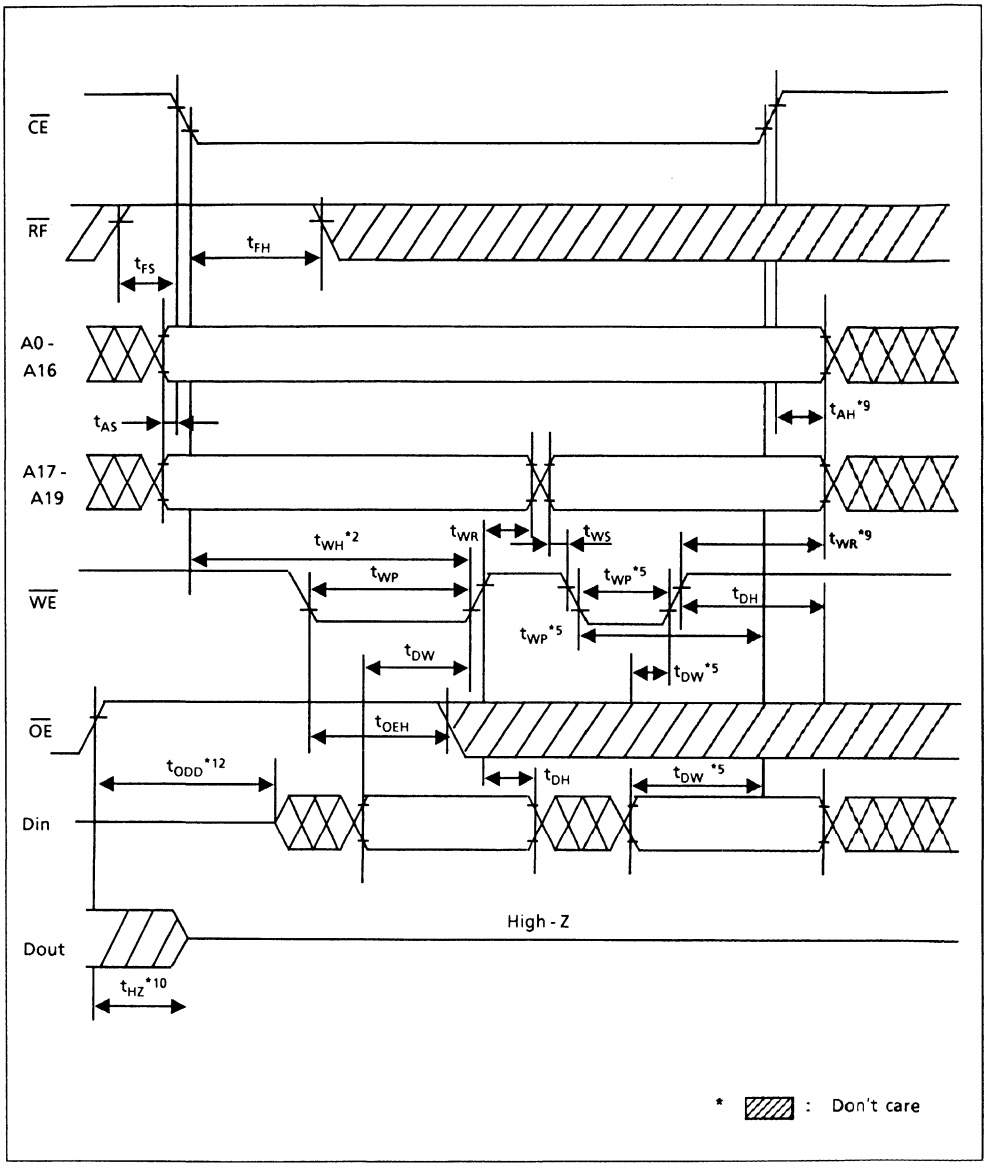
Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})



Static Column Mode Write Cycle*8 (1st cycle = Early Write Cycle)



Static Column Mode Write Cycle*8 (1st cycle = Delayed Write Cycle)



HM571000 Series

1,048,576-Word × 1-Bit High Speed Dynamic Random Access Memory

The Hitachi HM571000 is a super high speed dynamic RAM organized 1,048,576-word × 1-bit. HM571000 has realized higher density, higher performance and various functions by employing 1.3 µm Bi-CMOS technology and some new Bi-CMOS circuit design technologies. The HM571000 offers 8 bits static column mode as a high speed access mode.

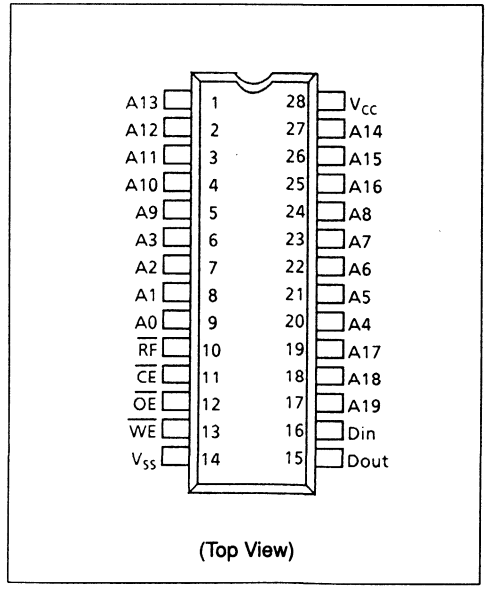
Ordering Information

Type No	Access time	Package
HM571000JP-35R	35 ns	300-mil 28-pin plastic SOJ (CP-28DN)
HM571000JP-40	40 ns	
HM571000JP-45	45 ns	

Features

- Single 5 V (± 10%) for HM571000JP-40/45
  5 V (± 5%) for HM571000JP-35R
- High speed
  - Access time: 35 ns/40 ns/45 ns (max)
- 512 refresh cycles: 4 ms
- 2 variations of refresh
  - $\overline{CE}$ refresh
  - Automatic refresh
- 8 bits static column mode

Pin Arrangement



(Top View)

Pin Description

Pin name	Function
A0 – A8	Address input for $\overline{CE}$ refresh
A9 – A16	Address input
A17 – A19	Address input for static column mode
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Read/write enable
Din	Data in
Dout	Data out
$\overline{RF}$	Refresh control
V_{CC}	Power (+5 V)
V_{SS}	Ground

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_T	0.8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	–35R / –40/45	V_{CC}	4.75 / 4.50	5.0	5.25 / 5.50	V	1
Input high voltage		V_{IH}	2.4	—	6.5	V	1, 3
Input low voltage		V_{IL}	–1.0	—	0.8	V	1, 2

Notes: 1. All voltage referenced to V_{SS}.
2. The device will withstand undershoots to the –2 V level with a maximum pulse width of 20 ns at the –1.5 V level. (See figure 1.)
3. The V_{IH} level of $\overline{OE}$ shall be lower than V_{CC} +0.5 V.

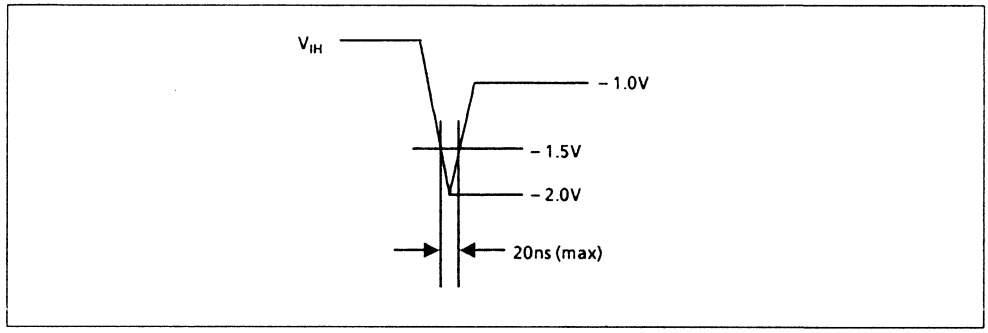


Figure 1 Undershoot of input voltage

DC Characteristics

(Ta = 0 to +70°C, V_{SS} = 0 V, V_{CC} = 5 V ± 10% for HM571000JP-40/45,
V_{CC} = 5 V ± 5% for HM571000JP-35R)

		HM571000-35R		HM571000-40		HM571000-45				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Normal operating current	I_{CCA}			See figure 2				mA		1
Refresh current	I_{CCR}			See figure 2				mA		1
Standby current	I_{CCS}	—	5	—	5	—	5	mA		
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V < Vin < 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V < Vout < 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –4 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 8 mA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

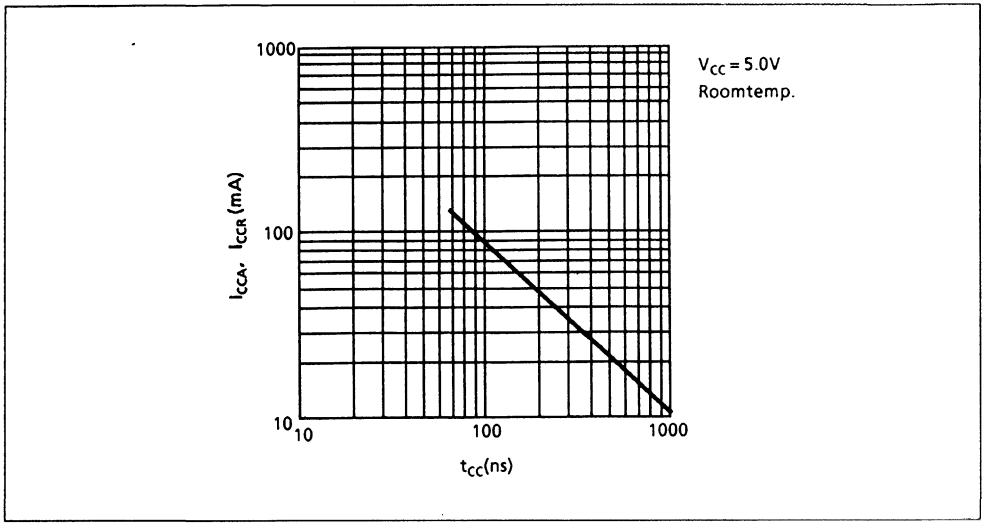


Figure 2 I_{CCA}, I_{CCR} **vs. Tcycle**

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10% for HM571000JP-40/45, V_{CC} = 5 V ± 5% for HM571000JP-35R)

Parameter		Symbol	Typ	Max	Unit	Notes
Input capacitance	Address, Data-in	Cin1	—	5	pF	1
	Clock ($\overline{CE}$, $\overline{OE}$)	Cin2	—	5	pF	1
	Clock ($\overline{WE}$, $\overline{RF}$)	Cin3	—	7	pF	1
Output capacitance	(Data-out)	C_O	—	10	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{OE}$, $\overline{CE}$ = V_{IH} to disable Dout.

AC Characteristics *1 (Ta = 0 to +70°C, V_{SS} = 0 V, V_{CC} = 5 V ± 10% for HM571000JP-40/45, V_{CC} = 5 V ±5% for HM571000JP-35R)

Test Conditions

Input pulse levels: V_{IH} = 3.0 V, V_{IL} = 0 V
Transition time: t_T = 3 ns
Input timing reference levels: high = 2.4 V, low = 0.8 V (See figure 3.)
Output timing reference levels: high = 2.4 V, low = 0.4 V
Output load: See figure 4.

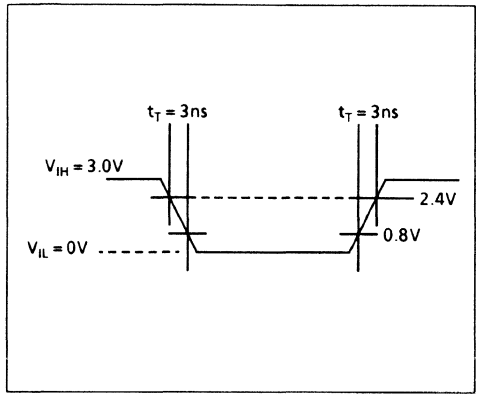


Figure 3 Input pulse

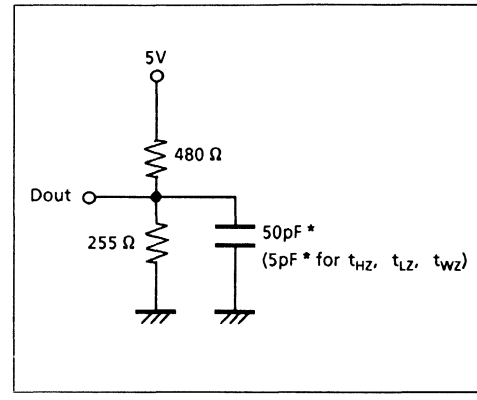


Figure 4 Output load

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

		HM571000-35R		HM571000-40		HM571000-45			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Read/write cycle time	t_{CC}	75	—	85	—	90	—	ns	
CE pulse width	t_{CE}	35	5000	40	5000	45	5000	ns	
CE precharge time	t_{CP}	34	—	39	—	39	—	ns	
Address setup time	t_{AS}	0	—	0	—	0	—	ns	
Address hold time	t_{AH}	5	—	5	—	5	—	ns	
Transition time (rise and fall)	t_T	1	10	1	10	1	10	ns	
Refresh period	t_{REF}	—	4	—	4	—	4	ms	

Read Cycle

		HM571000-35R		HM571000-40		HM571000-45			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{CE}$	t_{ACS}	—	35	—	40	—	45	ns	
Address access time	t_{AA}	—	25	—	30	—	30	ns	
Access time from $\overline{OE}$	t_{OAC}	—	20	—	25	—	25	ns	
Setup time on read	t_{RS}	0	—	0	—	0	—	ns	
Hold time on read	t_{RH}	5	—	5	—	5	—	ns	
$\overline{OE}$ setup time	t_{OES}	5	—	5	—	5	—	ns	
$\overline{OE}$ enable to output in low-Z	t_{LZ}	0	—	0	—	0	—	ns	
$\overline{OE}$ disable to output in high-Z	t_{HZ}	—	15	—	20	—	20	ns	
Output hold time from address	t_{AOH}	3	—	3	—	3	—	ns	
Output hold time from $\overline{CE}$	t_{COH}	0	—	0	—	0	—	ns	
$\overline{CE}$ to $\overline{OE}$ precharge time	t_{COP}	10	—	10	—	10	—	ns	

Write Cycle

		HM571000-35R		HM571000-40		HM571000-45			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Data setup time	t_{DW}	20	—	25	—	30	—	ns	
Data hold time	t_{DH}	5	—	5	—	5	—	ns	
Setup time on early write	t_{ES}	5	—	5	—	5	—	ns	
$\overline{WE}$ pulse width	t_{WP}	25	—	30	—	35	—	ns	
Write hold time from $\overline{CE}$	t_{WH}	35	—	40	—	45	—	ns	
$\overline{WE}$ enable to output in high-Z	t_{WZ}	—	15	—	20	—	20	ns	

Read-Modify-Write Cycle

		HM571000-35R		HM571000-40		HM571000-45			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{WE}$ delay time from $\overline{CE}$	t_{CWD}	35	—	40	—	45	—	ns	

Refresh Cycle

		HM571000-35R		HM571000-40		HM571000-45			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{RF}$ setup time	t_{FS}	5	—	5	—	5	—	ns	
$\overline{RF}$ hold time	t_{FH}	15	—	15	—	15	—	ns	
Mode selection setup time	t_{MS}	0	—	0	—	0	—	ns	
Mode selection hold time	t_{MH}	15	—	20	—	20	—	ns	
Setup time on $\overline{CE}$ refresh	t_{CRS}	15	—	20	—	20	—	ns	

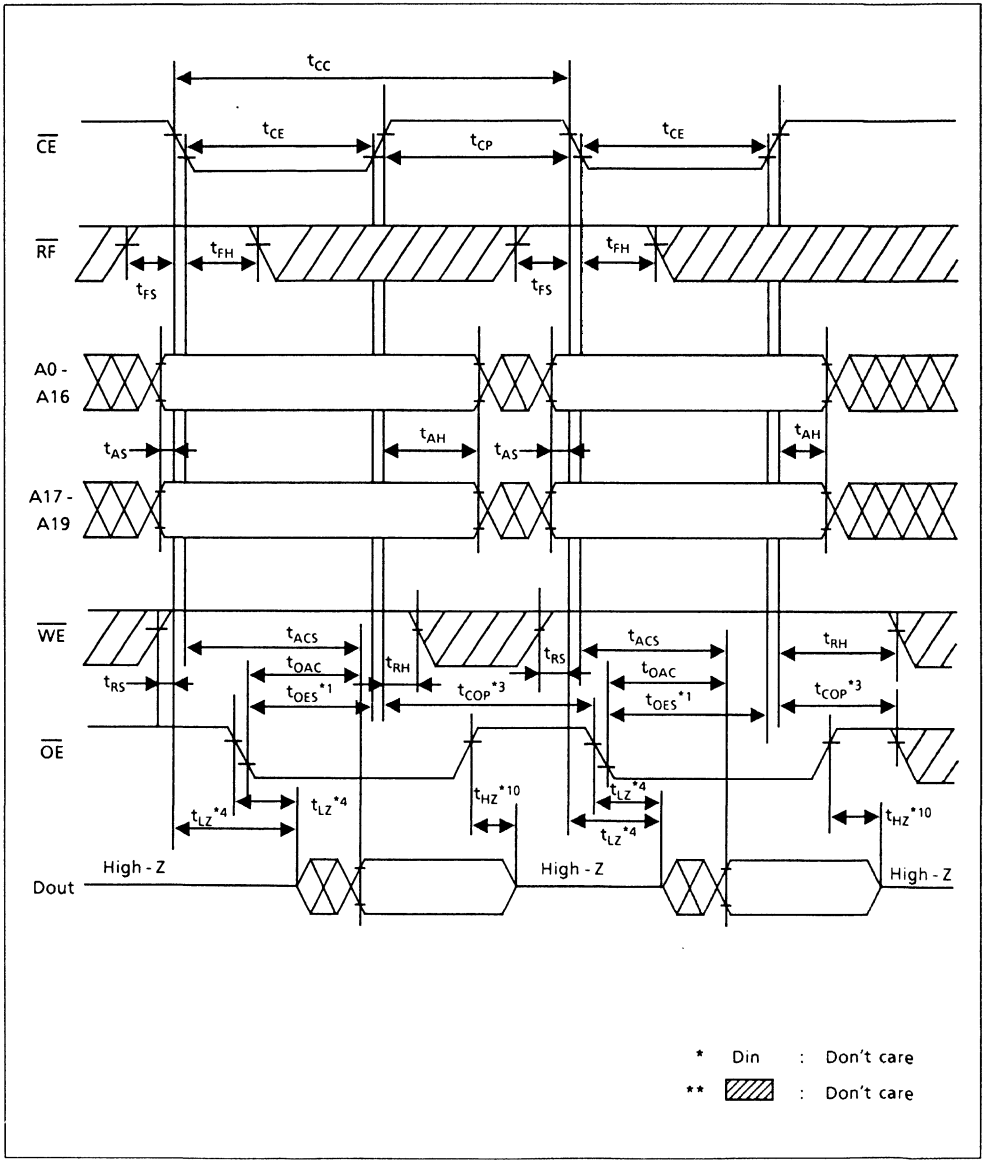
Static Column Mode Cycle

		HM571000-35R		HM571000-40		HM571000-45			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Static column address setup time	t_{ASZ}	20	—	25	—	25	—	ns	
Address setup time to $\overline{WE}$	t_{WS}	0	—	0	—	0	—	ns	
Address hold time from $\overline{WE}$	t_{WR}	0	—	0	—	0	—	ns	

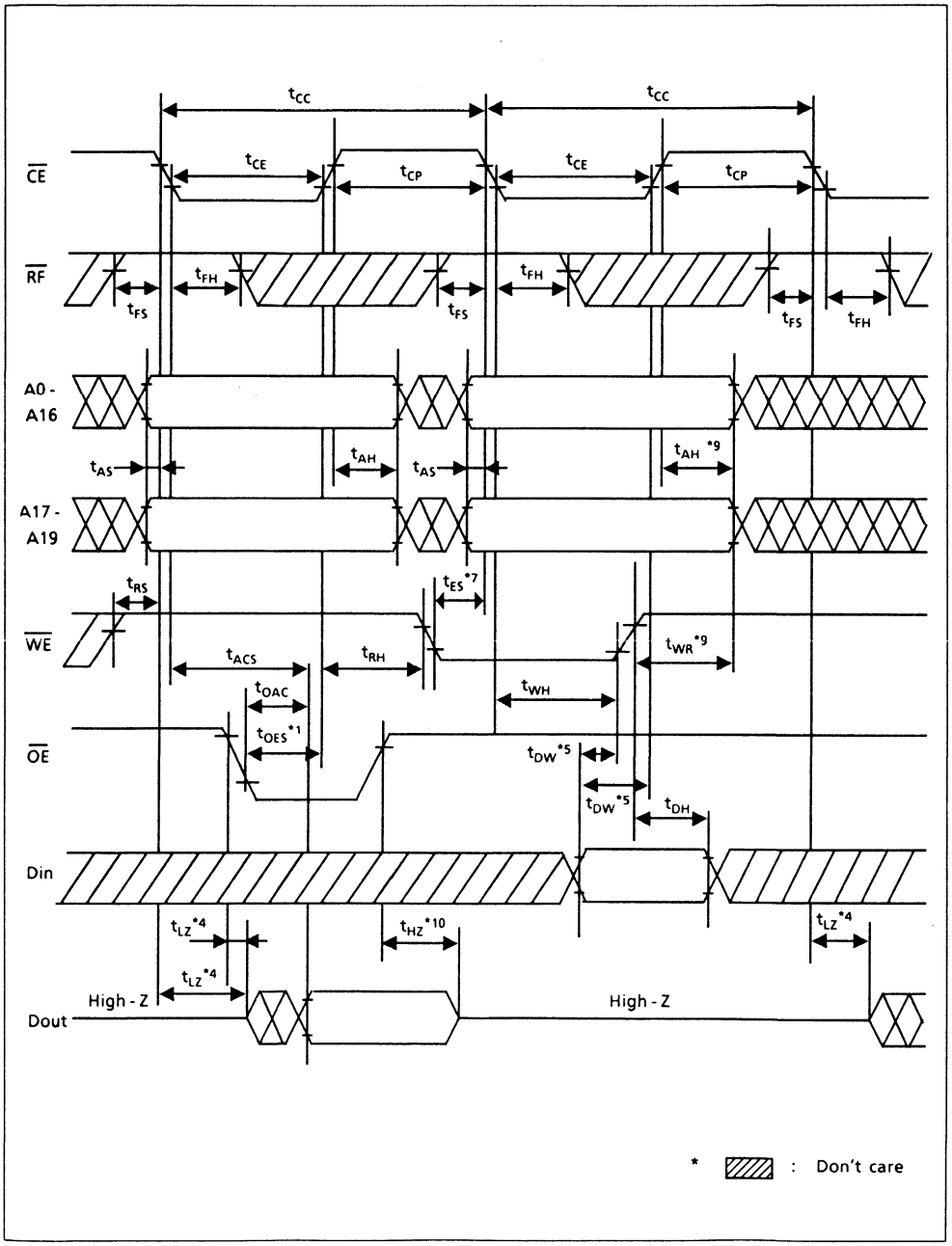
Notes:
1. If $t_{OES} > t_{OES}$ (min) and $\overline{OE}$ is held at low level, Dout will be valid until the next negative transition of $\overline{CE}$.
2. Both t_{WH} and t_{WP} must be satisfied for a delayed write cycle.
3. If $t_{COP} < t_{COP}$ (min), Dout cannot be guaranteed to be in high impedance.
4. If the negative transition of $\overline{OE}$ occurs before that of $\overline{CE}$, t_{LZ} is controlled by $\overline{CE}$.
5. t_{WP} and t_{DW} are specified by the positive transition of $\overline{CE}$ or $\overline{WE}$ whichever occurs earlier.
6. When $\overline{WE}$ goes low, Dout becomes high impedance and is held in this condition to the next cycle. If the negative transition of $\overline{WE}$ occurs before that of $\overline{CE}$, Dout is controlled by $\overline{CE}$. t_{WZ} is defined as the time at which the output achieves the open circuit condition.
7. If $t_{ES} > t_{ES}$ (min), the cycle is early write and Dout is in high impedance.
8. In static column mode cycles, read operation cannot be performed after write operation.
9. Both t_{AH} and t_{WR} must be satisfied for a write cycle.
10. t_{HZ} is defined as the time at which the output achieves the open circuit condition.
11. An initial pause of 100 μs is required after power-up, then execute at least eight $\overline{CE}$ refresh cycles.
12. In static column mode cycle, there must not be any invalid address inputs for static column mode (A17 to A19) which are less than t_{AA}.

Timing Waveforms

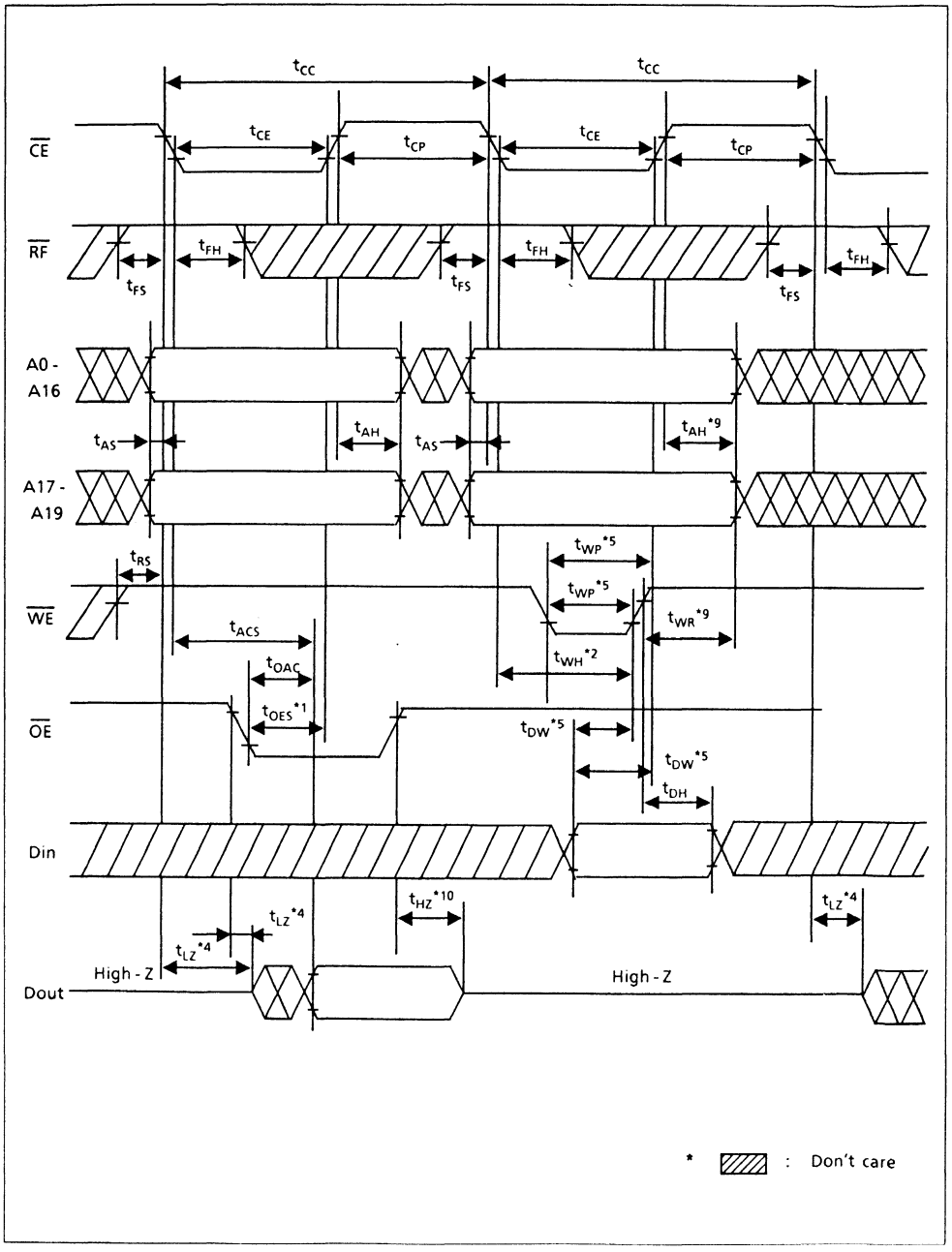
Read/Read Cycle



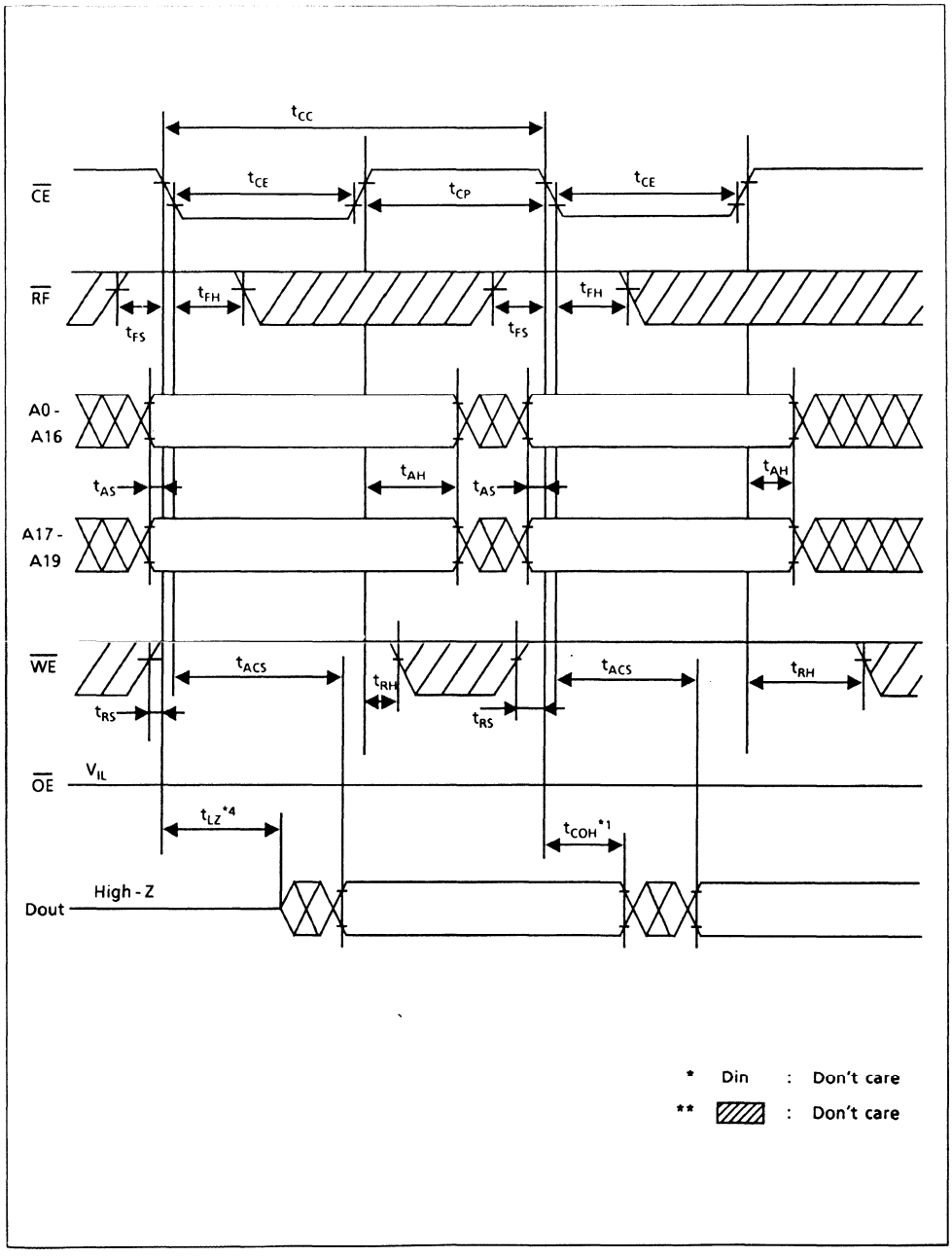
Read/Early Write Cycle



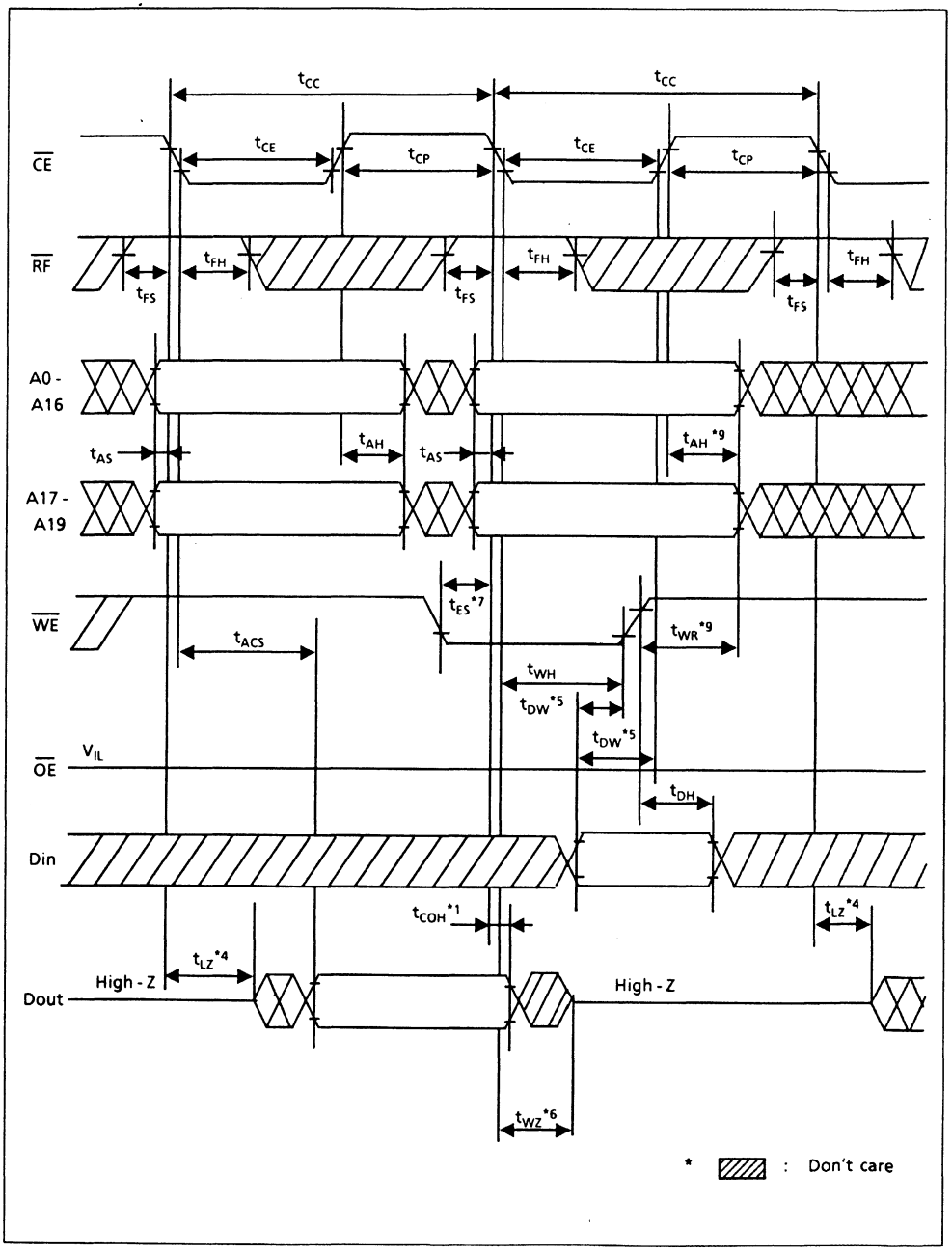
Read/Delayed Write Cycle



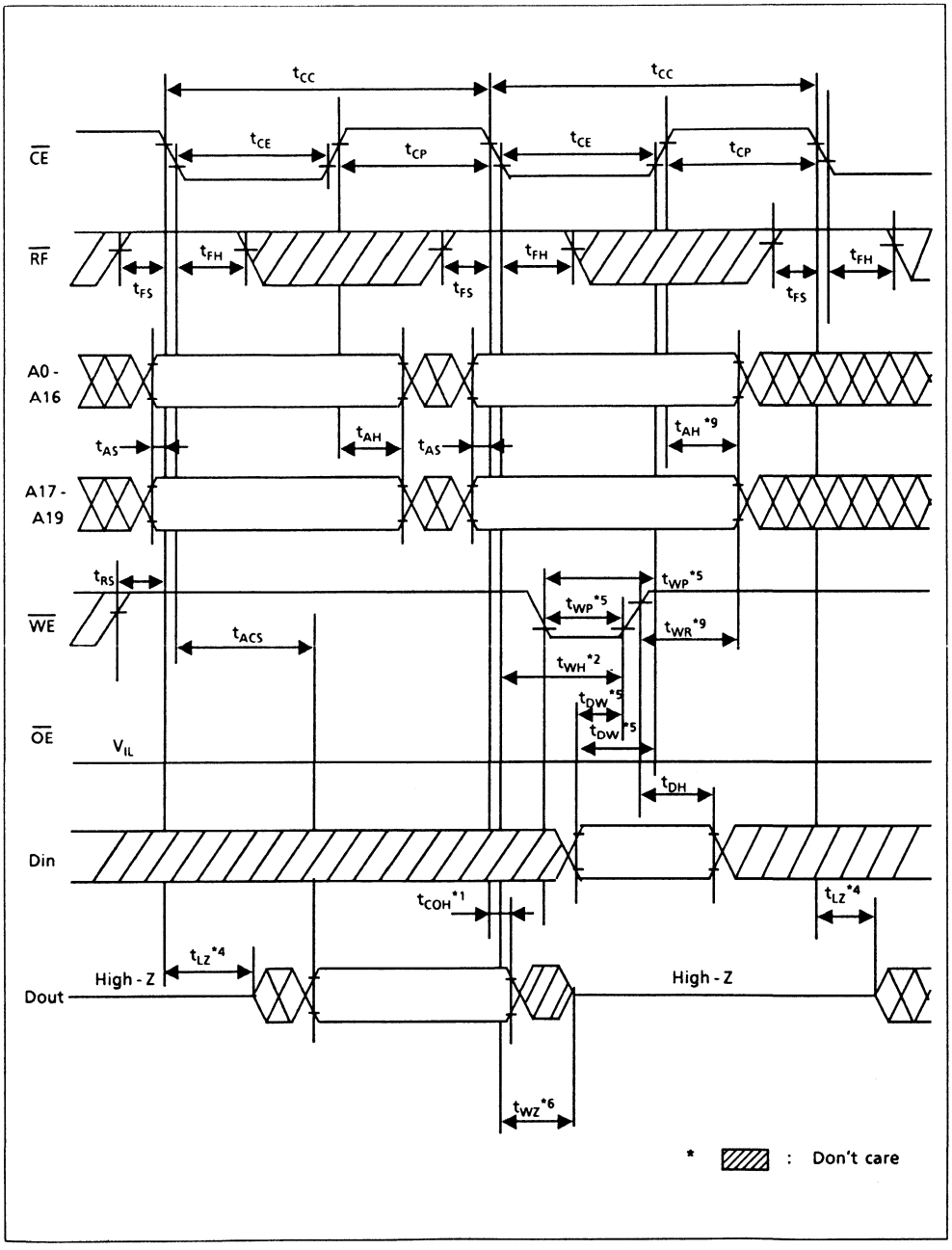
Read/Read Cycle ($\overline{OE}$ = V_{IL})



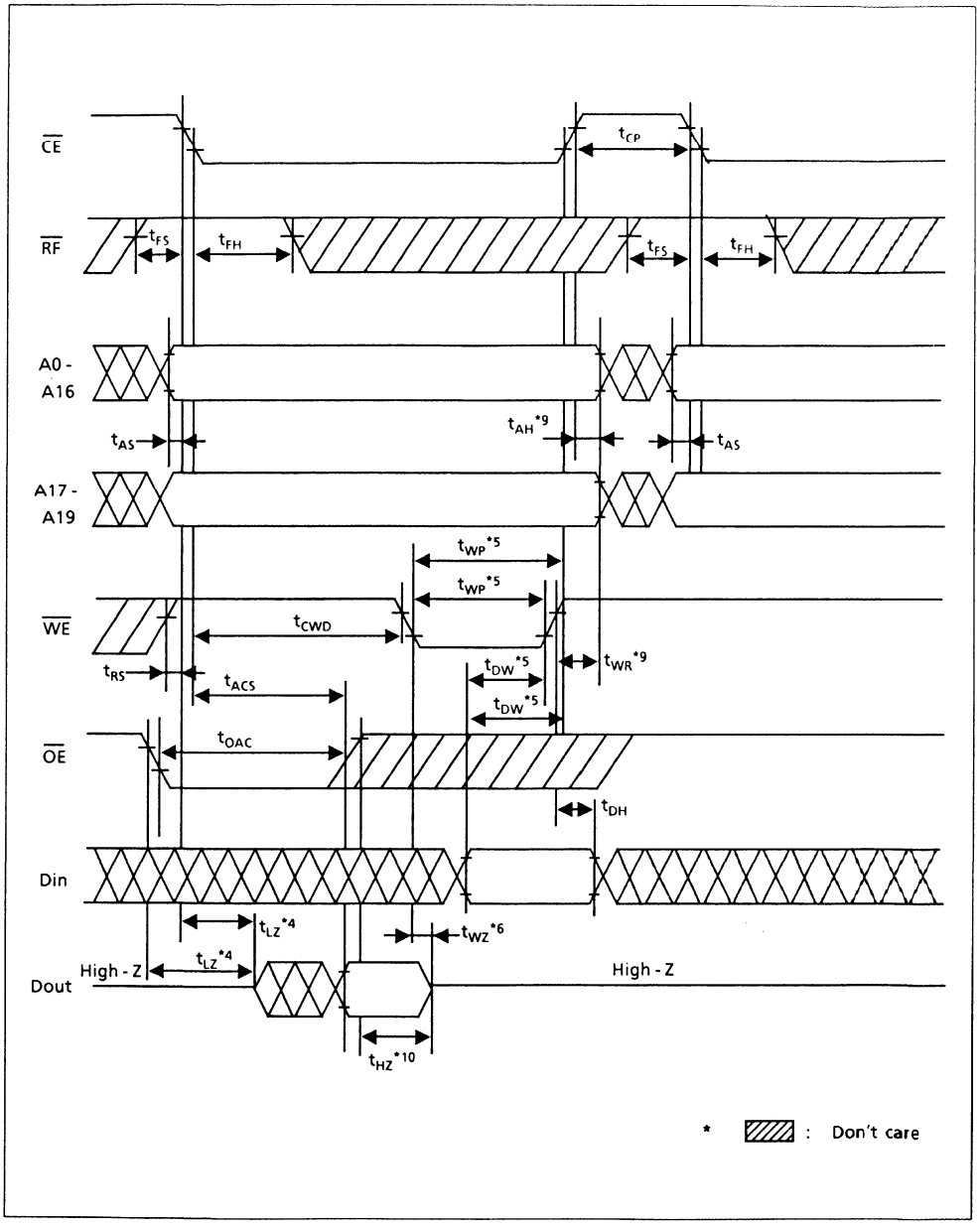
Read/Early Write Cycle ($\overline{OE}$ = V_{IL})



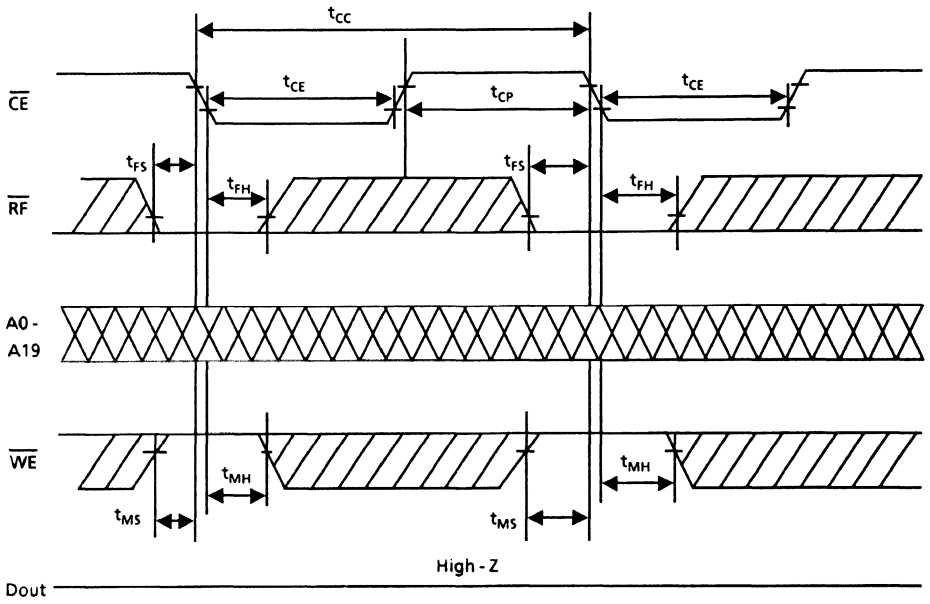
Read/Delayed Write Cycle ($\overline{OE}$ = V_{IL})



Read-Modify-Write Cycle



Automatic Refresh Cycle

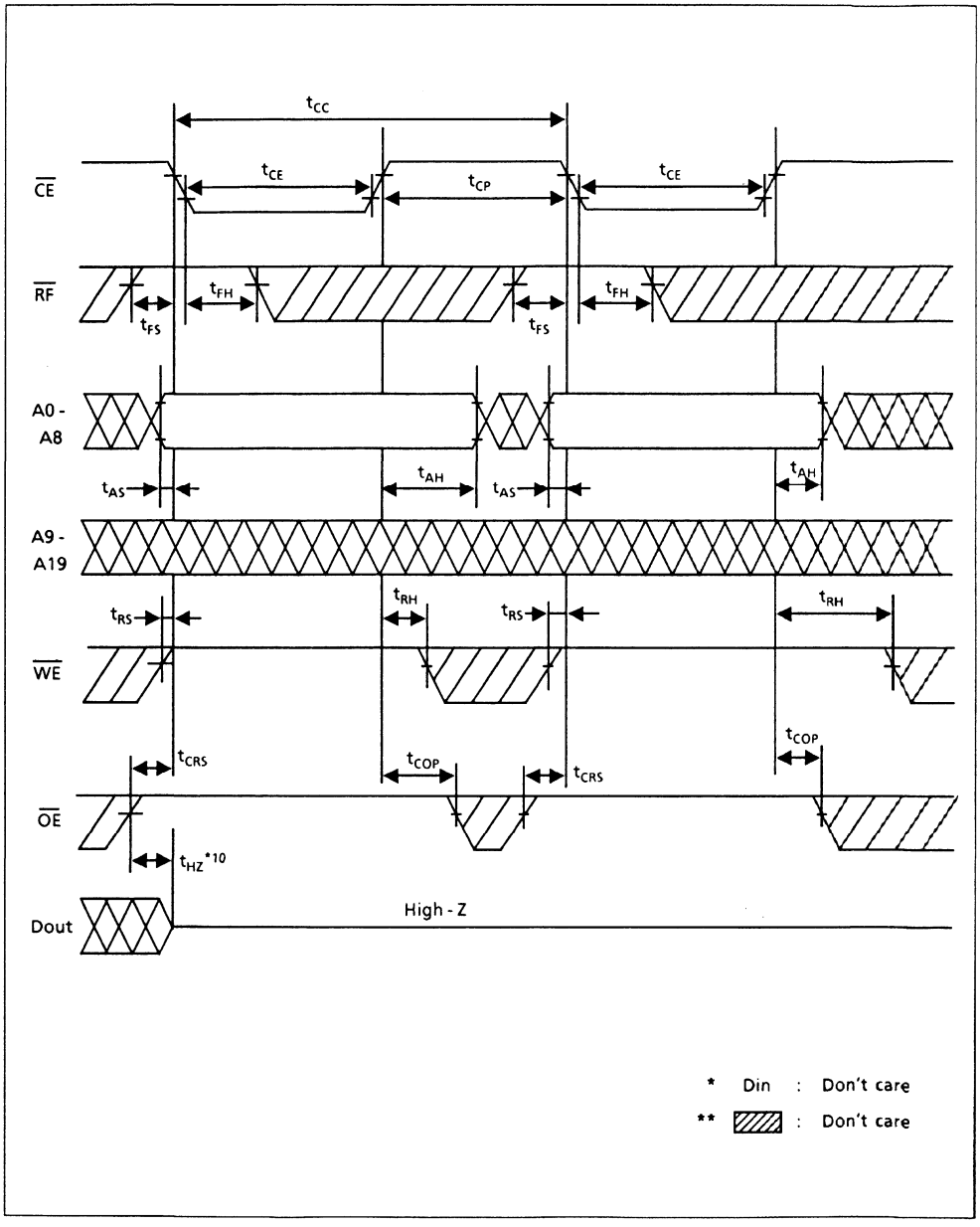


* A0 - A19 : Don't care

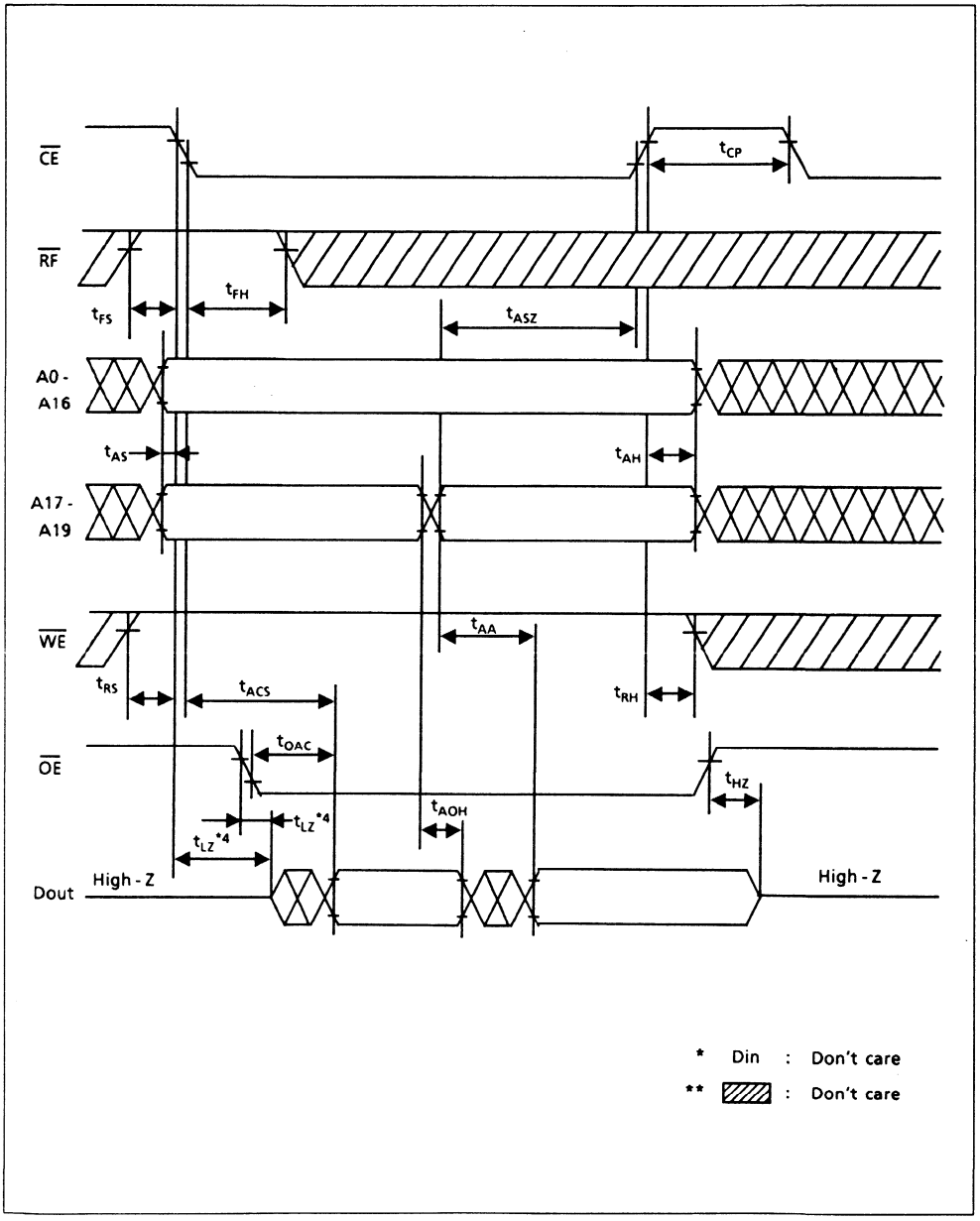
** $\overline{OE}$, Din : Don't care

*** ▨ : Don't care

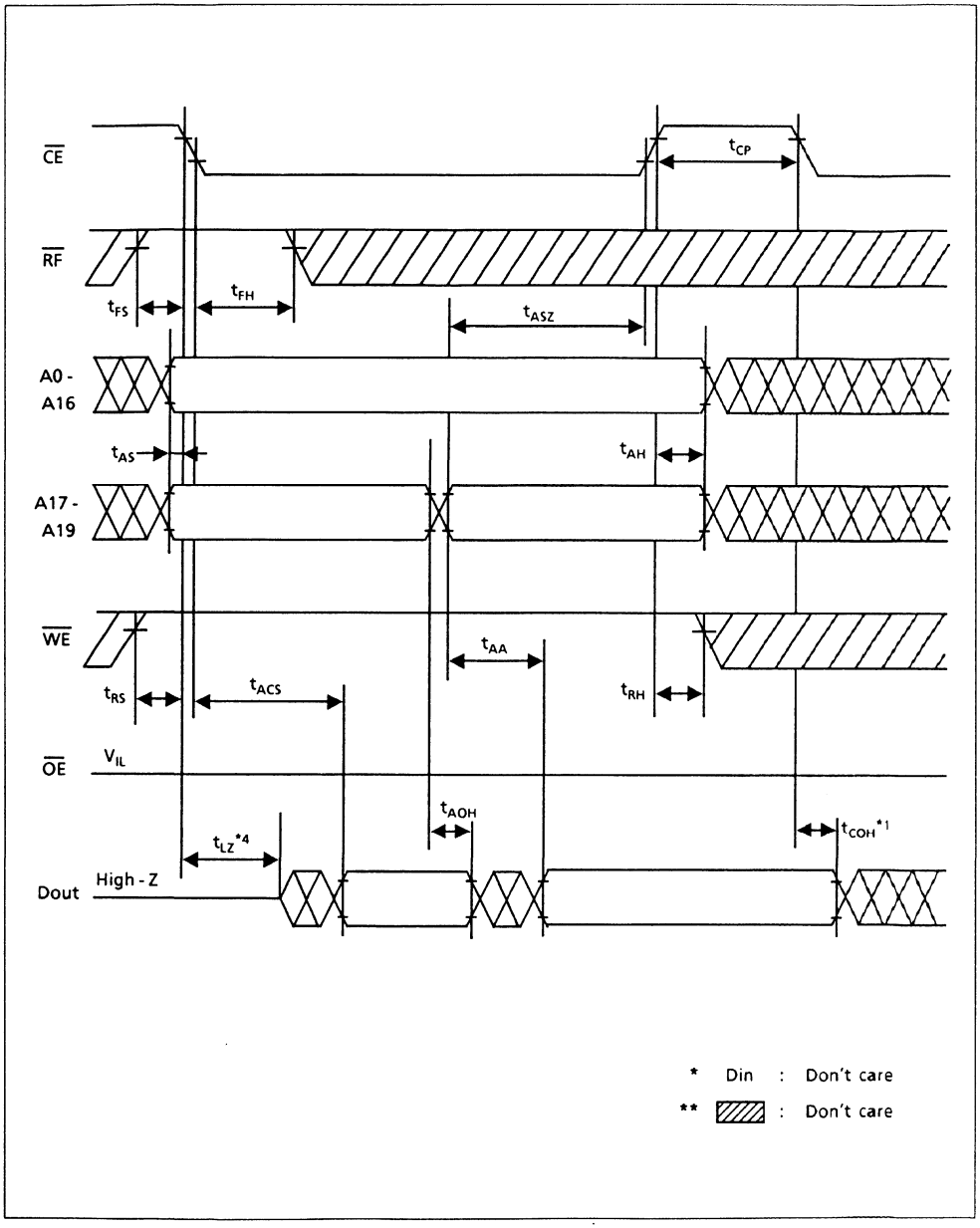
$\overline{CE}$ Refresh Cycle



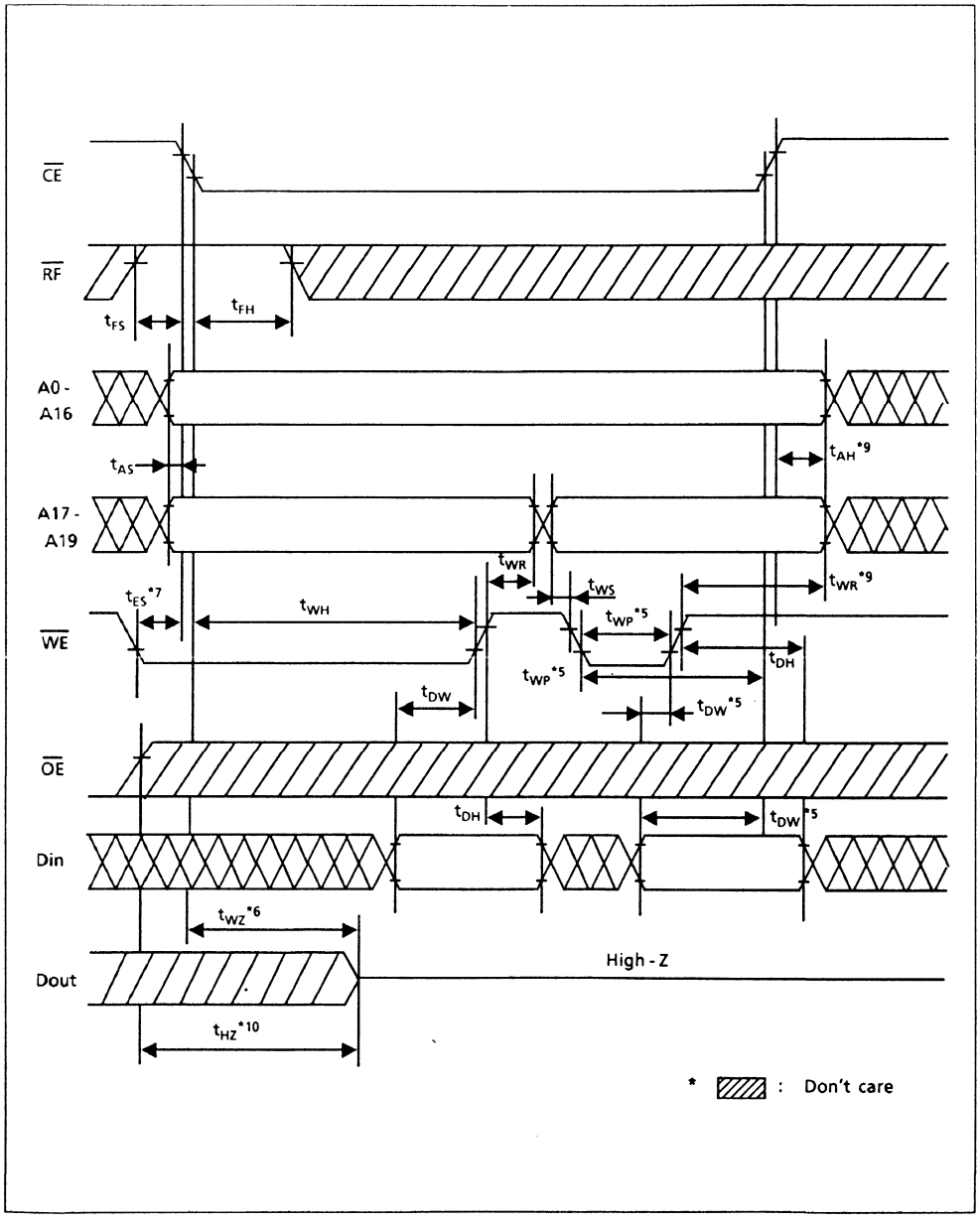
Static Column Mode Read Cycle



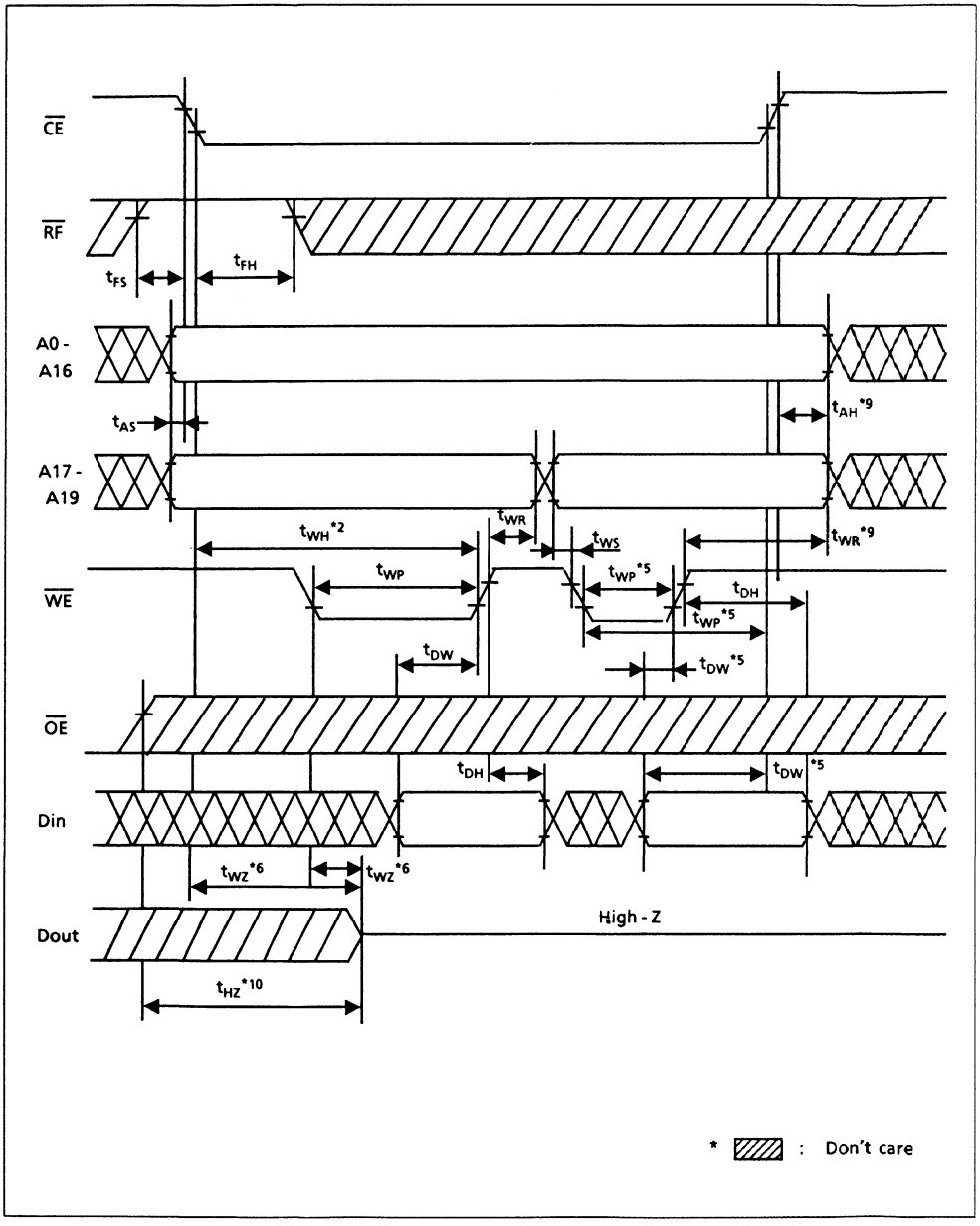
Static Column Mode Read Cycle ($\overline{OE}$ = V_{IL})



Static Column Mode Write Cycle*8 (1st cycle = Early Write Cycle)



Static Column Mode Write Cycle*8 (1st cycle = Delayed Write Cycle)



MOS DYNAMIC RAM MODULE

HB561409 Series

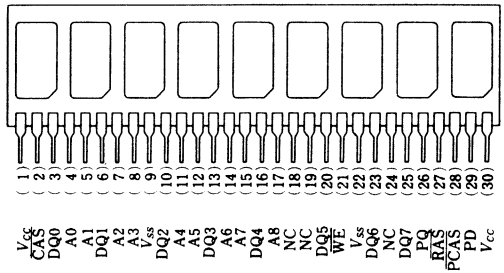
262,144-word x 9-bit Dynamic Random Access Memory Module

The HB561409 is a 256k x 9 dynamic RAM module, mounted 9 pieces of 256k-bit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB561409 is 30-pin single in-line package having two types; Lead type (HB561409A) and Socket type (HB561409B). Therefore, the HB561409 makes high density mounting possible without surface mount technology.
The HB561409 provides common data input and output, and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors to reduce noise.

Features

- 262,144 words x 9 bits organization
- Industry standard 30-pin Single In-line Package Memory Module
- Single 5V (±10%)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM51256CP)
- HB561409A/B operates as nine HM51256CPs as shown in the functional block diagram
- Low Power: Operating . . . . . 1,800mW (typ) (t_{RC} = 180ns)
  Standby . . . . . 60mW (typ)
- High speed: Access time = 85ns/100ns (max)
- High speed page mode capability (t_{PC} = 65ns)
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
  $\overline{RAS}$-only refresh
  $\overline{CAS}$-before-$\overline{RAS}$ refresh
  Hidden refresh
- Operating Ambient Air Temperature . . . . . 0°C to +70°C.

Pin Arrangement



(Side View)

Notes: 1. HB561409B's pin arrangement is same as HB561409A's.
2. Common $\overline{CAS}$ control for eight common Data-In and Data-Out lines.
3. Separate $\overline{PCAS}$ control for one separate pair of Data-In and Data-Outlines.
4. The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

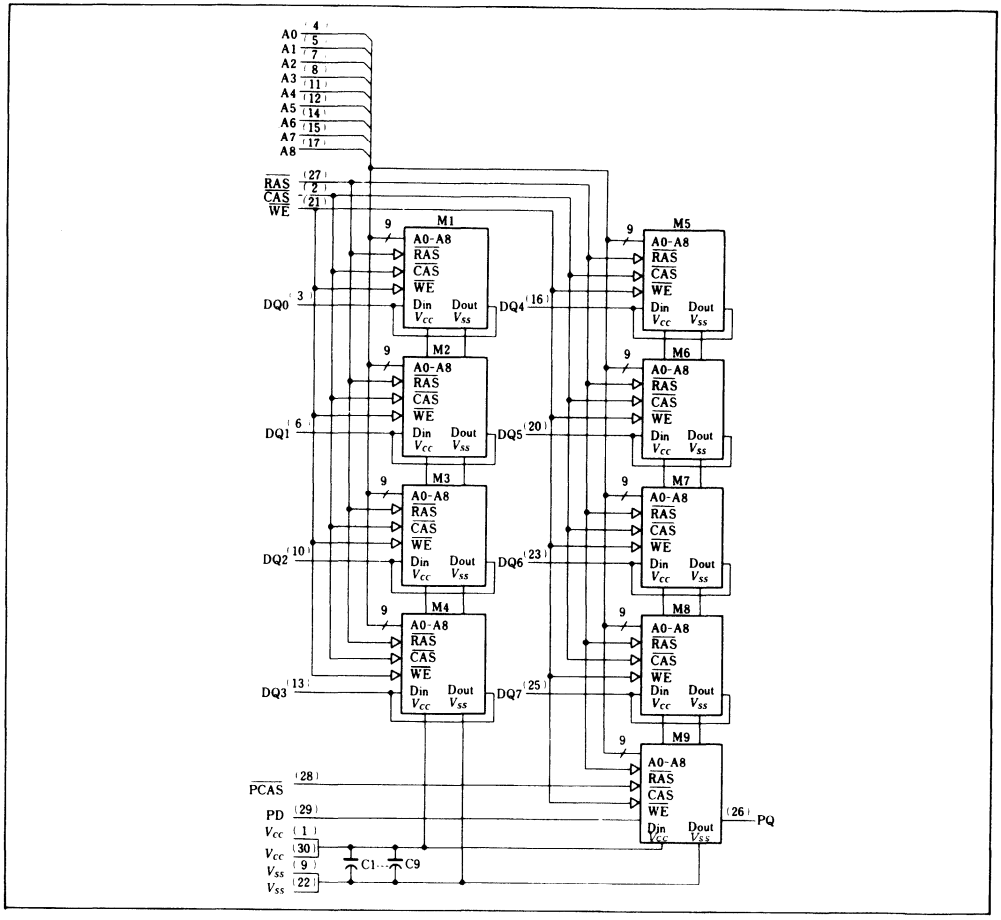
Ordering Information

Type No.	Access Time	Package
HB561409A-85	85ns	30-pin SIP
HB561409A-10	100ns	Lead Type
HB561409B-85	85ns	30-pin SIP
HB561409B-10	100ns	Socket Type

Pin Description

A0–A8	Address Input
A0-A7	Refresh Address Input
$\overline{CAS}$, $\overline{PCAS}$	Column address strobe
DQ0-DQ7	Data In/Data Out
PD	Data In for Parity
NC	No Connection
PQ	Data Out for Parity
$\overline{RAS}$	Row Address Strobe
Vcc	+5V Supply
Vss	Ground
$\overline{WE}$	Write Enable

Functional Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} . . . . . −1V to +7V
Operating temperature, T_a (Ambient) . . . . . 0°C to +70°C
Storage temperature (Ambient) . . . . . −55°C to +125°C
Power dissipation 9W
Short circuit output current 50mA

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	—	5.5	V	1
Input Low voltage	V_{IL}	−1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}.

DC Electrical Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	HB561409-85		HB561409-10		Unit	Notes
		Min	Max	Min	Max		
Operating current t_{RC}=min	I_{CC1}	—	630	—	540	mA	*1
Standby current	I_{CC2}	—	18	—	18	mA	
Refresh current t_{RC}=min	I_{CC3}	—	630	—	540	mA	$\overline{RAS}$ only refresh
Standby current (Dout Enable)	I_{CC4}	—	54	—	54	mA	*1
Refresh current t_{RC}=min	I_{CC5}	—	540	—	495	mA	$\overline{CAS}$ before $\overline{RAS}$ refresh
Operating current t_{PC}=min	I_{CC6}	—	630	—	540	mA	*1, High speed page mode
Input leakage 0<Vin<7V	I_{LI}	-10	10	-10	10	µA	
Output leakage 0<Vout<7V	I_{LO}	-10	10	-10	10	µA	Dout is disabled
Output levels High Iout=-5mA	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	
Low Iout=4.2mA	V_{OL}	0	0.4	0	0.4	V	

Notes: *1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.

Capacitance (V_{CC} = 5V ± 10%, Ta = 25°C)

Parameter	Symbol	Type	Max	Unit	Notes
Address	C_{I1}	—	60	pF	*1
Clocks	C_{I2}	—	75	pF	*1,2
DQ	$C_{I/O}$	—	17	pF	*1,2
PQ	C_O	—	12	pF	*1,2
PD	C_{I3}	—	10	pF	*1

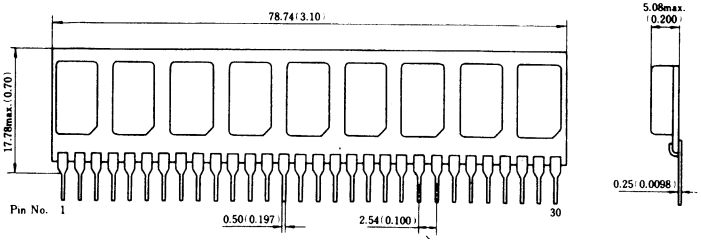
Notes: *1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
*2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

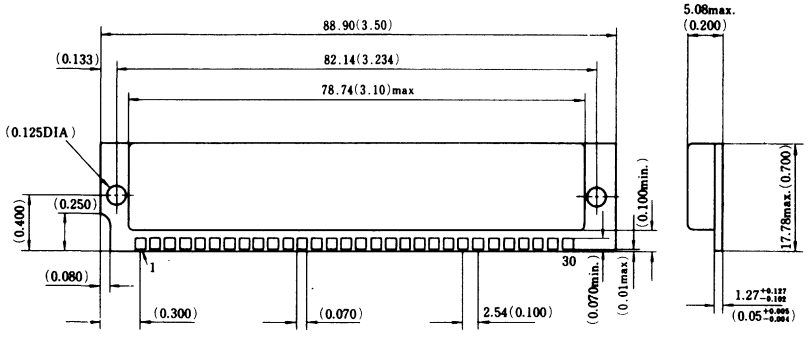
Refer to the HM51256 series data sheet. The HB561409 writes data only in early write cycle (twcs ≥ twcs (min)). Delayed write cycle is not available because of I/O common.

Package Outline, Unit; mm (inch)

HB561409A



HB561409B



HB56D25609 Series

262,144-Word × 9-Bit High Density Dynamic RAM Module

The HB56D25609 is a 256 k × 9 dynamic RAM module, mounted two 1-Mbit DRAM (HM514256JP) sealed in SOJ package and 256-kbit DRAM (HM51256) sealed in PLCC package. An outline of the HB56D25609 is 30-pin single in-line package having lead types (HB56D25609A), socket type (HB56D25609B). Therefore, the HB56D25609 makes high density mounting possible without surface mount technology. The HB56D25609 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ and PLCC.

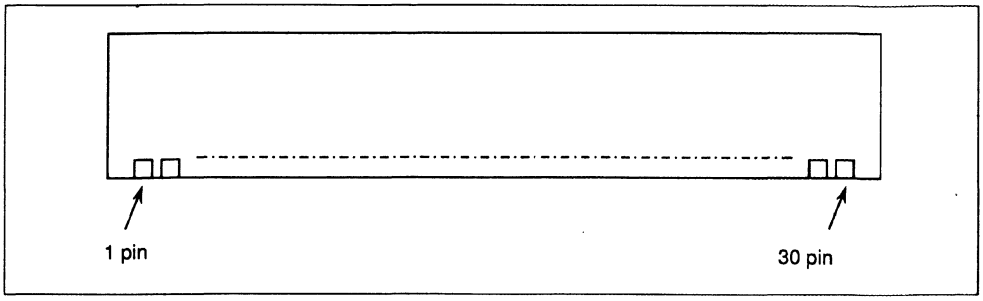
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (±10%) supply
- High speed
  - Access time: 85 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 1.11 W/0.94 W/0.79 W (max)
  - Standby mode: 33 mW (max)
- Fast page mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HB56D25609A-85A	85 ns	30-pin SIP lead type
HB56D25609A-10A	100 ns	
HB56D25609A-12A	120 ns	
HB56D25609B-85A	85 ns	30-pin SIP socket type
HB56D25609B-10A	100 ns	
HB56D25609B-12A	120 ns	

Pin Arrangement

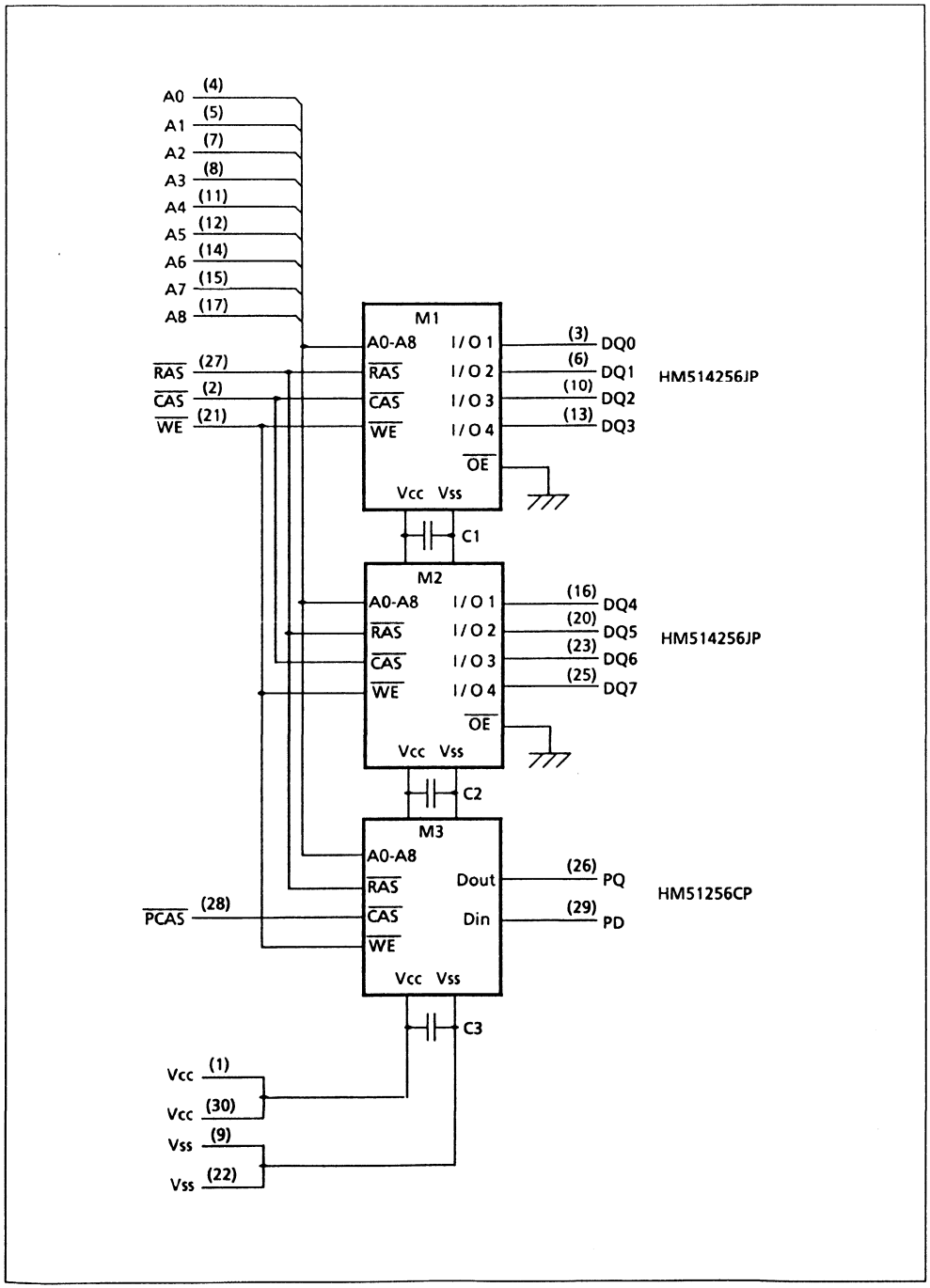


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	NC
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCAS}$
14	A6	29	PD
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A8	Address input
A0 – A8	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$, $\overline{PCAS}$	Column address strobe
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
PD	Data-in for parity
PQ	Data-out for parity
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	3	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56D25609A/B								
		-85A		-10A		-12A				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	202	—	170	—	144	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	6	—	6	—	6	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	3	—	3	—	3	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}−0.2 V Dout = High-Z	

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) (cont)

		HB56D25609A/B								
		-85A		-10A		-12A				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
$\overline{RAS}$-only refresh current	I_{CC3}	—	202	—	170	—	144	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	16	—	16	—	16	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	192	—	165	—	139	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	180	—	170	—	144	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	30	pF	1
Input capacitance (Clock)	C_{I2}	—	36	pF	1
Input/output capacitance (DQ0 – DQ7)	$C_{I/O}$	—	17	pF	1, 2
Input capacitance (PD)	C_{I3}	—	10	pF	1, 2
Output capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *12

Read, Write and Refresh Cycle (Common Parameter)

		HB56D25609A/B							
		-85A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
Column address hold time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	15

Read Cycle

		HB56D25609A/B							
		-85A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access time from Address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

		HB56D25609A/B							
		-85A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	20	—	25	—	30	—	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	20	—	20	—	25	—	ns	11
Data-in hold time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

Refresh Cycle

		HB56D25609A/B							
		-85A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	15	—	15	—	15	—	ns	

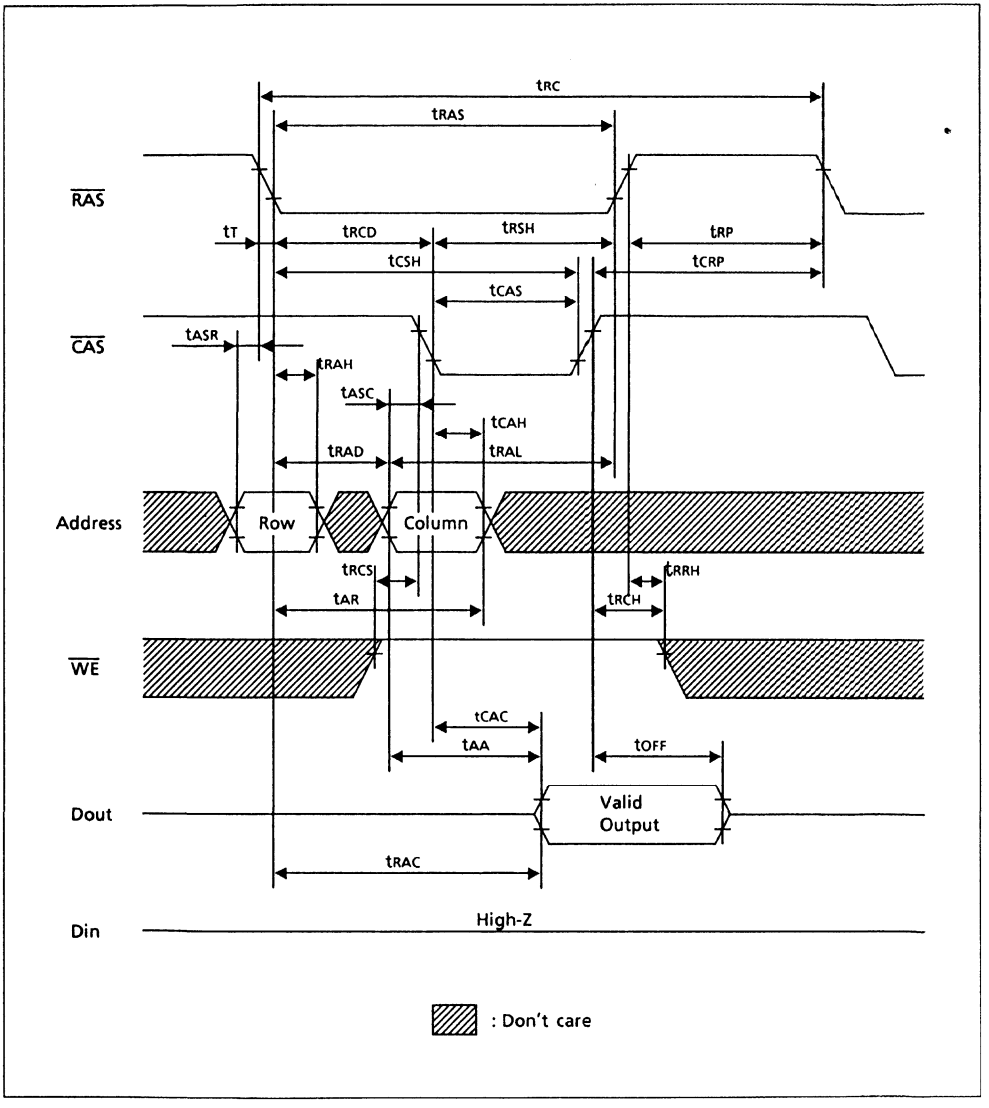
Fast Page Mode Cycle

		HB56D25609A/B							
		-85A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	

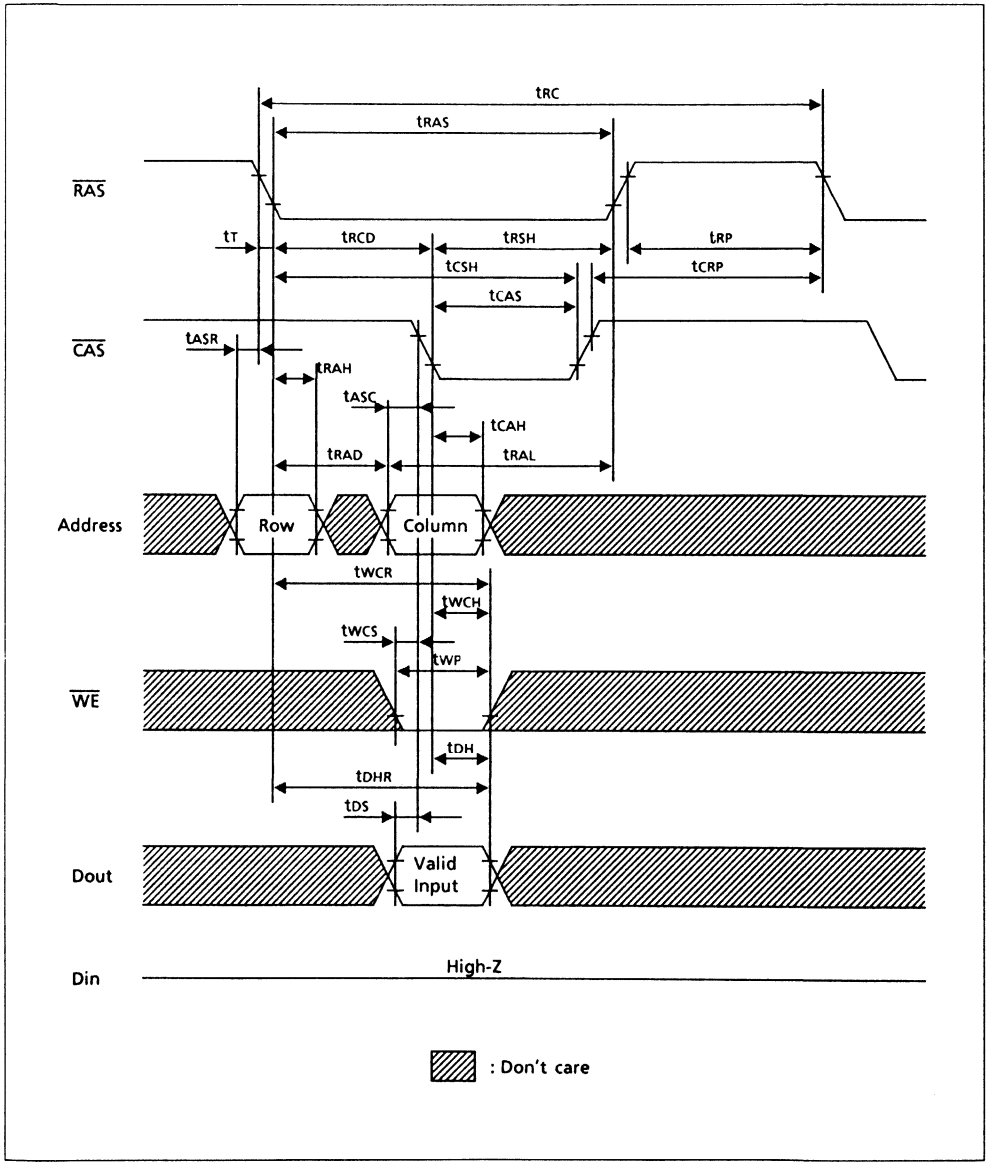
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

Timing Waveforms

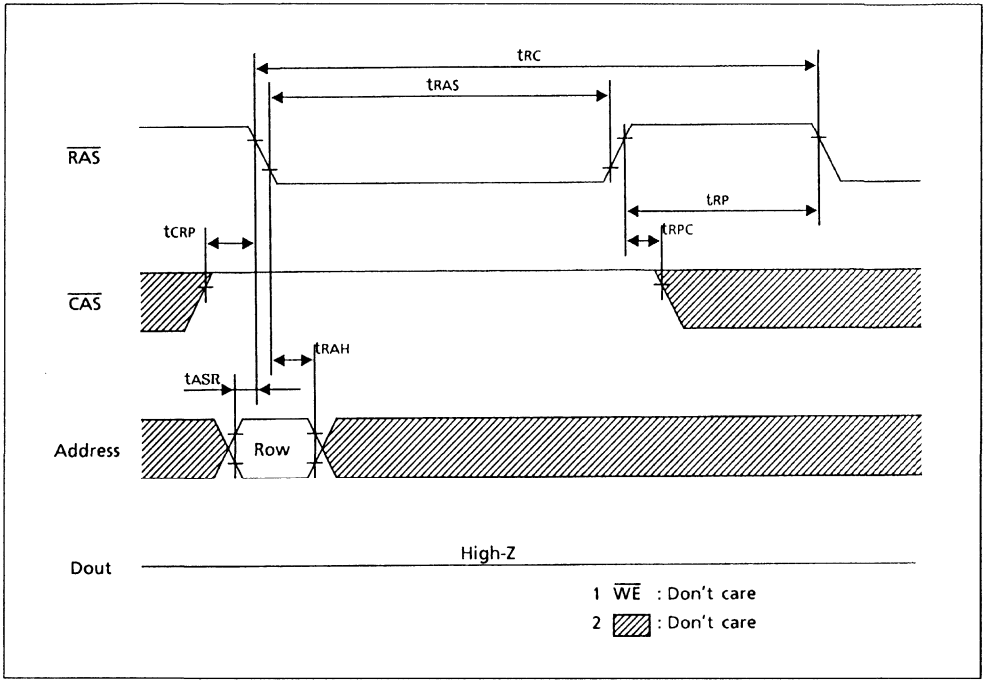
Read Cycle



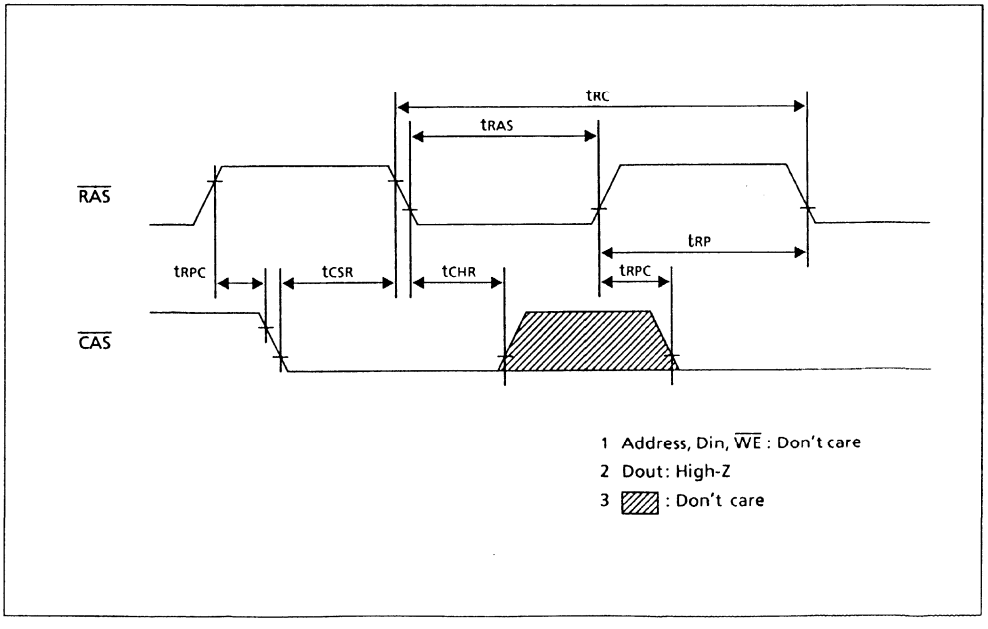
Early Write Cycle



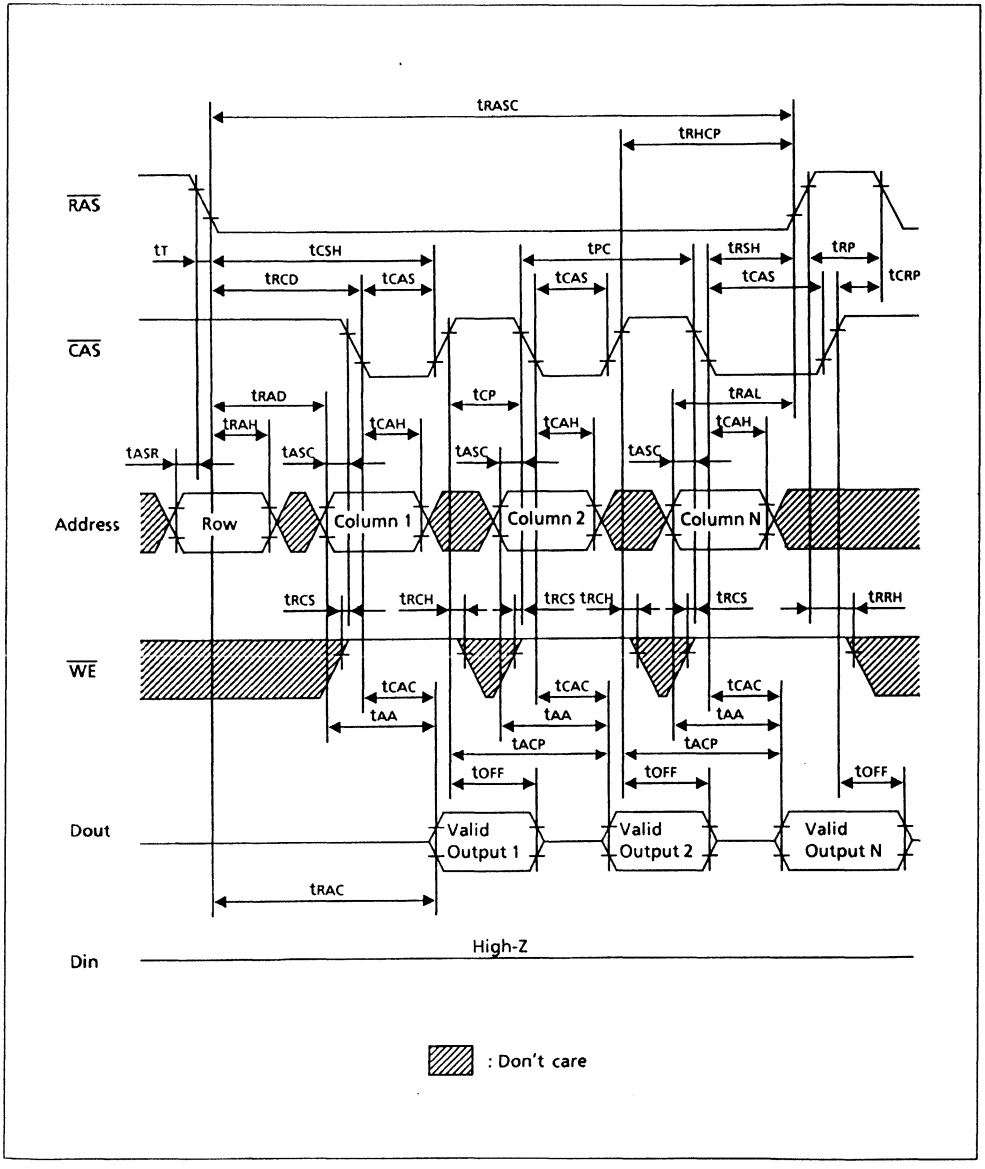
$\overline{RAS}$-Only Refresh Cycle



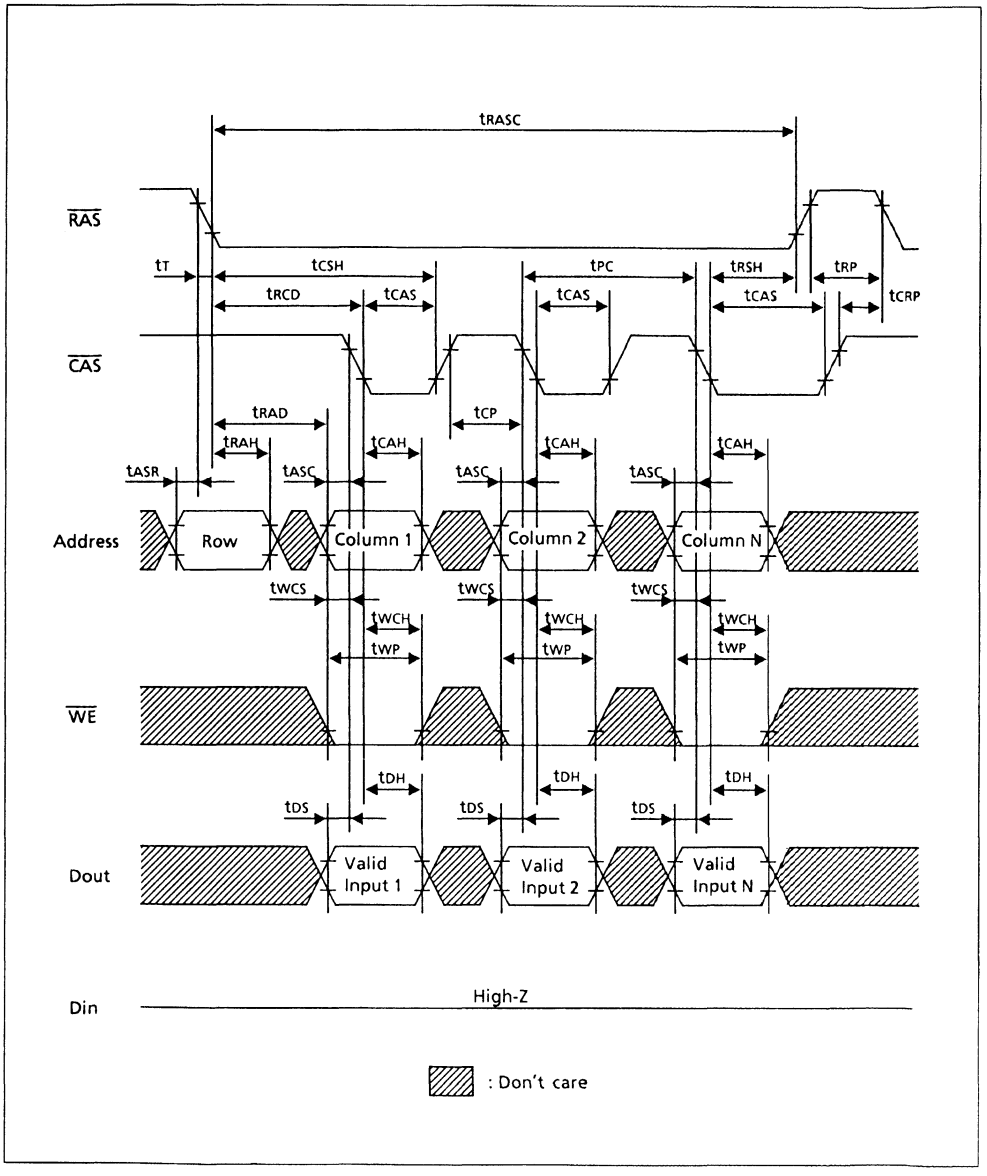
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle



Fast Page Mode Read Cycle



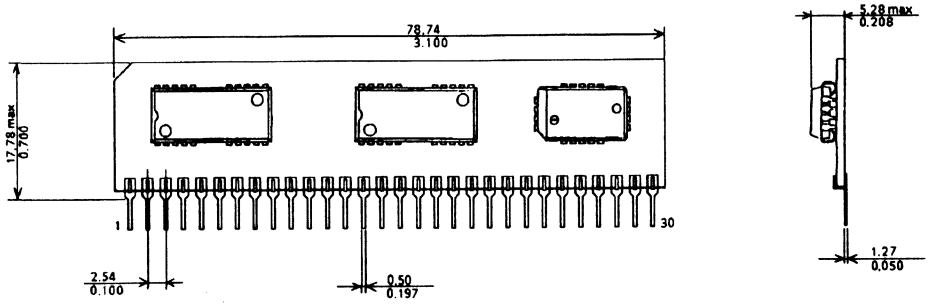
Fast Page Mode Early Write Cycle



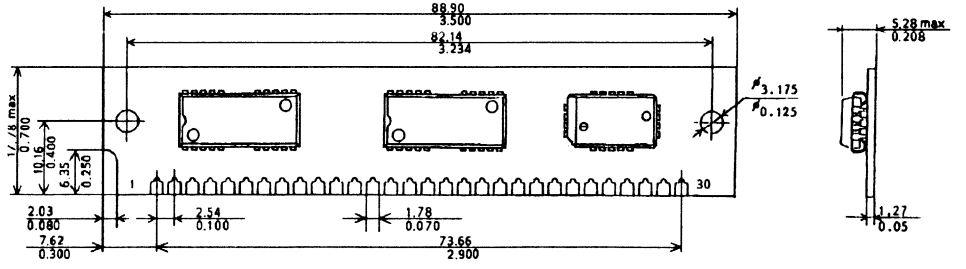
Physical Outline

Unit: mm/inch

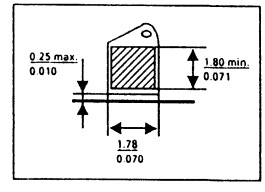
HB56D25609A series



HB56D25609B series



Detail A



Note: The plating of the contact finger is solder coat.

HB56D25608 Series

262,144-Word × 8-Bit High Density Dynamic RAM Module

The HB56D25608 is a 256k × 8 dynamic RAM module, mounted two 1-Mbit DRAM (HM514256JP) sealed in SOJ package. An outline of the HB56D25608 is 30-pin single in-line package having lead types (HB56D25608A), socket type (HB56D25608B). Therefore, the HB56D25608 makes high density mounting possible without surface mount technology. The HB56D25608 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

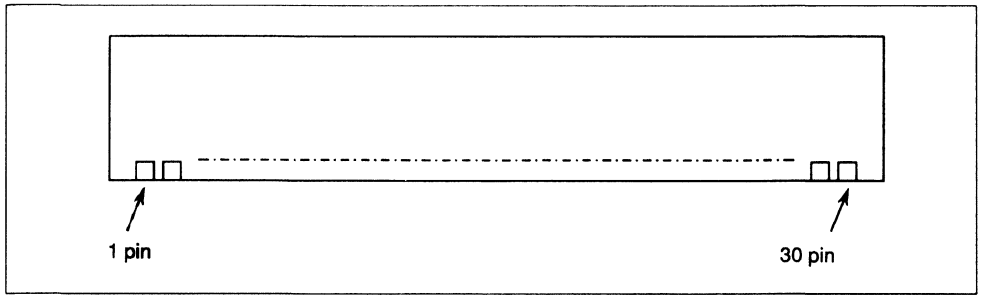
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time:
    60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 990 mW/880 mW/726 mW/
    605 mW/517 mW (max)
  - Standby mode: 22 mW (max)
- Fast page mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  $\overline{\text{RAS}}$-only refresh
  $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Type No.	Access time	Package
HB56D25608A-6A	60 ns	30-pin SIP lead type	HB56D25608B-6A	60 ns	30-pin SIP socket type
HB56D25608A-7A	70 ns		HB56D25608B-7A	70 ns	
HB56D25608A-8A	80 ns		HB56D25608B-8A	80 ns	
HB56D25608A-10A	100 ns		HB56D25608B-10A	100 ns	
HB56D25608A-12A	120 ns		HB56D25608B-12A	120 ns	

Pin Arrangement

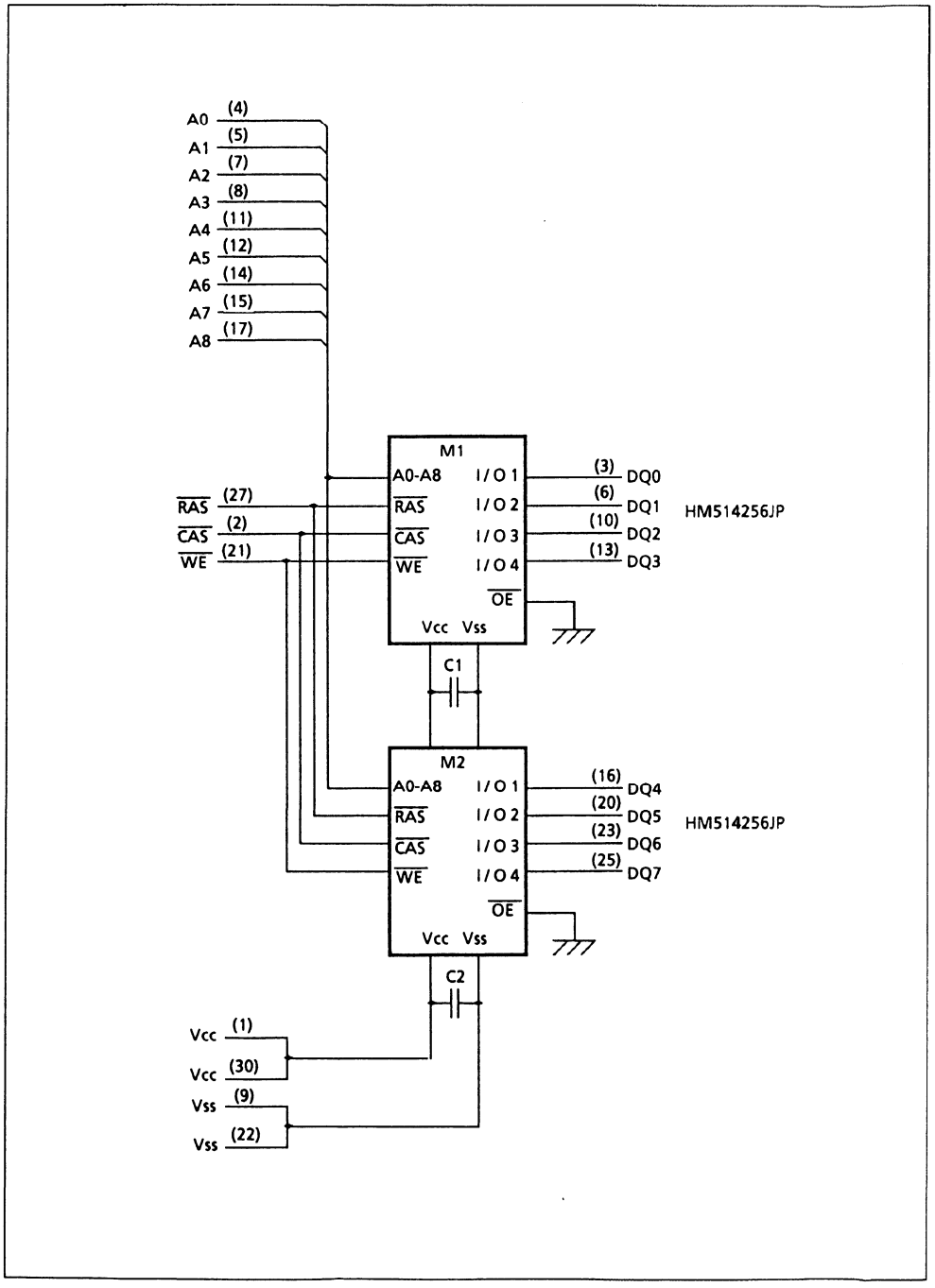


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	NC
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	NC
12	A5	27	$\overline{RAS}$
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A8	Address input
A0 – A8	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	2	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Condtions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56D25608A/B												
		-6A		-7A		-8A		-10A		-12A				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	180	—	160	—	132	—	110	—	94	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	4	—	4	—	4	—	4	—	4	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	2	—	2	—	2	—	2	—	2	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	180	—	160	—	132	—	110	—	94	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	10	—	10	—	10	—	10	—	10	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	180	—	160	—	132	—	110	—	94	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	180	—	160	—	110	—	110	—	94	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high current	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{i1}	—	25	pF	1
Input capacitance (Clock)	C_{I2}	—	30	pF	1
Input / output capacitance (DQ0 – DQ7)	$C_{I/O1}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V) *1, *12

Read, Write and Refresh Cycle (Common Parameter)

		HB56D25608A/B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Random read or write cycle time	t_{RC}	125	—	140	—	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	55	—	60	—	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	40	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	80	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	—	8	ms	15

Read Cycle

		HB56D25608A/B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	60	—	70	—	80	—	100	—	120	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	20	—	25	—	25	—	30	ns	3, 4
Access time from address	t_{AA}	—	30	—	35	—	40	—	45	—	55	ns	3, 5
Read command setup time	t_{RCS}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	—	35	—	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	—	20	—	20	—	20	—	25	—	30	ns	6

Write Cycle

		HB56D25608A/B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	20	—	20	—	25	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	15	—	15	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	15	—	15	—	20	—	20	—	25	—	ns	11

Refresh Cycle

		HB56D25608A/B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	15	—	15	—	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10	—	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

		HB56D25608A/B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Fast page mode cycle time	t_{PC}	45	—	50	—	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	10	—	10	—	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	60	100000	70	100000	80	100000	100	100000	120	100000	ns	13
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	—	45	—	50	—	50	—	60	ns	14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	45	—	50	—	50	—	60	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

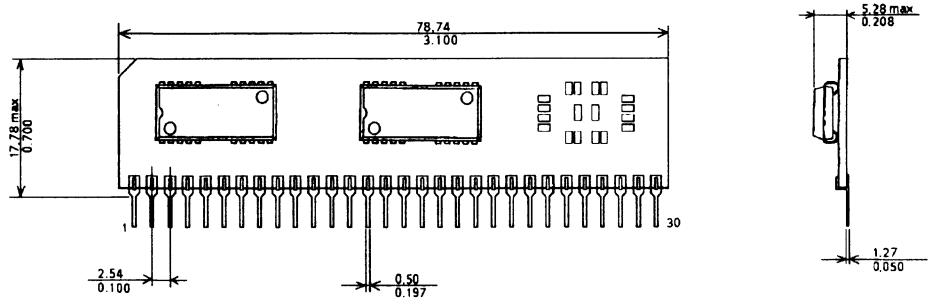
Timing Waveforms

Refer to the HB56D25609 data sheet.

Physical Outline

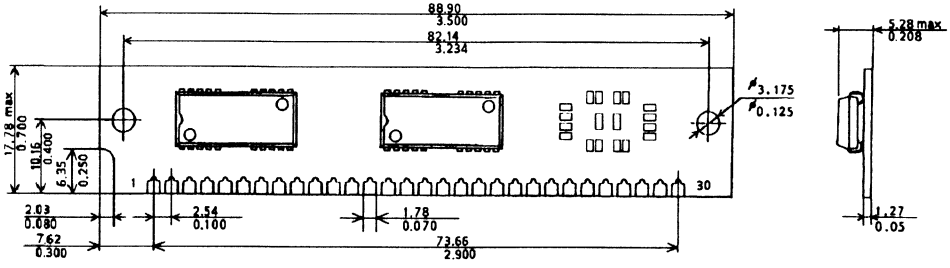
Unit: mm/inch

HB56D25608A Series

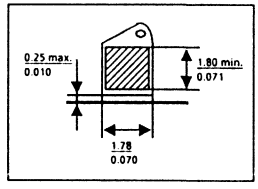


Unit: mm/inch

HB56D25608B Series



Detail A



Note: The plating of the contact finger is solder coat.

HB56D25636B Series

262,144-Word × 36-Bit High Density Dynamic RAM Module

The HB56D25636B is a 256k × 36 dynamic RAM module, mounted 8 pieces of 1-Mbit DRAM (HM514256JP) sealed in SOJ package and 4 pieces of 256-kbit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB56D25636B is 72-pin single in-line package. Therefore, the HB56D25636B makes high density mounting possible without surface mount technology. The HB56D25636B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ and each PLCC.

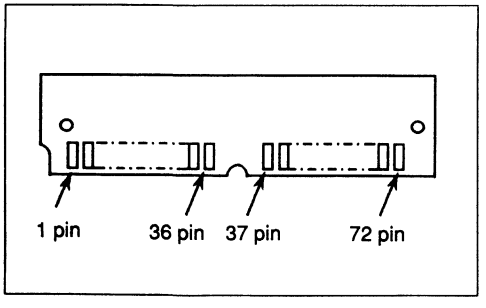
Features

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: 85 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 4.24 W/3.57 W/3.02 W (max)
  - Standby mode: 126 mW (max)
- Fast page mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HB56D25636B-85	85 ns	72-pin SIP socket type
HB56D25636B-10	100 ns	
HB56D25636B-12	120 ns	

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	NC	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

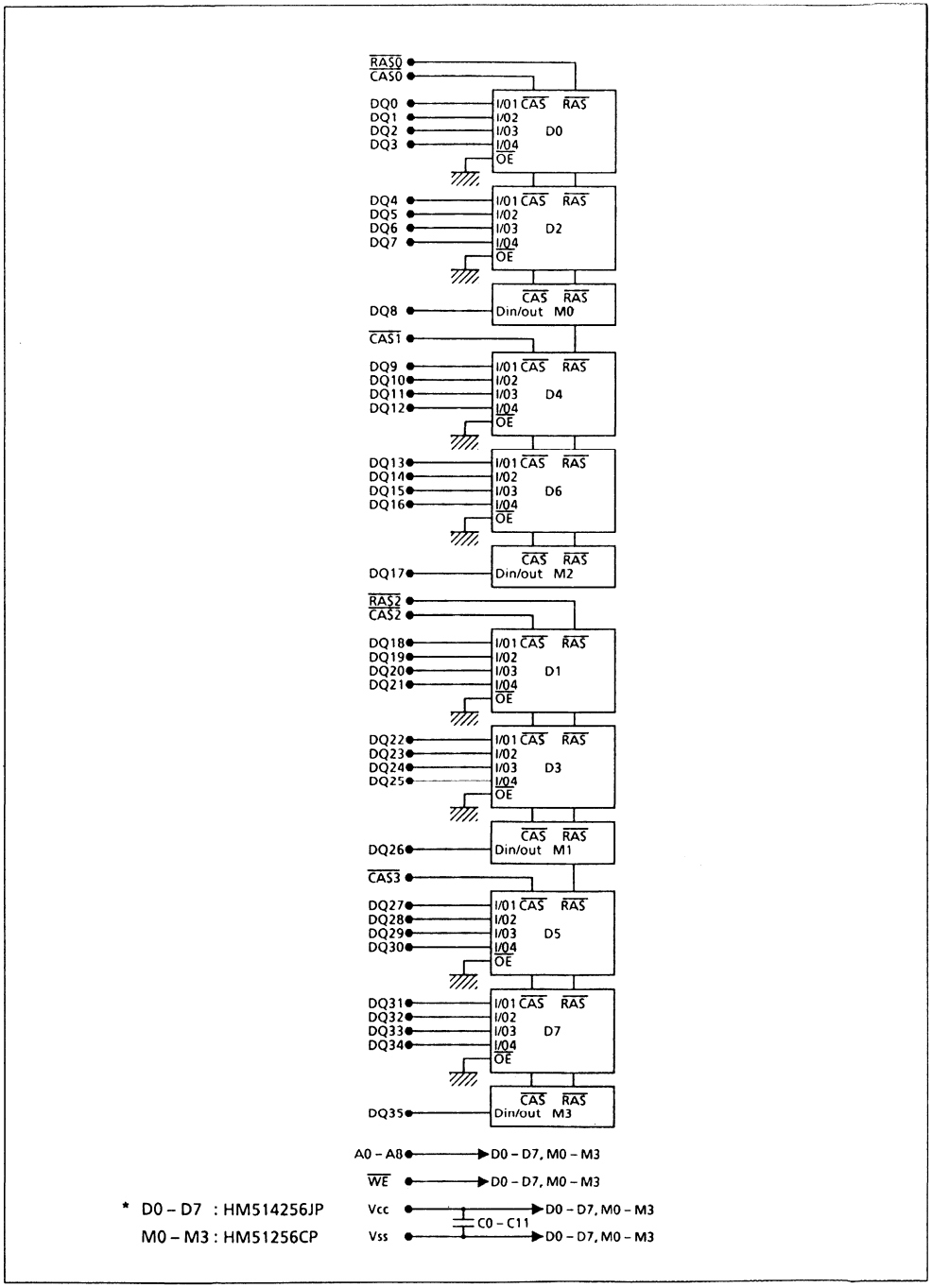
Pin Description

Pin name	Function
A0 – A8	Address input
A0 – A8	Refresh address input
DQ0 – DQ35	Data-in/data-out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$ – $\overline{RAS2}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56D25636B		
Pin No.	Pin name	85ns	100ns	120ns
67	PD1	V_{SS}	V_{SS}	V_{SS}
68	PD2	NC	NC	NC
69	PD3	NC	V_{SS}	NC
70	PD4	V_{SS}	V_{SS}	NC

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	Vin	–1.0 to +7.0	V
	(Output)	Vout	–1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	–1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	12	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	88	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output capacitance (DQ0 – DQ7, DQ9 – DQ16, DQ18 – DQ25, DQ27 –DQ34)	$C_{I/O1}$	—	17	pF	1, 2
Output capacitance (DQ8, DQ17, DQ26, DQ35)	$C_{I/O2}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56D25636B-85		HB56D25636B-10		HB56D25636B-12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	808	—	680	—	576	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	24	—	24	—	24	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	12	—	12	—	12	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	808	—	680	—	576	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	64	—	64	—	64	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	768	—	660	—	556	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	764	—	680	—	576	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) *1, *12

Read, Write and Refresh Cycle (Common parameters)

		HB56D25636B-85		HB56D25636B-10		HB56D25636B-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
Column address hold time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	15

Read Cycle

		HB56D25636B-85		HB56D25636B-10		HB56D25636B-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access time from address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

		HB56D25636B-85		HB56D25636B-10		HB56D25636B-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	20	—	25	—	30	—	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	20	—	20	—	25	—	ns	11
Data-in hold time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

Refresh Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	15	—	15	—	15	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56D25636B-85		HB56D25636B-10		HB56D25636B-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	

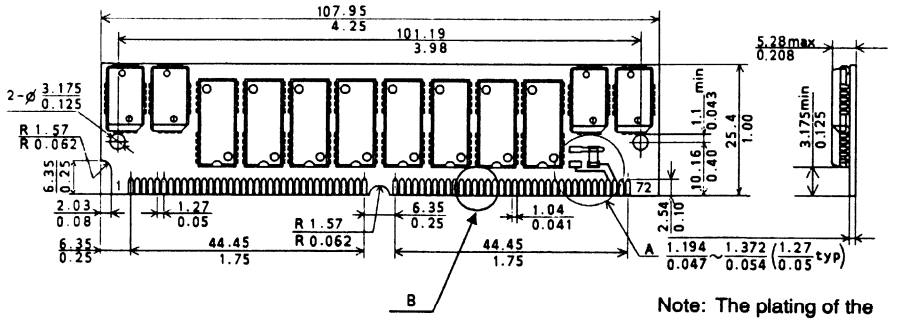
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

Timing Waveforms

Refer to the HB56D25609 data sheet.

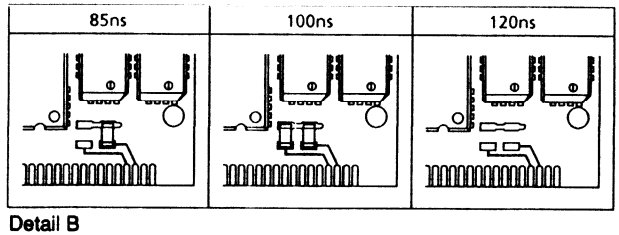
Physical Outline

Unit: mm/inch

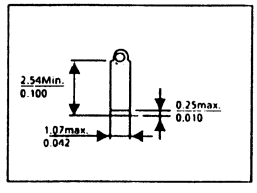


Note: The plating of the contact finger is gold.

Detail A



Detail B



HB56D51236B Series

524,288-Word × 36-Bit High Density Dynamic RAM Module

The HB56D51236B is a 512k × 36 dynamic RAM module, mounted 16 pieces of 1-Mbit DRAM (HM514256JP) sealed in SOJ package and 8 pieces of 256-kbit DRAM (HM51256CP) sealed in PLCC package. An outline of the HB56D51236B is 72-pin single in-line package. Therefore, the HB56D51236B makes high density mounting possible without surface mount technology. The HB56D51236B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ and each PLCC but only on the one side of its module board.

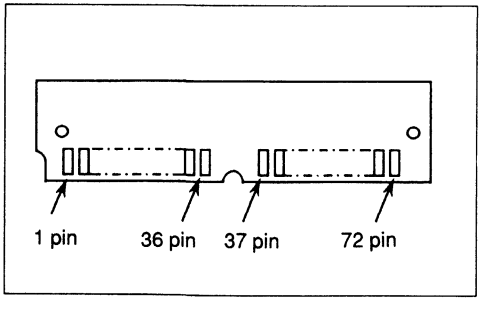
Features

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: 85 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 4.58 W/3.91 W/3.36 W (max)
  - Standby mode: 252 mW (max)
- Fast page mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HB56D51236B-85	85 ns	72-pin SIP socket type
HB56D51236B-10	100 ns	
HB56D51236B-12	120 ns	

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{RAS1}$	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	NC	50	DQ27	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

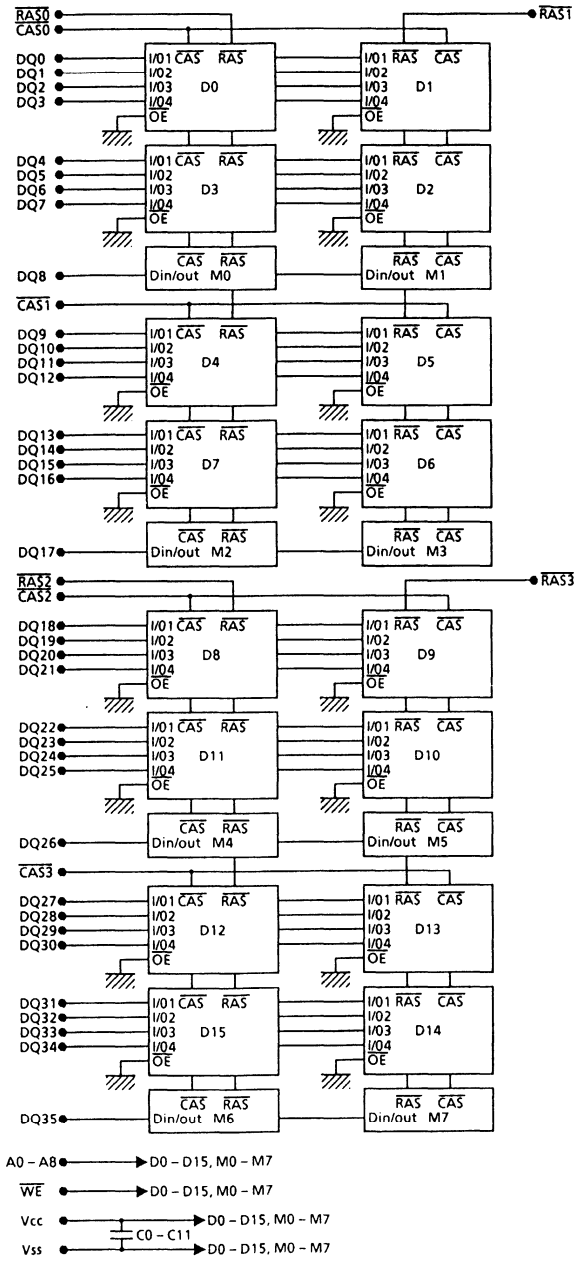
Pin Description

Pin name	Function
A0 – A8	Address input
A0 – A8	Refresh address input
DQ0 – DQ35	Data-in/data-out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$ – $\overline{RAS3}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56D51236B		
Pin No.	Pin name	85ns	100ns	120ns
67	PD1	NC	NC	NC
68	PD2	V_{SS}	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}	NC
70	PD4	V_{SS}	V_{SS}	NC

Block Diagram



* D0 – D15: HM514256JP
M0 – M7 : HM51256CP

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	Vin	−1.0 to +7.0	V
	(Output)	Vout	−1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	12	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	−55 to +125	°C

Recommended DC Operating Condtions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	161	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output capacitance (DQ0 – DQ7, DQ9 – DQ16, DQ18 – DQ25, DQ27 –DQ34)	$C_{I/O1}$	—	29	pF	1, 2
Output capacitance (DQ8, DQ17, DQ26, DQ35)	$C_{I/O2}$	—	39	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56D51236B-85		HB56D51236B-10		HB56D51236B-12				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	872	—	744	—	640	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	48	—	48	—	48	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	24	—	24	—	24	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	872	—	744	—	640	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	128	—	128	—	128	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$-refresh current	I_{CC6}	—	832	—	724	—	620	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	828	—	744	—	640	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) *1, *12

Read, Write and Refresh Cycle (Common parameters)

		HB56D51236B-85		HB56D51236B-10		HB56D51236B-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Ramdom read or write cycle time	t_{RC}	160	—	190	—	220	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	30	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	25	—	ns	
Column address hold time to $\overline{RAS}$	t_{AR}	60	—	75	—	90	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	25	90	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	45	20	55	20	65	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	8	—	8	—	8	ms	15

Read Cycle

		HB56D51236B-85		HB56D51236B-10		HB56D51236B-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	85	—	100	—	120	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	—	30	ns	3, 4
Access time from address	t_{AA}	—	40	—	45	—	55	ns	3, 5
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	55	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	25	0	30	ns	6

Write Cycle

		HB56D51236B-85		HB56D51236B-10		HB56D51236B-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	20	—	25	—	30	—	ns	
Write command hold time to $\overline{RAS}$	t_{WCR}	65	—	80	—	95	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	25	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	20	—	20	—	25	—	ns	11
Data-in hold time to $\overline{RAS}$	t_{DHR}	60	—	75	—	90	—	ns	

Refresh Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	25	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	15	—	15	—	15	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56D51236B-85		HB56D51236B-10		HB56D51236B-12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	55	—	55	—	65	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	20	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	120	100000	ns	13
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	—	60	ns	14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	60	—	ns	

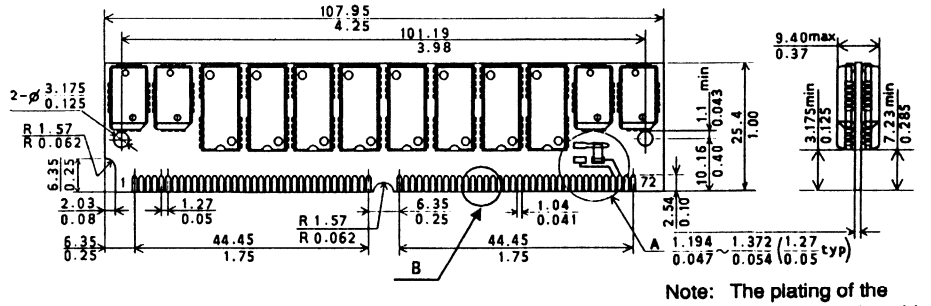
Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 512 refresh cycles.

Timing Waveforms

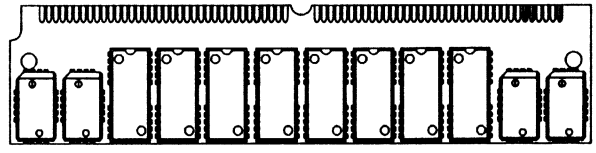
Refer to the HB56D25609 data sheet.

Physical Outline

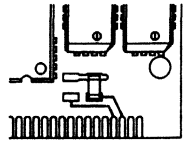
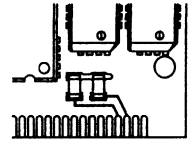
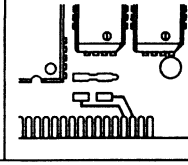
Unit: mm/inch



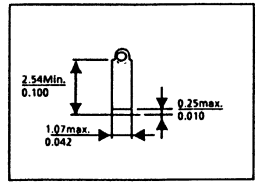
Note: The plating of the contact finger is gold.



Detail A

85ns	100ns	120ns
		

Detail B



HB56A19 Series

1,048,576-Word × 9-Bit High Density Dynamic RAM Module

The HB56A19 is a 1M × 9 dynamic RAM module, mounted nine 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A19 is 30-pin single in-line package having lead types (HB56A19A, HB56A19AT), socket type (HB56A19B). Therefore, the HB56A19 makes high density mounting possible without surface mount technology. The HB56A19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

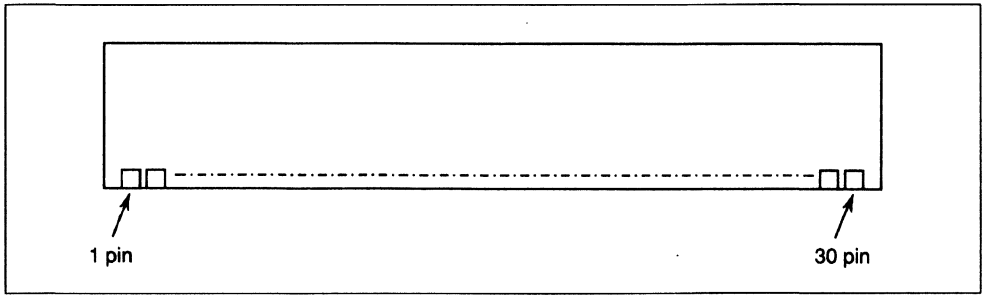
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time: 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 4455 mW/3960 mW/3465 mW 2970 mW/2475 mW (max)
  - Standby mode: 99 mW (max)
- Fast page mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

	Package		
Access time	**30-pin SIP Lead type**	**30-pin SIP Low Profile Lead type**	**30-pin SIP Socket type**
60 ns	HB56A19A-6A	HB56A19AT-6A	HB56A19B-6A
70 ns	HB56A19A-7A	HB56A19AT-7A	HB56A19B-7A
80 ns	HB56A19A-8A	HB56A19AT-8A	HB56A19B-8A
100 ns	HB56A19A-10A	HB56A19AT-10A	HB56A19B-10A
120 ns	HB56A19A-12A	HB56A19AT-12A	HB56A19B-12A

Pin Arrangement

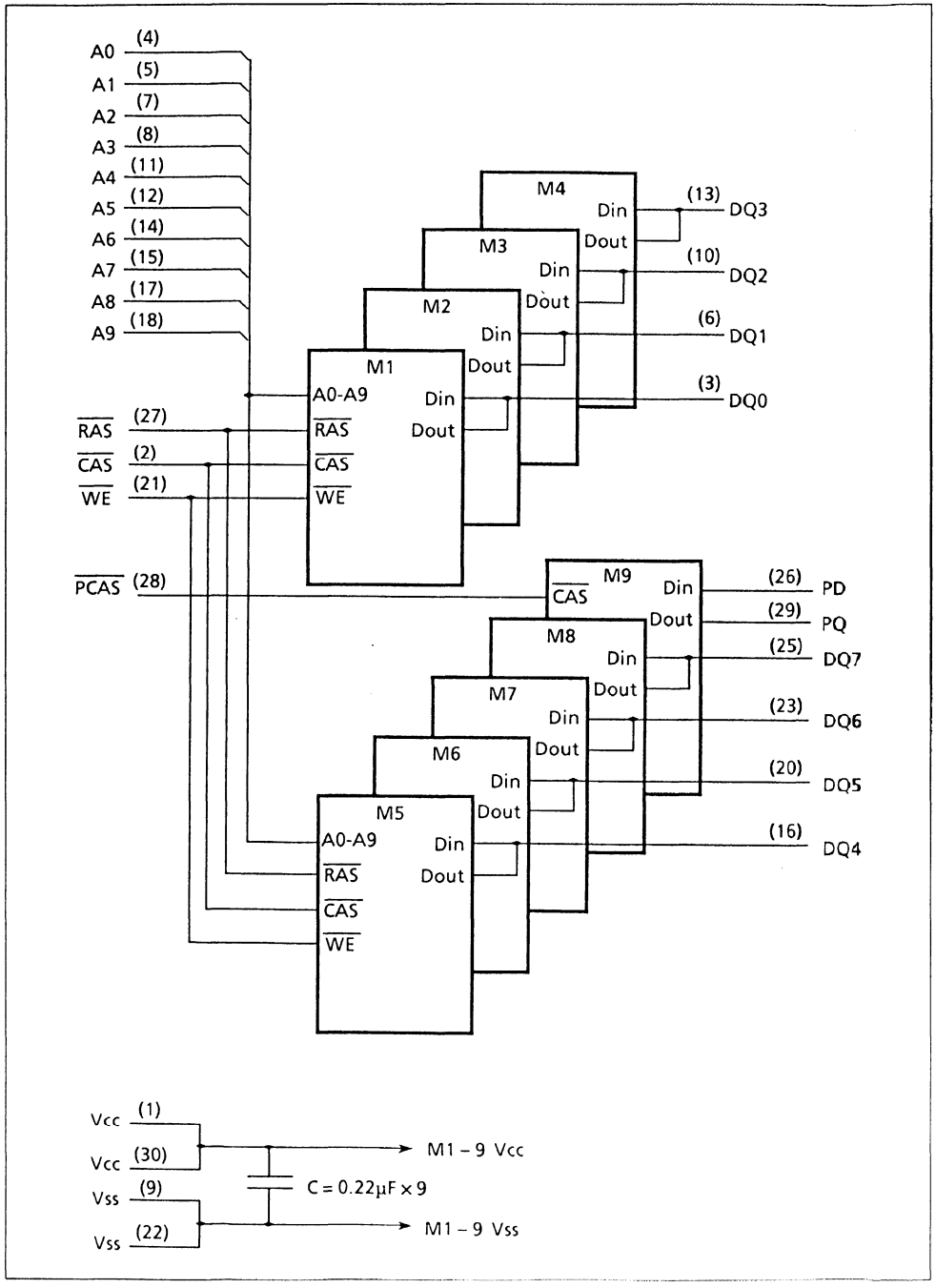


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCAS}$
14	A6	29	PD
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$, $\overline{PCAS}$	Column address strobe
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
PD	Data-in for parity
PQ	Data-out for parity
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	Vin	−1.0 to +7.0	V
	(output)	Vout	−1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	9	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56A19A/AT/B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	810	—	720	—	630	—	540	—	450	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	18	—	18	—	18	—	18	—	18	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	9	—	9	—	9	—	9	—	9	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}–0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	810	—	720	—	540	—	450	—	405	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	45	—	45	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	810	—	720	—	540	—	450	—	360	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	810	—	720	—	450	—	450	—	360	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	60	pF	1
Input capacitance (Clock)	C_{I2}	—	75	pF	1
Input/output capacitance (DQ0 – DQ7)	$C_{I/O}$	—	17	pF	1, 2
Input capacitance (PD)	C_{I3}	—	10	pF	1, 2
Output capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

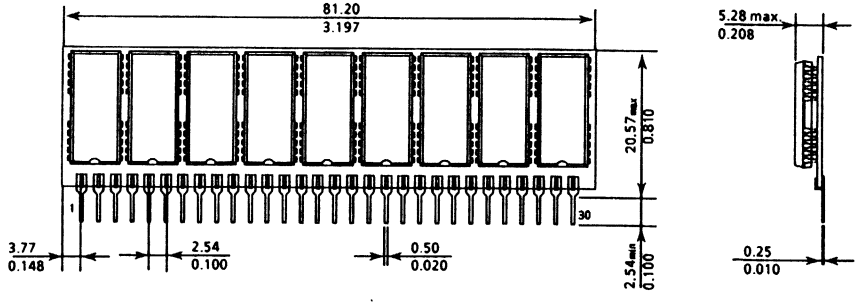
AC Characteristics

Refer to the HM511000A data sheet for AC characteristics. The HB56A19 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

Physical Outline

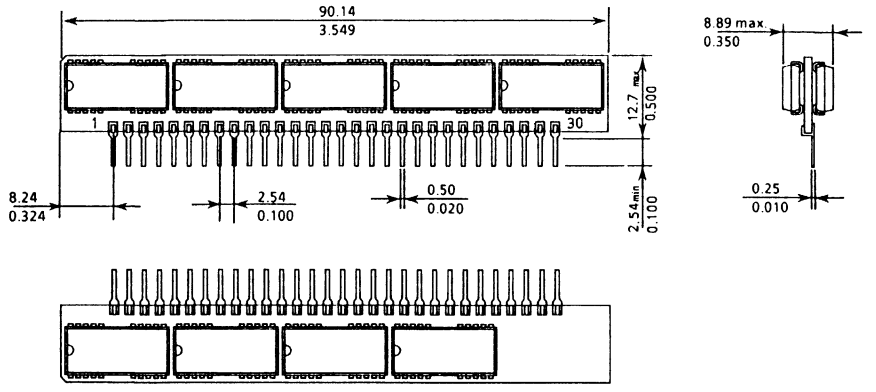
Unit: mm/inch

HB56A19A series



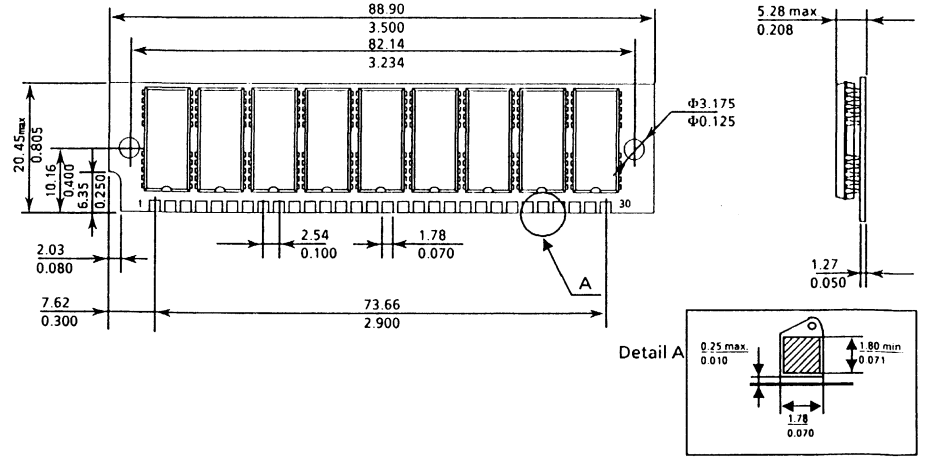
Unit: mm/inch

HB56A19AT series



Unit: mm/inch

HB56A19B series



Note: The plating of the contact finger is solder coat.

HB56A18 Series

1,048,576-Word × 8-Bit High Density Dynamic RAM Module

The HB56A18 is a 1M × 8 dynamic RAM module, mounted eight 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A18 is 30-pin single in-line package having lead types (HB56A18A, HB56A18AT), socket type (HB56A18B). Therefore, the HB56A18 makes high density mounting possible without surface mount technology. The HB56A18 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

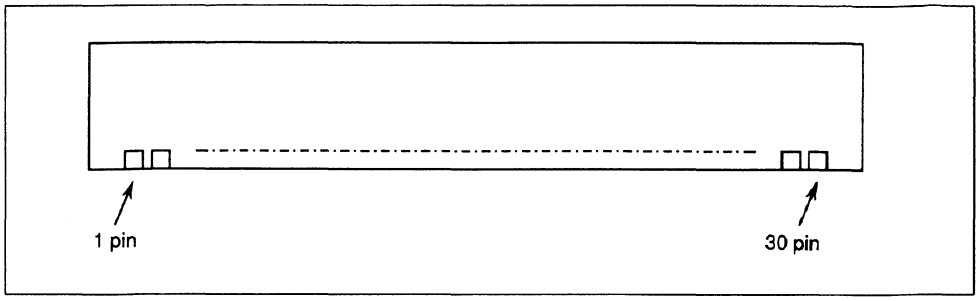
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time: 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 3.96 W/3.52 W/3.08 W 2.64 W/2.20 W (max)
  - Standby mode: 88 mW (max)
- Fast page mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

	Package		
Access time	30-pin SIP Lead type	30-pin SIP Low Profile Lead type	30-pin SIP Socket type
60 ns	HB56A18A-6A	HB56A18AT-6A	HB56A18B-6A
70 ns	HB56A18A-7A	HB56A18AT-7A	HB56A18B-7A
80 ns	HB56A18A-8A	HB56A18AT-8A	HB56A18B-8A
100 ns	HB56A18A-10A	HB56A18AT-10A	HB56A18B-10A
120 ns	HB56A18A-12A	HB56A18AT-12A	HB56A18B-12A

Pin Arrangement

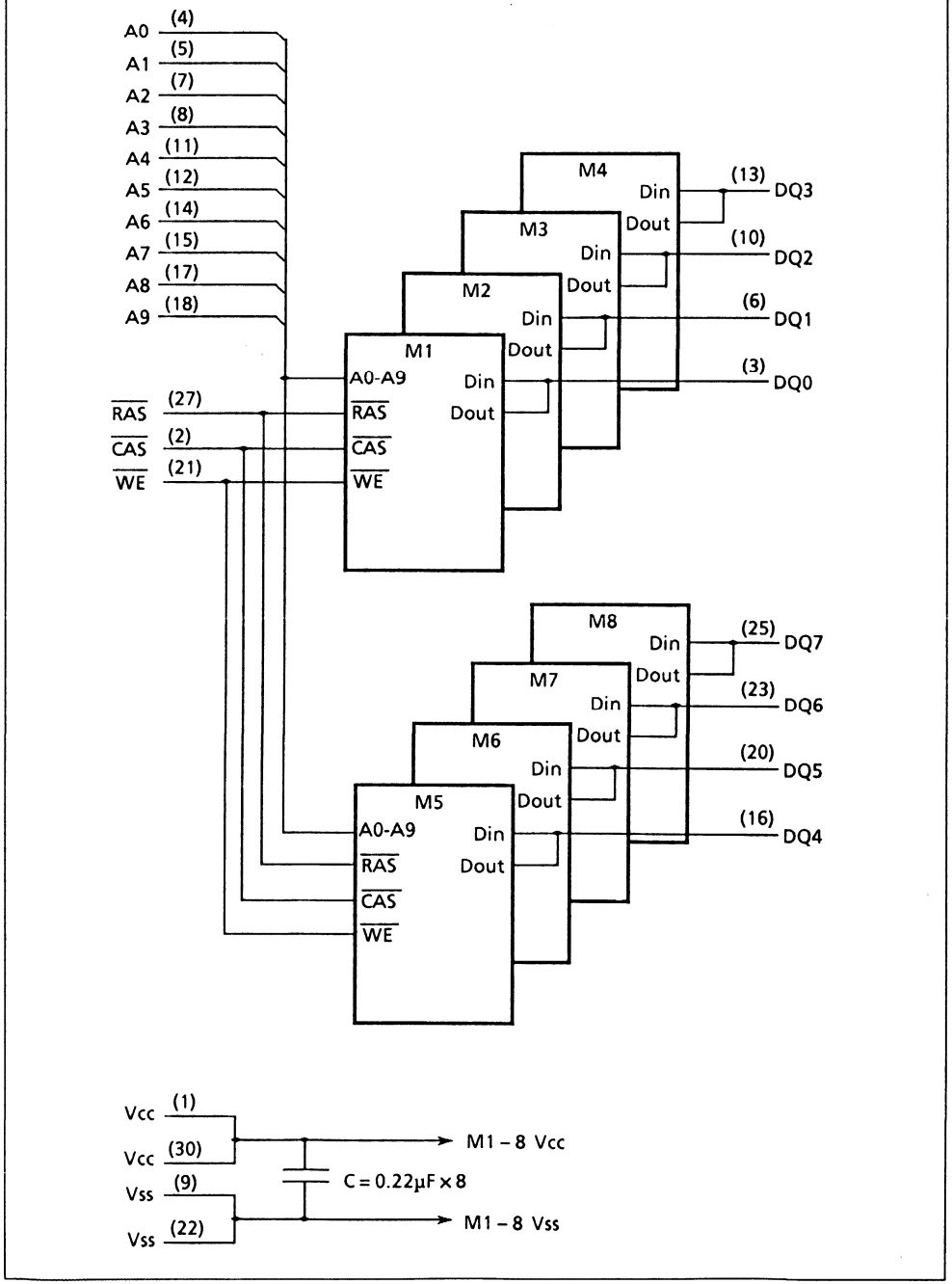


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	NC
12	A5	27	$\overline{RAS}$
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	(Input)	Vin	−1.0 to +7.0	V
	(output)	Vout	−1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	−1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	8	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56A18A/AT/B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	720	—	640	—	560	—	480	—	400	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	—	8	—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}–0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	720	—	640	—	480	—	400	—	360	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	720	—	640	—	480	—	400	—	320	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	720	—	640	—	400	—	400	—	320	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	55	pF	1
Input capacitance (Clock)	C_{I2}	—	70	pF	1
Input/output capacitance (DQ0 – DQ7)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

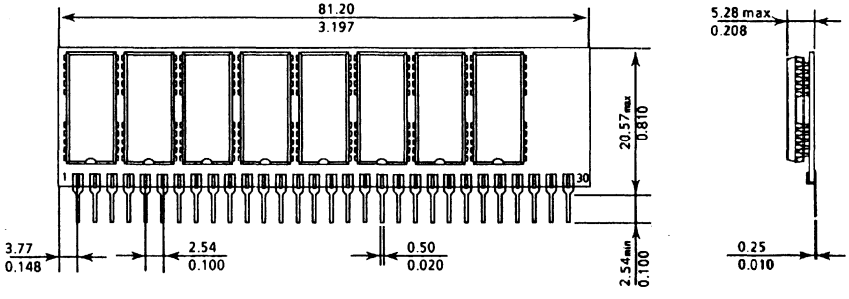
AC Characteristics

Refer to the HM511000A data sheet for AC characteristics. The HB56A18 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

Physical Outline

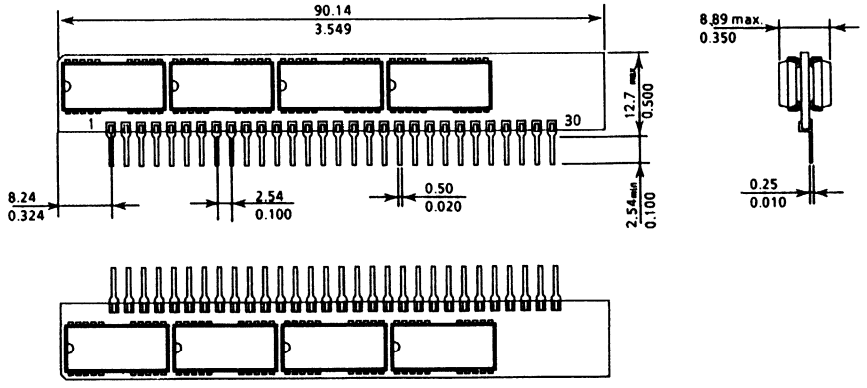
Unit: mm/inch

HB56A18A series



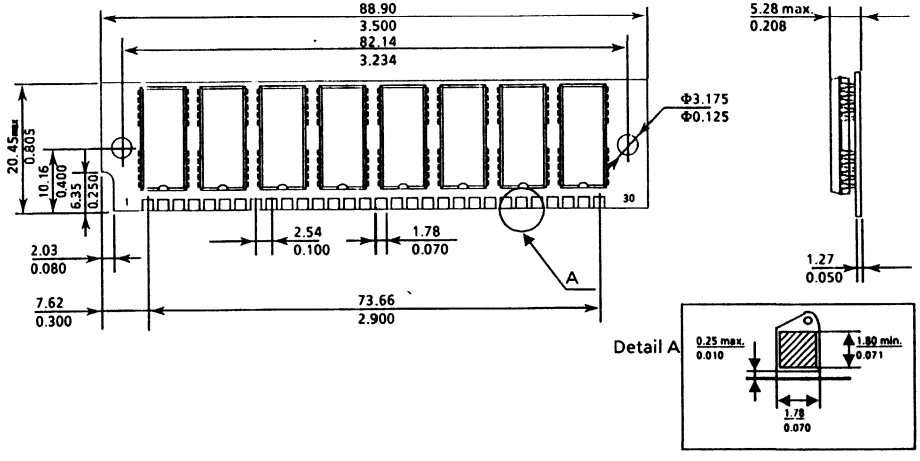
Unit: mm/inch

HB56A18AT series



Unit: mm/inch

HB56A18B series



Note: The plating of the contact finger is solder coat.

HB56A24B Series

Dual 1,048,576-Word × 4-Bit High Density Dynamic RAM Module

The HB56A24B is a dual 1M × 4 dynamic RAM module, mounted eight 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56A24B is 30-pin single in-line package. Therefore, the HB56A24B makes high density mounting possible without surface mount technology. The HB56A24B provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

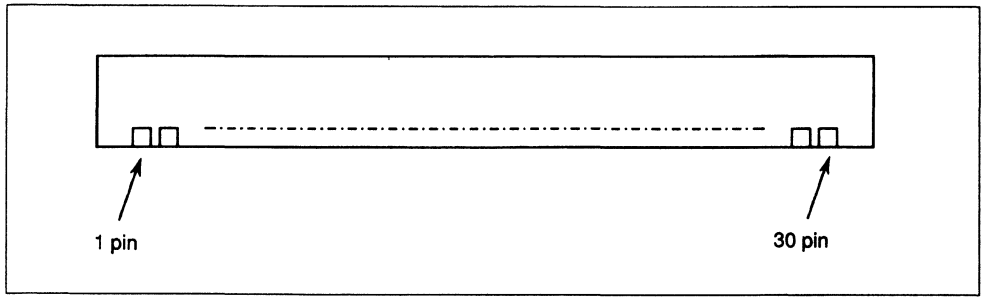
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time: 60 ns/70 ns/80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 3.96 W/3.52 W/3.08 W 2.64 W/2.20 W (max)
  - Standby mode: 22 mW (max)
- Fast page mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package
HB56A24B-6A	60 ns	30-pin SIP socket type
HB56A24B-7A	70 ns	
HB56A24B-8A	80 ns	
HB56A24B-10A	100 ns	
HB56A24B-12A	120 ns	

Pin Arrangement

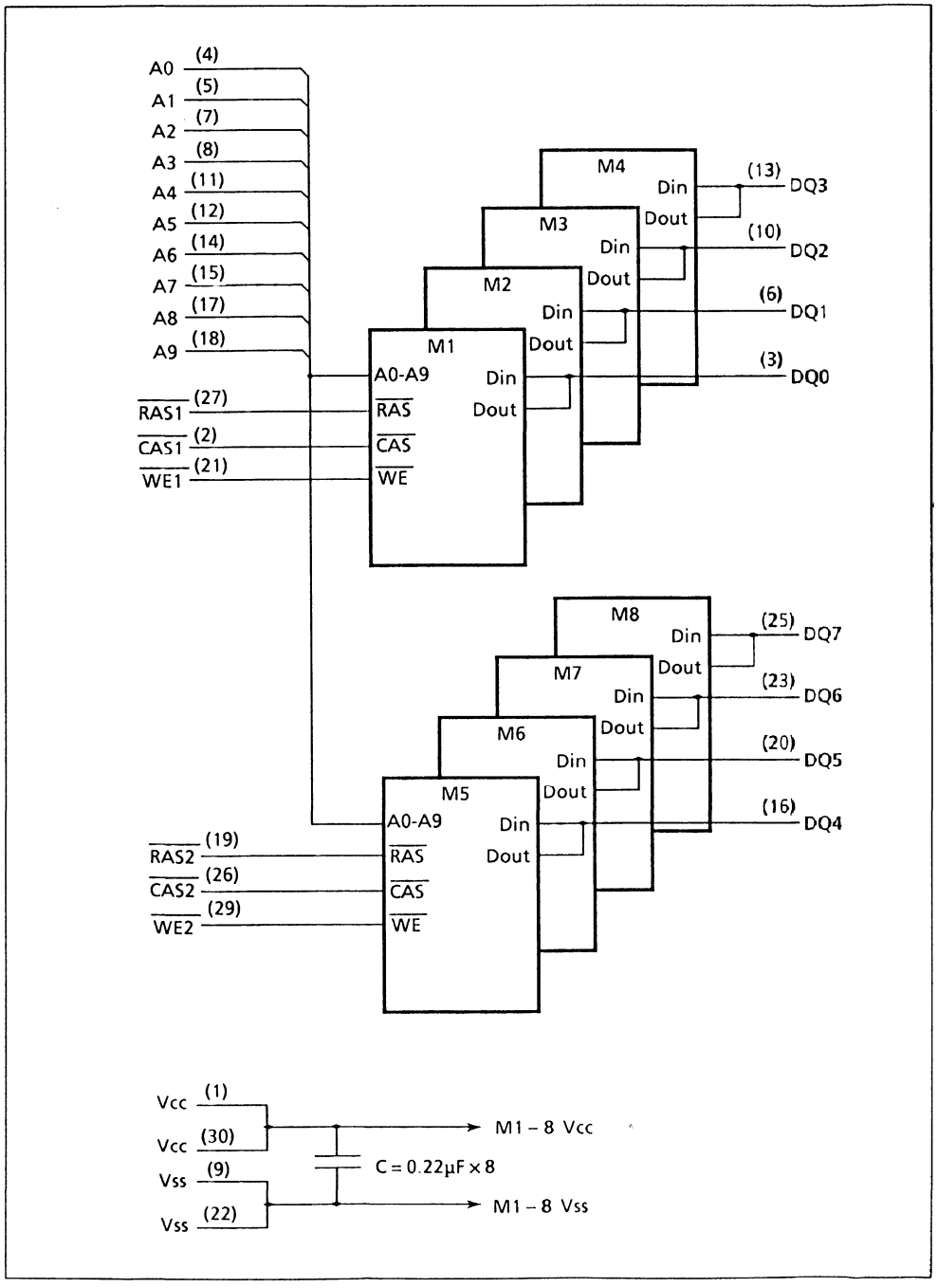


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CAS1}$	17	A8
3	DQ0	18	A9
4	A0	19	$\overline{RAS2}$
5	A1	20	DQ5
6	DQ1	21	$\overline{WE1}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	$\overline{CAS2}$
12	A5	27	$\overline{RAS1}$
13	DQ3	28	NC
14	A6	29	$\overline{WE2}$
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
$\overline{RAS1}$, $\overline{RAS2}$	Row address strobe
$\overline{CAS1}$, $\overline{CAS2}$	Column address strobe
$\overline{WE1}$, $\overline{WE2}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	8.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56A24B											
		-6A		-7A		-8A		-10A		-12A			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	720	—	640	—	560	—	480	—	400	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	—	8	—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC}–0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	720	—	640	—	480	—	400	—	360	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	720	—	640	—	480	—	400	—	320	mA	t_{RC} = min	
Fast page mode current	I_{CC7}	—	720	—	640	—	400	—	400	—	320	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	55	pF	1
Input capacitance (Clock)	C_{I2}	—	44	pF	1
Input/output capacitance (DQ0 – DQ7)	$C_{I/O1}$	—	17	pF	1, 2

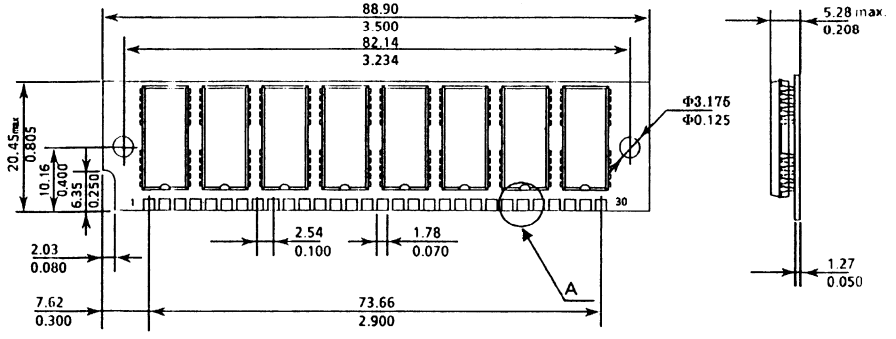
Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

AC Characteristics

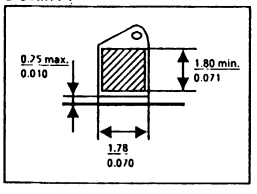
Refer to the HM511000A data sheet for AC characteristics. The HB56A24B writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

Physical Outline

Unit: mm/inch



Detail A



Note: The plating of the contact finger is solder coat.

HB56C19 Series

1,048,576-Word × 9-Bit High Density Dynamic RAM Module

The HB56C19 is a 1M × 9 static column mode dynamic RAM module, mounted nine 1-Mbit DRAM (HM511002JP) sealed in SOJ package. An outline of the HB56C19 is 30-pin single in-line package having lead types (HB56C19A, HB56C19AT), socket type (HB56C19B). Therefore, the HB56C19 makes high density mounting possible without surface mount technology. The HB56C19 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

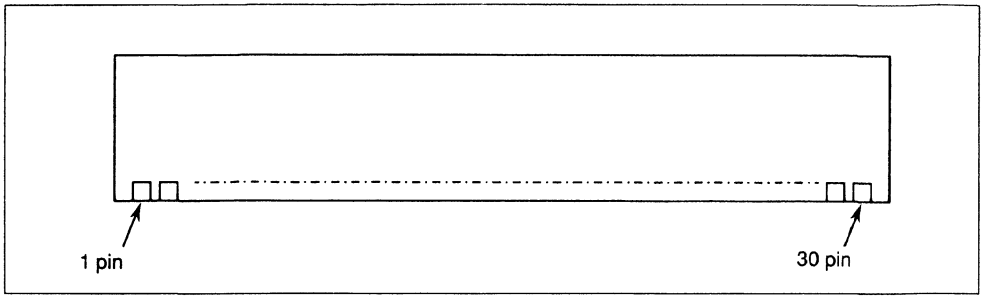
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time: 80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 3465 mW/2970 mW/2475 mW (max)
  - Standby mode: 99 mW (max)
- Static column mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

	Package		
Access time	**30-pin SIP Lead type**	**30–pin SIP Low Profile Lead type**	**30-pin SIP Socket type**
80 ns	HB56C19A-8A	HB56C19AT-8A	HB56C19B-8A
100 ns	HB56C19A-10A	HB56C19AT-10A	HB56C19B-10A
120 ns	HB56C19A-12A	HB56C19AT-12A	HB56C19B-12A

Pin Arrangement

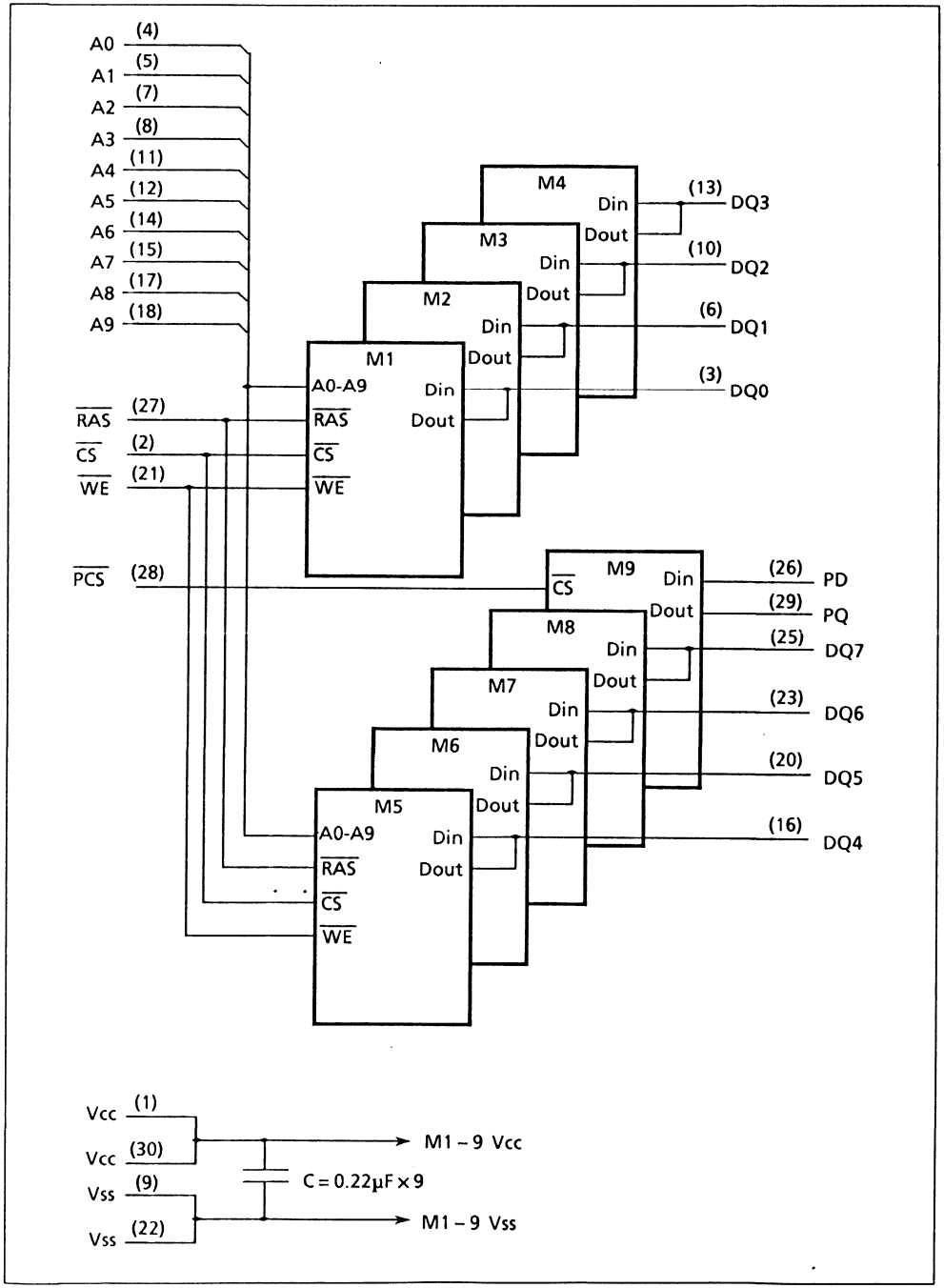


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCS}$
14	A6	29	PD
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{PCS}$	Parity chip select
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
PD	Data-in for parity
PQ	Data-out for parity
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	9.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56C19A/AT/B								
		-8A		-10A		-12A				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	630	—	540	—	450	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	18	—	18	—	18	mA	TTL interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z	
		—	9	—	9	—	9	mA	CMOS interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC}–0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	540	—	450	—	405	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	45	—	45	—	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IL} Dout = enable	1
$\overline{CS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	540	—	450	—	360	mA	t_{RC} = min	
Static column mode current	I_{CC9}	—	540	—	450	—	360	mA	Static column mode t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	60	pF	1
Input capacitance (Clock)	C_{I2}	—	75	pF	1, 2
Input/output capacitance (DQ0 – DQ7)	$C_{I/O}$	—	17	pF	1, 2
Input capacitance (PD)	C_{I3}	—	10	pF	1
Output capacitance (PQ)	C_O	—	12	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout.

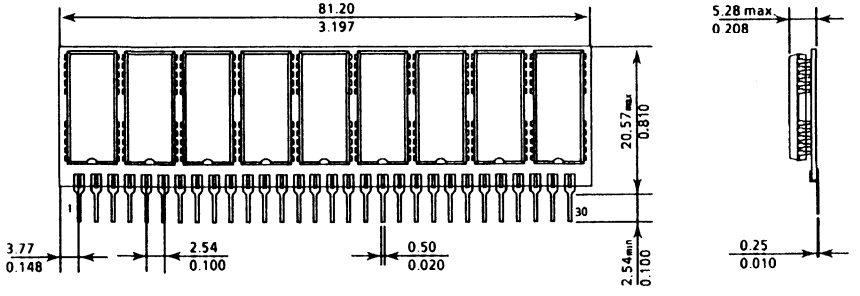
AC Characteristics

Refer to the HM511002A data sheet for AC characteristics. The HB56C19 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

Physical Outline

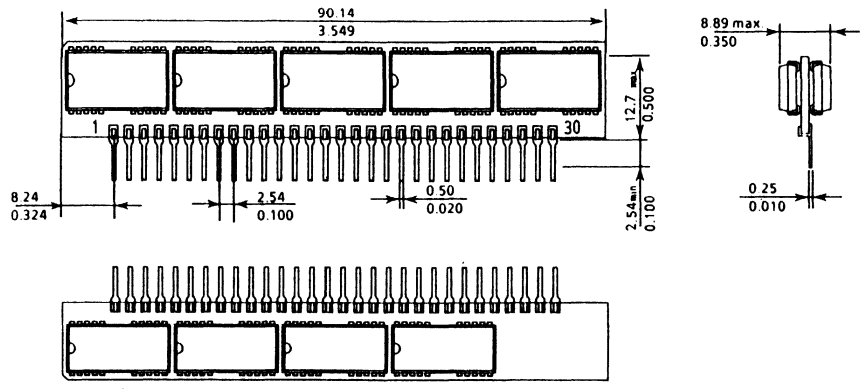
Unit: mm/inch

HB56C19A series



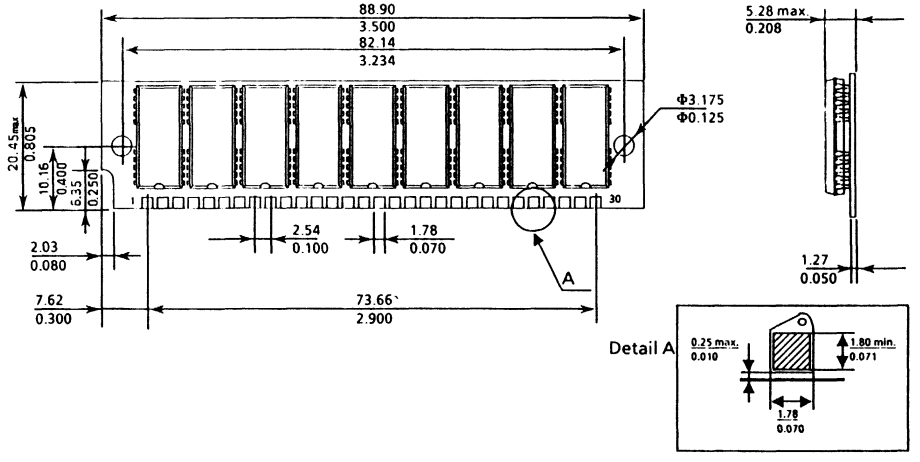
Unit: mm/inch

HB56C19AT series



Unit: mm/inch

HB56C19B series



Note: The plating of the contact finger is solder coat.

HB56C18 Series

1,048,576-Word × 8-Bit High Density Dynamic RAM Module

The HB56C18 is a 1M × 8 static column mode dynamic RAM module, mounted eight 1-Mbit DRAM (HM511002JP) sealed in SOJ package. An outline of the HB56C18 is 30-pin single in-line package having lead types (HB56C18A, HB56C18AT), socket type (HB56C18B). Therefore, the HB56C18 makes high density mounting possible without surface mount technology. The HB56C18 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

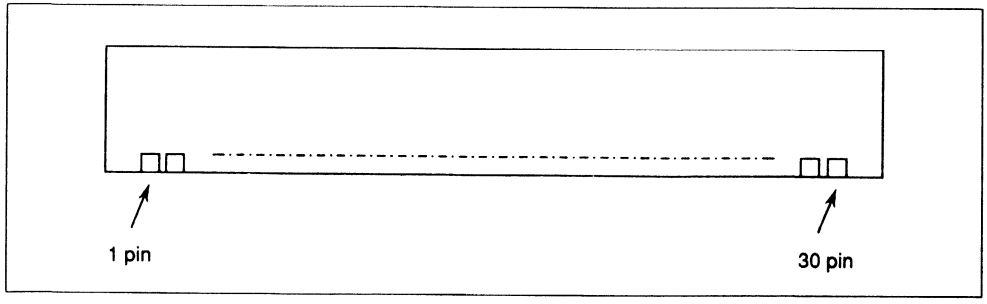
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time: 80 ns/100 ns/120 ns (max)
- Low power dissipation
  - Active mode: 3080 mW/2640 mW/2200 mW (max)
  - Standby mode: 88 mW (max)
- Static column mode capability
- 512 refresh cycle/8 ms
- 2 variations of refresh
  - $\overline{RAS}$-only refresh
  - $\overline{CS}$-before-$\overline{RAS}$ refresh
- TTL compatible

Ordering Information

	Package		
Access time	**30-pin SIP Lead type**	**30-pin SIP Low Profile Lead type**	**30-pin SIP Socket type**
80 ns	HB56C18A-8A	HB56C18AT-8A	HB56C18B-8A
100 ns	HB56C18A-10A	HB56C18AT-10A	HB56C18B-10A
120 ns	HB56C18A-12A	HB56C18AT-12A	HB56C18B-12A

Pin Arrangement

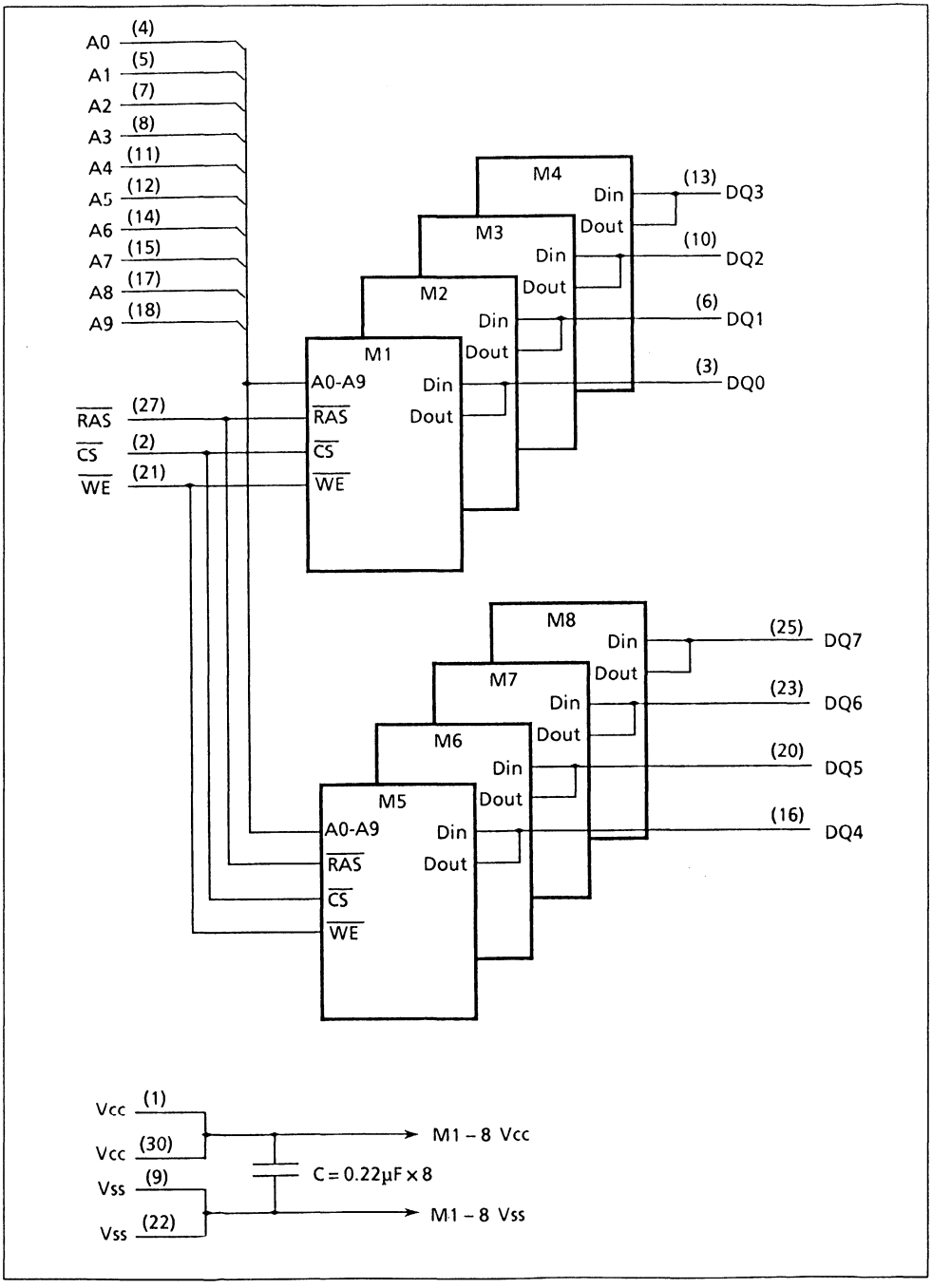


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CS}$	17	A8
3	DQ0	18	A9
4	A0	19	NC
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	NC
12	A5	27	$\overline{RAS}$
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A8	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CS}$	Chip select
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	8.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Condtions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56C18A/AT/B								
		-8A		-10A		-12A				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	560	—	480	—	400	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—	16	mA	TTL interface $\overline{RAS}$, $\overline{CS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CS}$ ≥ V_{CC}–0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	480	—	400	—	360	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IL} Dout = enable	1
$\overline{CS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	480	—	400	—	320	mA	t_{RC} = min	
Static column mode current	I_{CC9}	—	480	—	400	—	320	mA	Static column mode t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	55	pF	1
Input capacitance (Clock)	C_{I2}	—	70	pF	1, 2
Input/output capacitance (DQ0 – DQ7)	$C_{I/O}$	—	17	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CS}$ = V_{IH} to disable Dout.

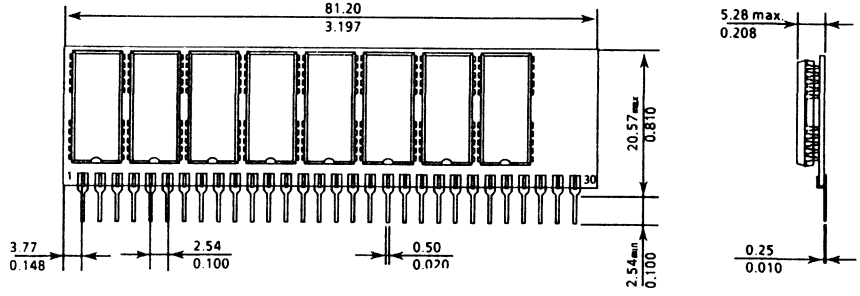
AC Characteristics

Refer to the HM511002A data sheet for AC characteristics. The HB56C18 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

Physical Outline

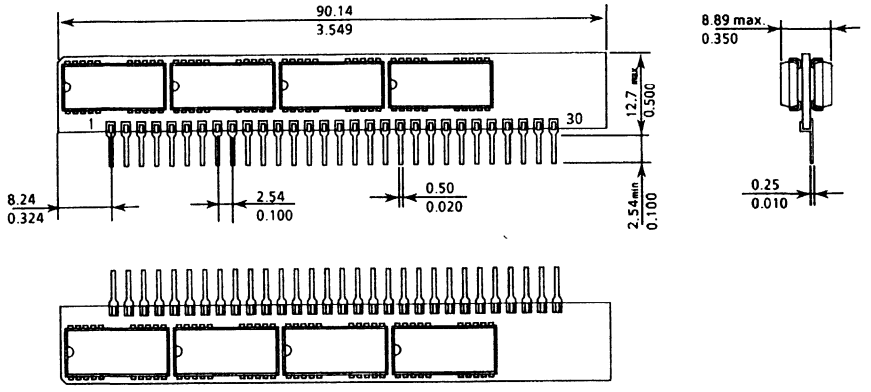
Unit: mm/inch

HB56C18A series



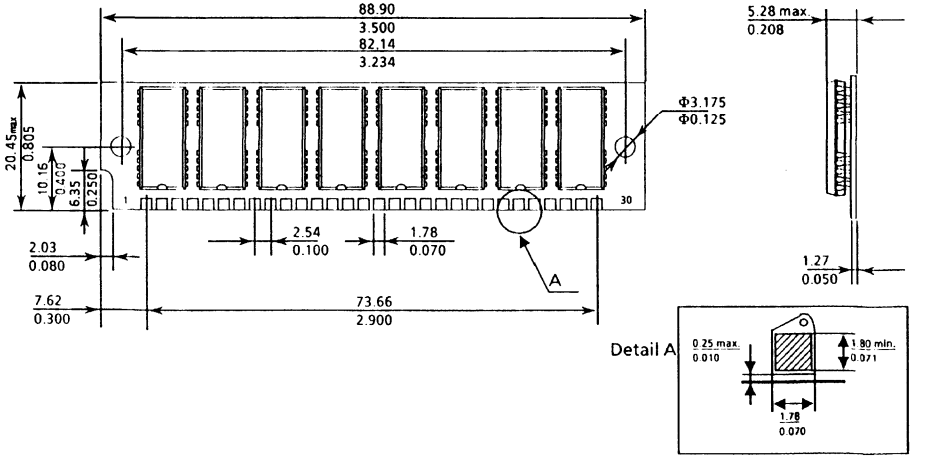
Unit: mm/inch

HB56C18AT series



Unit: mm/inch

HB56C18B series



Note: The plating of the contact finger is solder coat.

HB56D136 Series

1,048,576-Word × 36-Bit High Density Dynamic RAM Module

The HB56D136 is a 1M × 36 dynamic RAM module, mounted 8 pieces of 4-Mbit DRAM (HM514400JP) sealed in SOJ package and 4 peices of 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56D136 is 72-pin single in-line package. Therefore, the HB56D136 makes high density mounting possible without surface mount technology. The HB56D136 provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ.

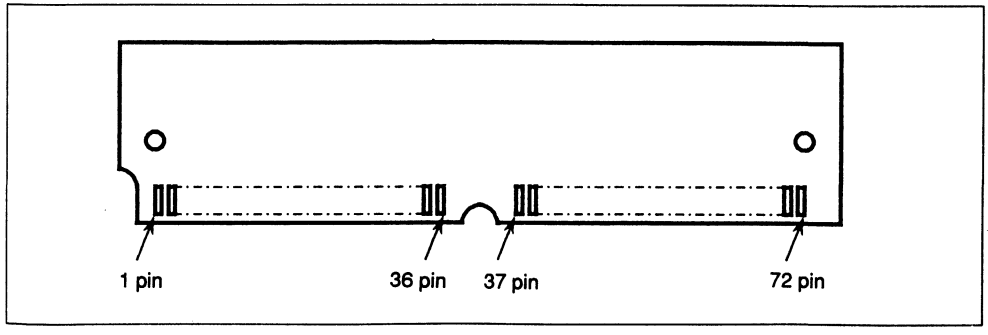
Ordering Information

Type No.	Access time	Package
HB56D136B-8	80 ns	72-pin SIP socket type
HB56D136B-10	100 ns	
HB56D136BR-8	80 ns	
HB56D136BR-10	100 ns	

Features

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: 80 ns/100 ns (max)
- Low power dissipation
  - Active mode: 5.25 W/4.62 W (max)
  - Standby mode: 126 mW (max)
- Fast page mode capability
- 1,024 refresh cycle/16 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	NC	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

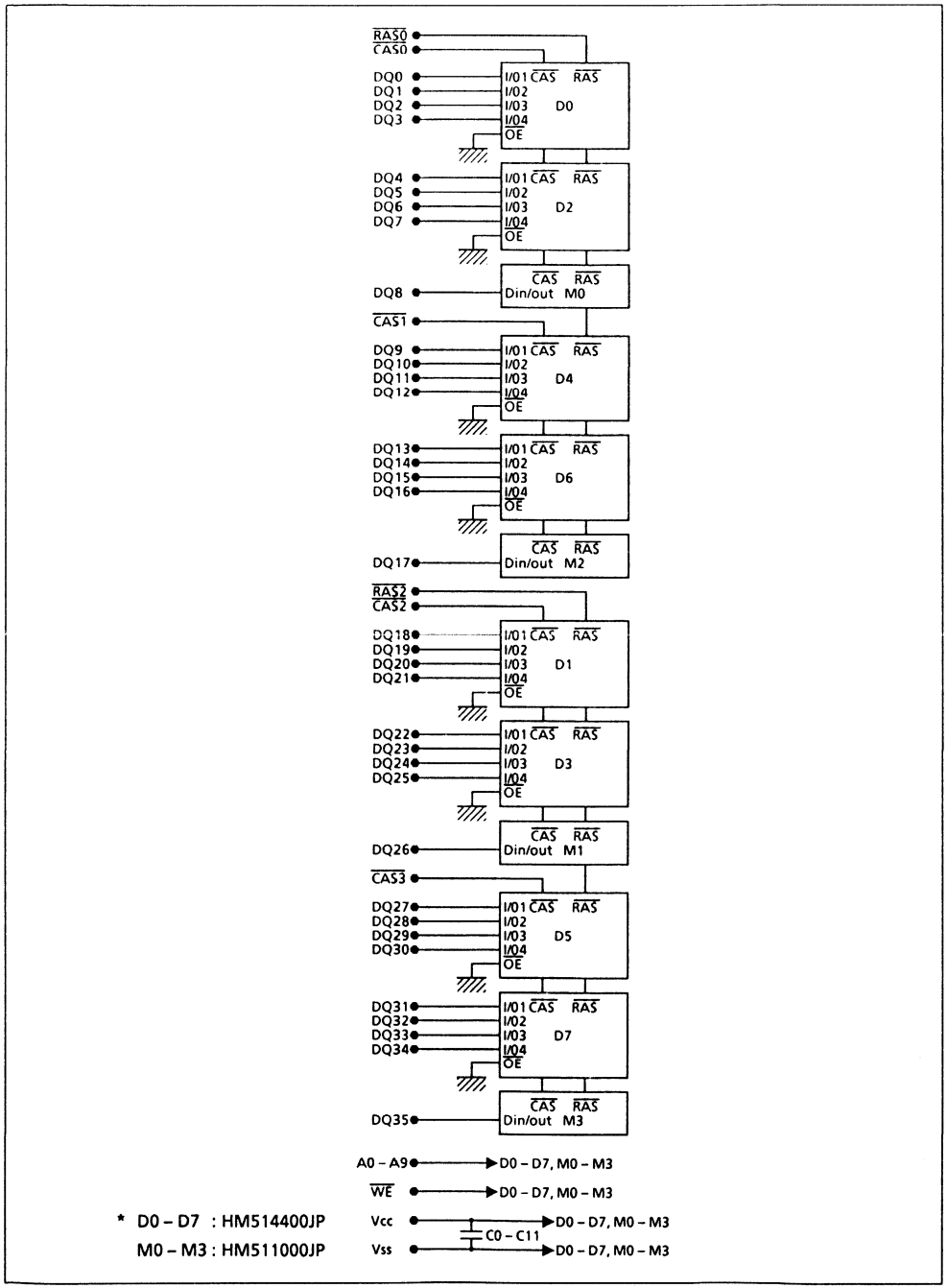
Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
DQ0 – DQ35	Data-in/data out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56D136B/BR	
Pin No.	Pin name	80 ns	100 ns
67	PD1	V_{SS}	V_{SS}
68	PD2	V_{SS}	V_{SS}
69	PD3	NC	V_{SS}
70	PD4	V_{SS}	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Input	Vin	–1.0 to +7.0	V
	Output	Vout	–1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	–1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	12	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	88	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	104	pF	1
Input capacitance ($\overline{RAS}$)	C_{I3}	—	57	pF	1
Input capacitance ($\overline{CAS}$)	C_{I4}	—	36	pF	1
Output capacitance (DQ0 – DQ7, DQ9 – DQ16 DQ18 – DQ25, DQ27 – DQ34)	$C_{I/O1}$	—	17	pF	1, 2
Output capacitance (DQ8, DQ17, DQ26, DQ35)	$C_{I/O2}$	—	22	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56D136B/BR-8		HB56D136B/BR-10				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	1000	—	880	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	24	—	24	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	12	—	12	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	960	—	840	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	60	—	60	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	960	—	840	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	920	—	840	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V) *1, *12

Read, Write and Refresh Cycle (Common parameters)

		HB56D136B/BR-8		HB56D136B/BR-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	160	—	190	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	25	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	20	—	20	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	75	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	55	ns	9
$\overline{RAS}$ hold time	t_{RSH}	25	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	ms	15

Read Cycle

		HB56D136B/BR-8		HB56D136B/BR-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 3
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	25	ns	3, 4
Access time from address	t_{AA}	—	40	—	45	ns	3, 5
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	

Read Cycle (cont)

Parameter	Symbol	HB56D136B/BR-8		HB56D136B/BR-10		Unit	Notes
		Min	Max	Min	Max		
Read command hold time to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF}	0	20	0	25	ns	6

Write Cycle

Parameter	Symbol	HB56D136B/BR-8		HB56D136B/BR-10		Unit	Notes
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	ns	10
Write command hold time	t_{WCH}	20	—	25	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	11
Data-in hold time	t_{DH}	20	—	20	—	ns	11

Refresh Cycle

Parameter	Symbol	HB56D136B/BR-8		HB56D136B/BR-10		Unit	Notes
		Min	Max	Min	Max		
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh cycle)	t_{CHR}	20	—	20	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	15	—	15	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	HB56D136B/BR-8		HB56D136B/BR-10		Unit	Notes
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	55	—	55	—	ns	
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	15	—	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASC}	80	100000	100	100000	ns	13
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	50	—	50	ns	14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	50	—	50	—	ns	

Notes:
1. AC measurements assume t_T = 5 ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max).
5. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max).
6. t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
10. Early write cycle only ($t_{WCS} \geq t_{WCS}$ (min)).
11. These parameters are referenced to $\overline{CAS}$ leading edge in an early write cycle.
12. An initial pause of 100 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh).
13. t_{RASC} is determined by $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{ACP}.
15. t_{REF} is determined by 1,024 refresh cycles.

Timing Waveforms

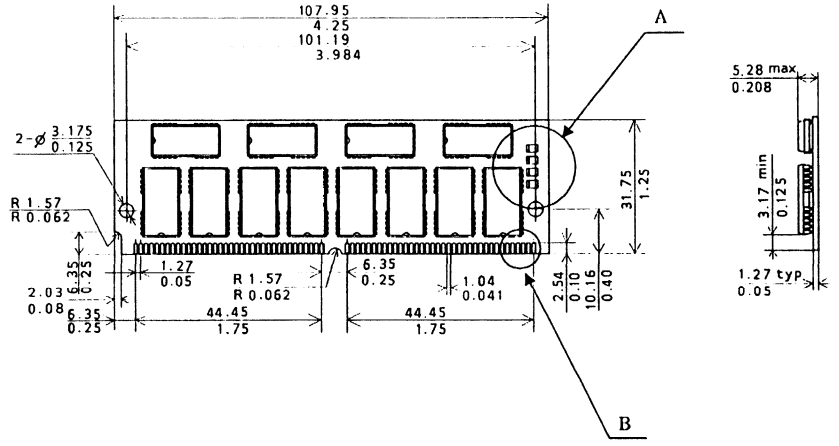
Refer to the HB56D25609 data sheet.

For HB56D136B series, $\overline{WE}$ = V_{IH} in $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

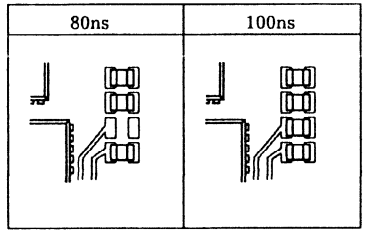
Physical Outline

Unit: mm/inch

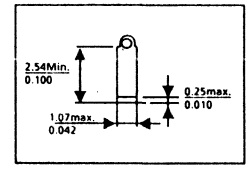
HB56D136B series



Detail A

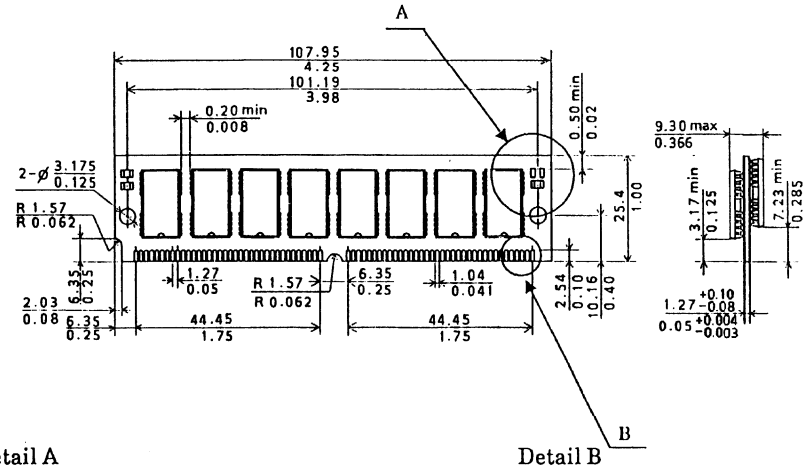


Detail B



Note: The plating of the contact finger is gold.

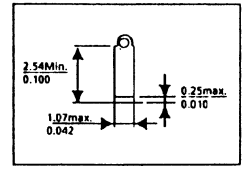
HB56D136BR series



Detail A

80ns	100ns
	

Detail B



Note : The plating of the contact finger is gold.

HB56D236B Series

2,097,152-Word × 36-Bit High Density Dynamic RAM Module

The HB56D236B is a 2M × 36 dynamic RAM module, mounted 16 pieces of 4-Mbit DRAM (HM514400JP) sealed in SOJ package and 8 pieces of 1-Mbit DRAM (HM511000JP) sealed in SOJ package. An outline of the HB56D236B is 72-pin single in-line package. Therefore, the HB56D236B makes high density mounting possible without surface mount technology. The HB56D236B provides common data inputs and outputs. Decoupling capacitors are mounted beneath each SOJ but only on the one side of its module board.

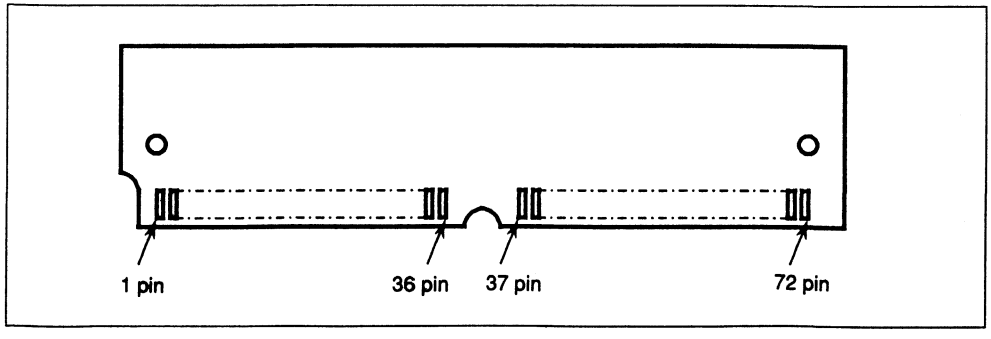
Ordering Information

Type No	Access time	Package
HB56D236B-8	80 ns	72-pin SIP socket type
HB56D236B-10	100 ns	

Features

- 72-pin single in-line package
  - Lead pitch: 1.27 mm
- Single 5 V (± 5%) supply
- High speed
  - Access time: 80 ns/100 ns (max)
- Low power dissipation
  - Active mode: 5.57 W/4.94 W (max)
  - Standby mode: 252 mW (max)
- Fast page mode capability
- 1,024 refresh cycle/16 ms
- 2 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
- TTL compatible

Pin Arrangement



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	19	NC	37	DQ17	55	DQ12
2	DQ0	20	DQ4	38	DQ35	56	DQ30
3	DQ18	21	DQ22	39	V_{SS}	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	V_{CC}
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	$\overline{RAS1}$	63	DQ15
10	V_{CC}	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{WE}$	65	DQ16
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	PD1
14	A2	32	A9	50	DQ27	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ10	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	PD4
17	A5	35	DQ26	53	DQ11	71	NC
18	A6	36	DQ8	54	DQ29	72	V_{SS}

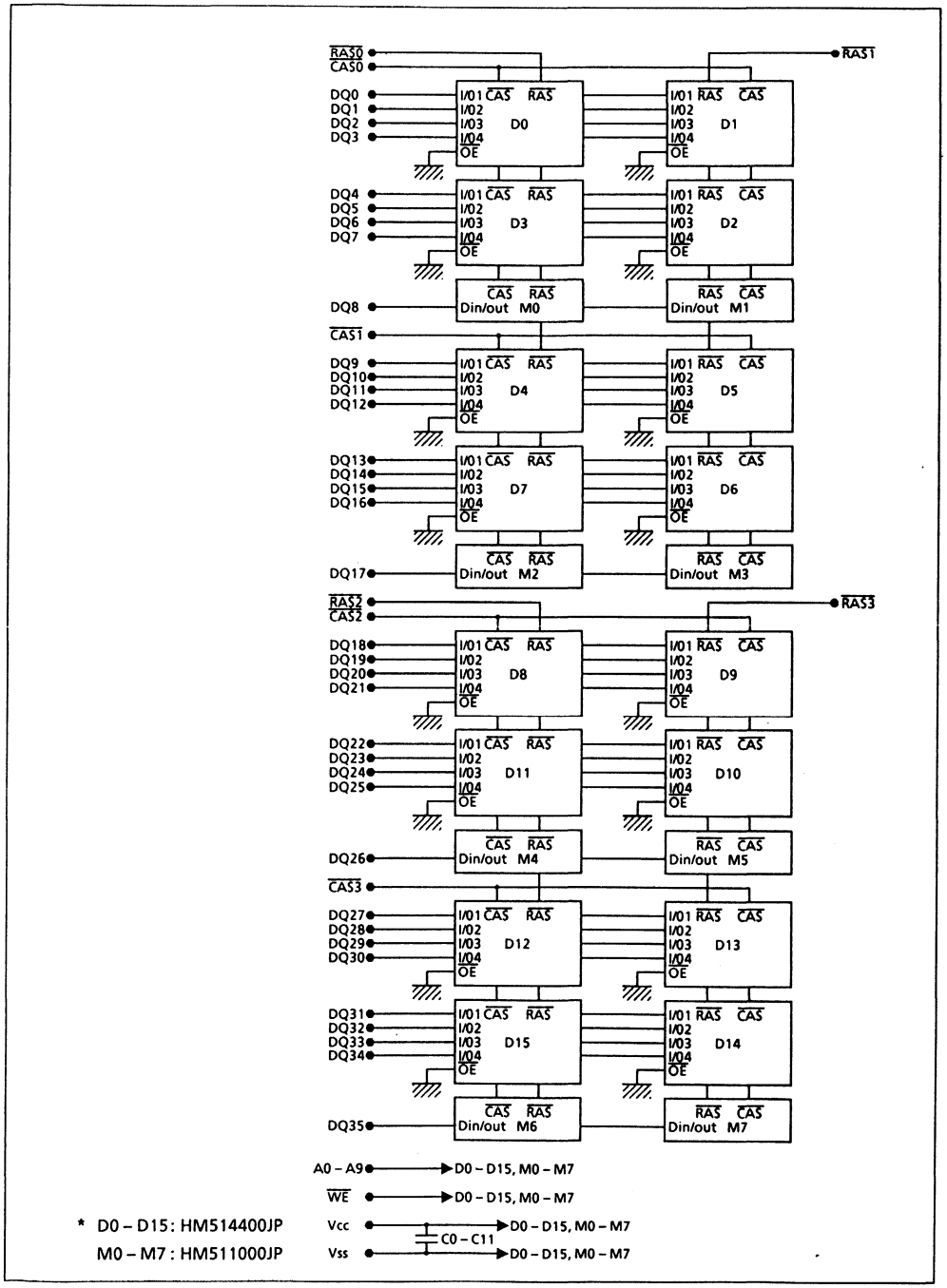
Pin Description

Pin name	Function
A0 – A9	Address input
A0 – A9	Refresh address input
DQ0 – DQ35	Data-in/data out
$\overline{CAS0}$ – $\overline{CAS3}$	Column address strobe
$\overline{RAS0}$ – $\overline{RAS3}$	Row address strobe
$\overline{WE}$	Read/write enable
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
PD1 – PD4	Presence detect pin
NC	No connection

Presence Detect Pin Arrangement

		HB56D236B	
Pin No	Pin name	80 ns	100 ns
67	PD1	NC	NC
68	PD2	NC	NC
69	PD3	NC	V_{SS}
70	PD4	V_{SS}	V_{SS}

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	Input	Vin	–1.0 to +7.0	V
	Output	Vout	–1.0 to +7.0	V
Supply voltage relative to V_{SS}		V_{CC}	–1.0 to +7.0	V
Short circuit output current		Iout	50	mA
Power dissipation		P_T	12	W
Operating temperature		Topr	0 to +70	°C
Storage temperature		Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.75	5.0	5.25	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 5%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	161	pF	1
Input capacitance ($\overline{WE}$)	C_{I2}	—	193	pF	1
Input capacitance ($\overline{RAS}$, $\overline{CAS}$)	C_{I3}	—	62	pF	1
Output capacitance (DQ0 – DQ7, DQ9 – DQ16 DQ18 – DQ25, DQ27 – DQ34)	$C_{I/O1}$	—	29	pF	1,2
Output capacitance (DQ8, DQ17, DQ26, DQ35)	$C_{I/O2}$	—	39	pF	1,2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

		HB56D236B-8		HB56D236B-10				
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**	**Notes**
Operating current	I_{CC1}	—	1060	—	940	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	48	—	48	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	24	—	24	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	1020	—	900	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	120	—	120	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	1020	—	900	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	980	—	900	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 4.2 mA	

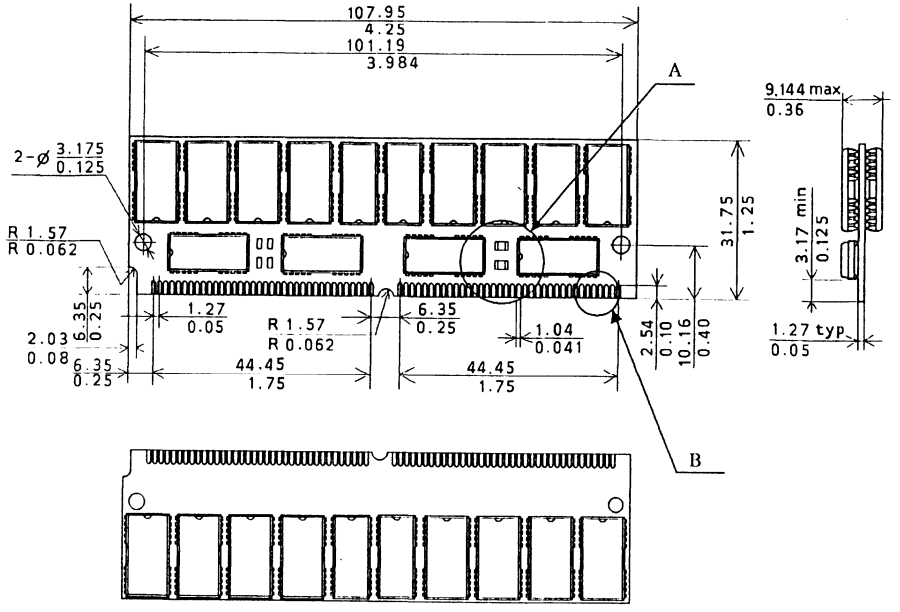
Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC Characteristics

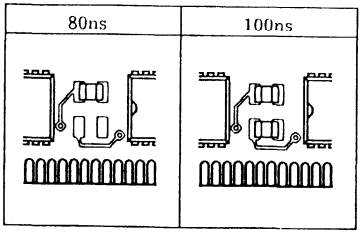
Refer to the HB56D136 data sheet.

Physical Outline

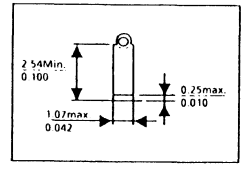
Unit: mm/inch



Detail A



Detail B



Note: The plating of the contact finger is gold.

HB56A49 Series

4,194,304-Word × 9-Bit High Density Dynamic RAM Module

The HB56A49 is a 4M × 9 dynamic RAM module, mounted nine 4-Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A49 is 30-pin single in-line package having lead types (HB56A49A, HB56A49AT), socket type (HB56A49B). Therefore, the HB56A49 makes high density mounting possible without surface mount technology. The HB56A49 provides common data inputs and outputs and also provides separate I/O on parity bit for parity check. Its module board has decoupling capacitors beneath the each SOJ.

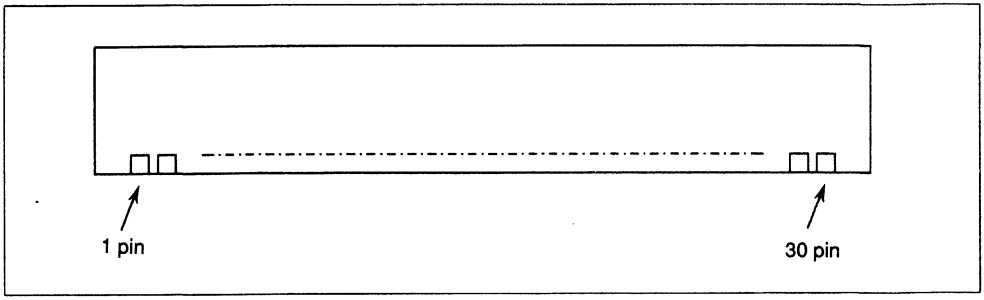
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time: 80 ns/100 ns (max)
- Low power dissipation
  - Active mode: 4455 mW/3960 mW (max)
  - Standby mode: 99 mW (max)
- Fast page mode capability
- 1,024 refresh cycle/16 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

	Package		
Access time	**30-pin SIP Lead type**	**30-pin SIP Low Profile Lead type**	**30-pin SIP Socket type**
80 ns	HB56A49A-8	HB56A49AT-8	HB56A49B-8
100 ns	HB56A49A-10	HB56A49AT-10	HB56A49B-10

Pin Arrangement

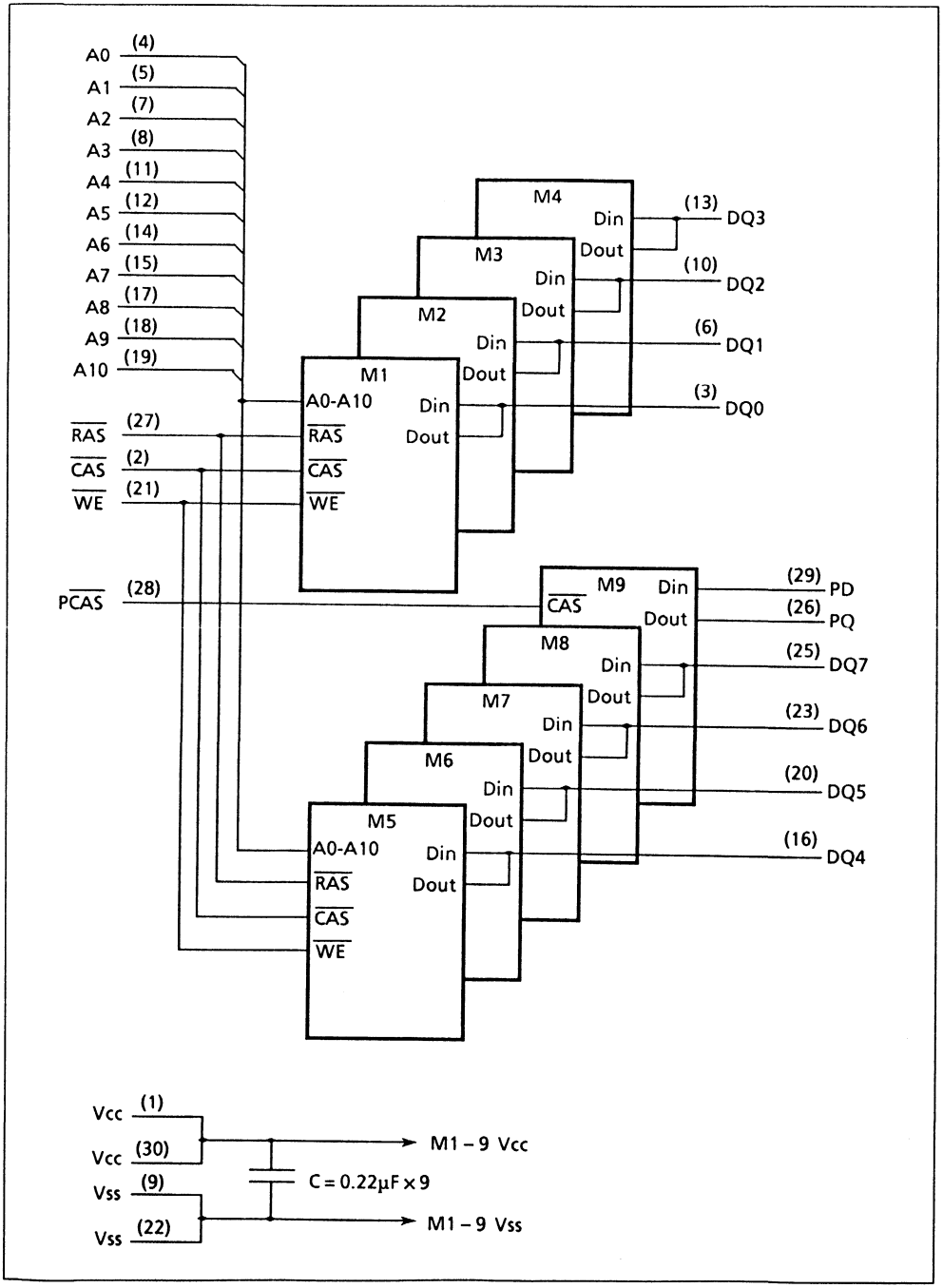


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	PQ
12	A5	27	$\overline{RAS}$
13	DQ3	28	$\overline{PCAS}$
14	A6	29	PD
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A9	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$, $\overline{PCAS}$	Column address strobe
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
PD	Data-in for parity
PQ	Data-out for parity
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	9	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	–1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56A49A/AT/B						
		-8		-10				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	810	—	720	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	18	—	18	mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	9	—	9	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	810	—	720	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	45	—	45	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	810	—	720	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	810	—	720	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current Dout = disable	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	70	pF	1
Input capacitance (Clock)	C_{I2}	—	88	pF	1
Input/output capacitance (DQ0 – DQ7)	$C_{I/O}$	—	30	pF	1,2
Input capacitance (PD)	C_{I3}	—	20	pF	1
Output capacitance (PQ)	C_O	—	20	pF	1,2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

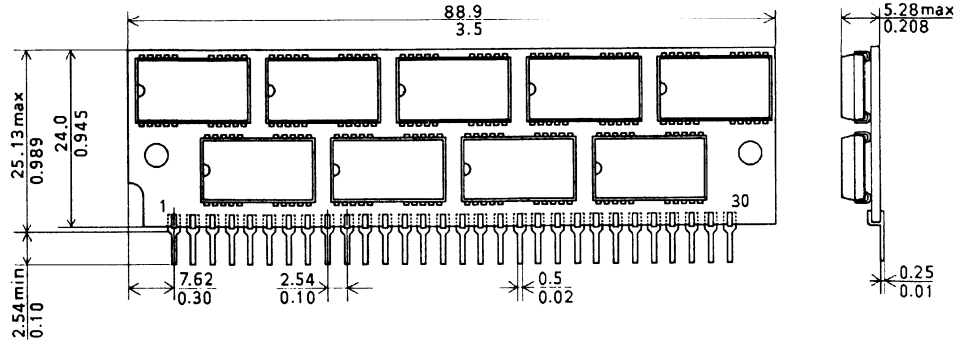
AC Characteristics

Refer to the HM514100 data sheet for AC characteristics. The HB56A49 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

Physical Outline

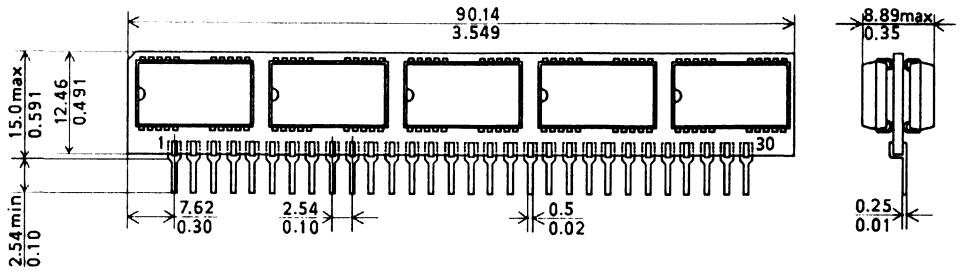
Unit: mm/inch

HB56A49A series



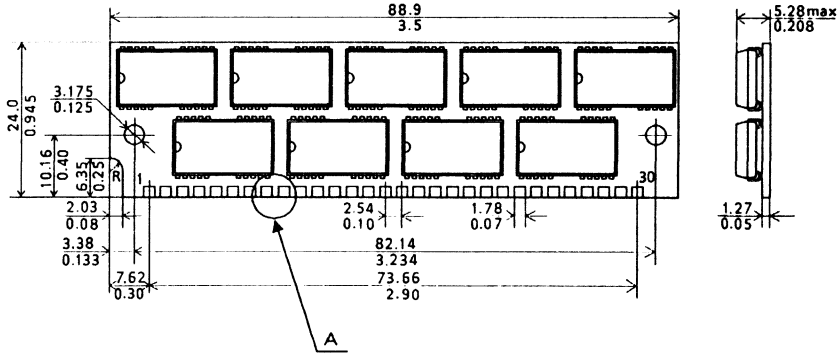
Unit: mm/inch

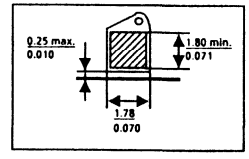
HB56A49AT series



Unit: mm/inch

HB56A49B series





Detail A

Note: The plating of the contact finger is solder coat.

HB56A48 Series

4,194,304-Word × 8-Bit High Density Dynamic RAM Module

The HB56A48 is a 4M × 8 dynamic RAM module, mounted eight 4-Mbit DRAM (HM514100JP) sealed in SOJ package. An outline of the HB56A48 is 30-pin single in-line package having lead types (HB56A48A, HB56A48AT), socket type (HB56A48B). Therefore, the HB56A48 makes high density mounting possible without surface mount technology. The HB56A48 provides common data inputs and outputs. Its module board has decoupling capacitors beneath the each SOJ.

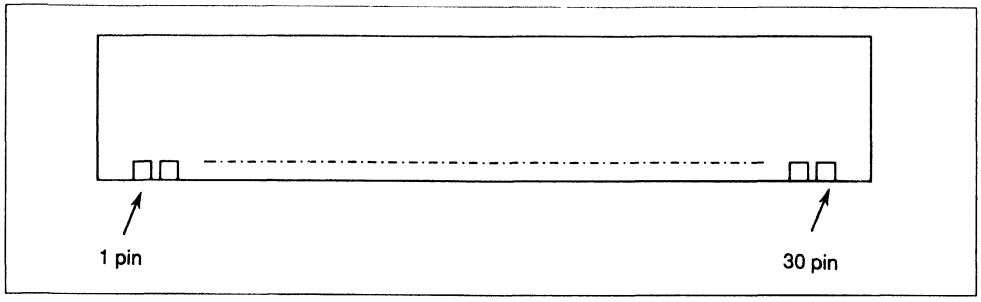
Features

- 30-pin single in-line package
  - Lead pitch: 2.54 mm
- Single 5 V (± 10%) supply
- High speed
  - Access time: 80 ns/100 ns (max)
- Low power dissipation
  - Active mode: 3.96 W/3.52 W (max)
  - Standby mode: 88 mW (max)
- Fast page mode capability
- 1,024 refresh cycle/16 ms
- 3 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
- TTL compatible

Ordering Information

	Package		
Access time	**30-pin SIP Lead type**	**30-pin SIP Low Profile Lead type**	**30-pin SIP Socket type**
80 ns	HB56A48A-8	HB56A48AT-8	HB56A48B-8
100 ns	HB56A48A-10	HB56A48AT-10	HB56A48B-10

Pin Arrangement

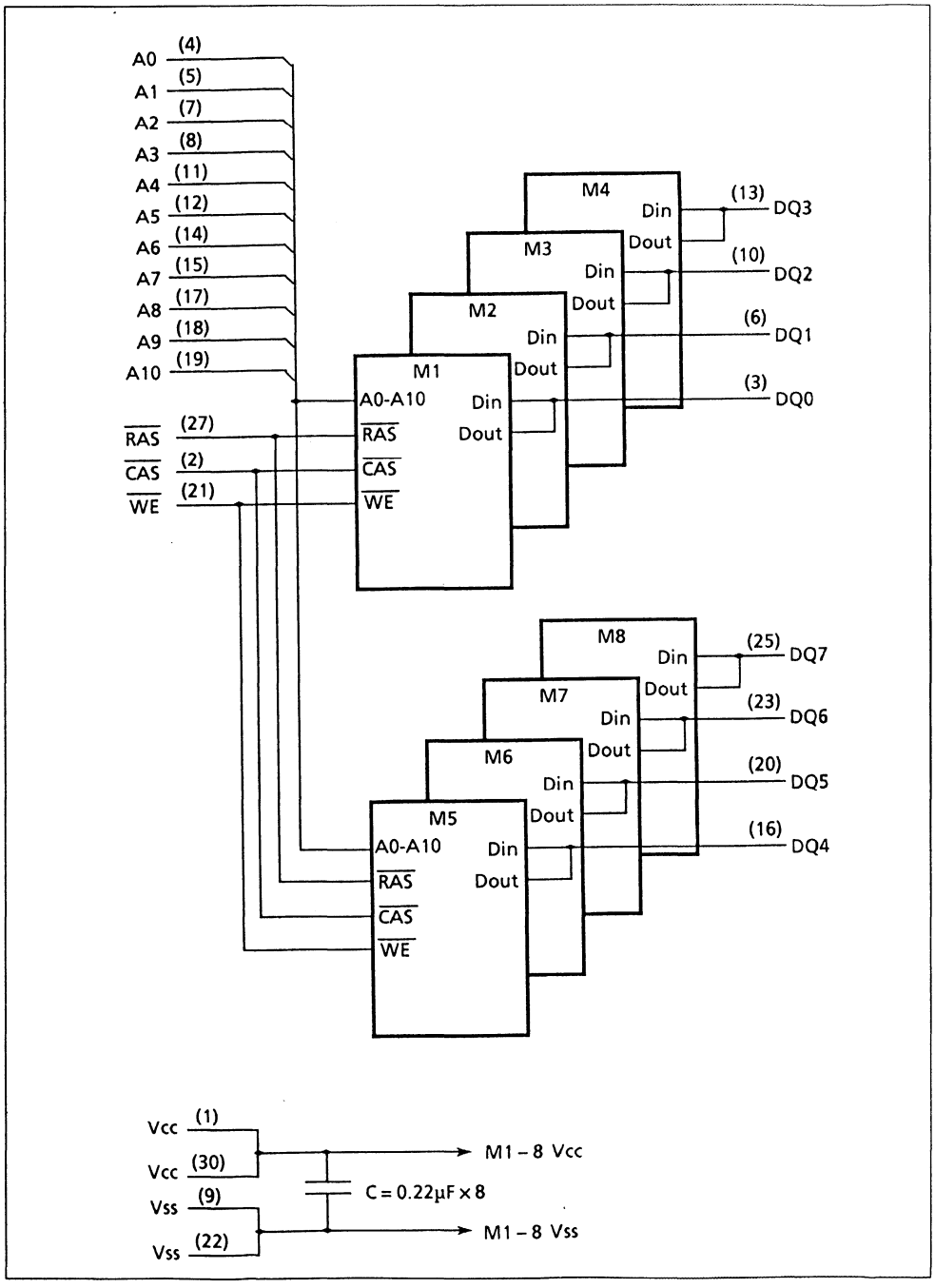


Pin No.	Pin name	Pin No.	Pin name
1	V_{CC}	16	DQ4
2	$\overline{CAS}$	17	A8
3	DQ0	18	A9
4	A0	19	A10
5	A1	20	DQ5
6	DQ1	21	$\overline{WE}$
7	A2	22	V_{SS}
8	A3	23	DQ6
9	V_{SS}	24	NC
10	DQ2	25	DQ7
11	A4	26	NC
12	A5	27	$\overline{RAS}$
13	DQ3	28	NC
14	A6	29	NC
15	A7	30	V_{CC}

Pin Description

Pin name	Function
A0 – A10	Address input
A0 – A9	Refresh address input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Read/write enable
DQ0 – DQ7	Data-in/data-out
V_{CC}	Power supply (+5 V)
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	−1.0 to +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	8	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	5.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

		HB56A48A/AT/B						
		-8		-10				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions	Notes
Operating current	I_{CC1}	—	720	—	640	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	16	—	16	—mA	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = High-Z	
		—	8	—	8	mA	CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	720	—	640	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	40	—	40	mA	$\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	720	—	640	mA	t_{RC} = min	
Page mode current	I_{CC7}	—	720	—	640	mA	t_{PC} = min	1, 3
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	Iout = –5 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Iout = 4.2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	65	pF	1
Input capacitance (Clock)	C_{I2}	—	81	pF	1
Input/output capacitance (DQ0 – DQ7)	$C_{I/O}$	—	30	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

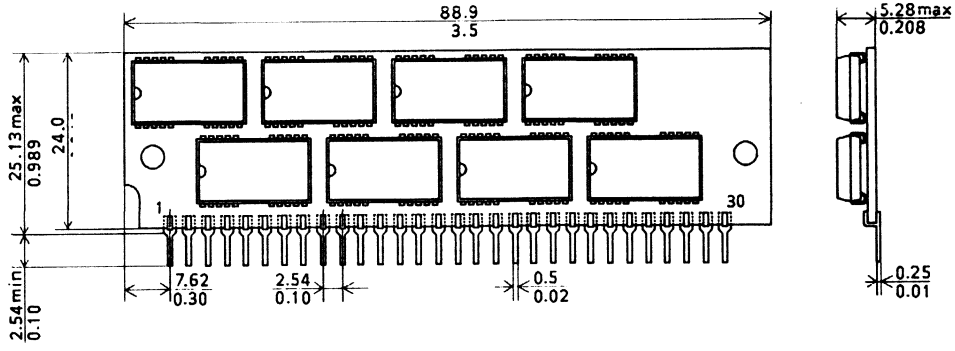
AC Characteristics

Refer to the HM514100 data sheet for AC characteristics. The HB56A48 writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)). Delayed write cycle is not available because of I/O common.

Physical Outline

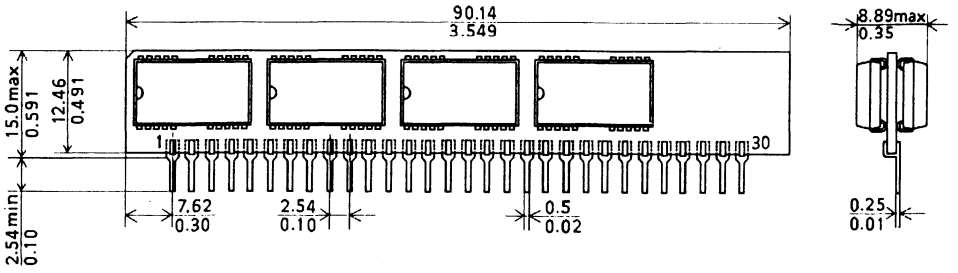
Unit: mm/inch

HB56A48A series



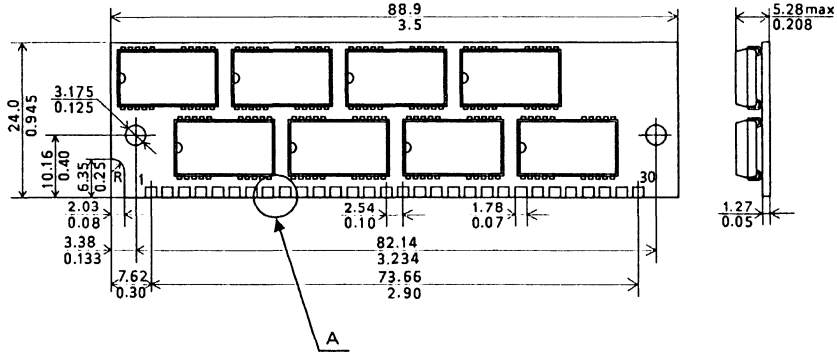
Unit: mm/inch

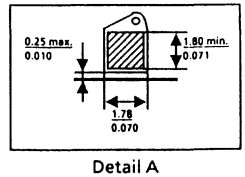
HB56A48AT series



Unit: mm/inch

HB56A48B series





Detail A

Note: The plating of the contact finger is solder coat.

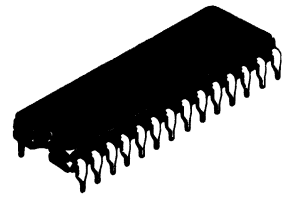
MOS MASK ROM

HN623257P Series
HN623257F Series

32768-word x 8-bit CMOS Mask Programmable Read Only Memory

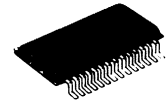
The HN623257P/F is a 256-kbit CMOS mask-programmable ROM organized as 32768 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

HN623257P



(DP-28)

HN623257F

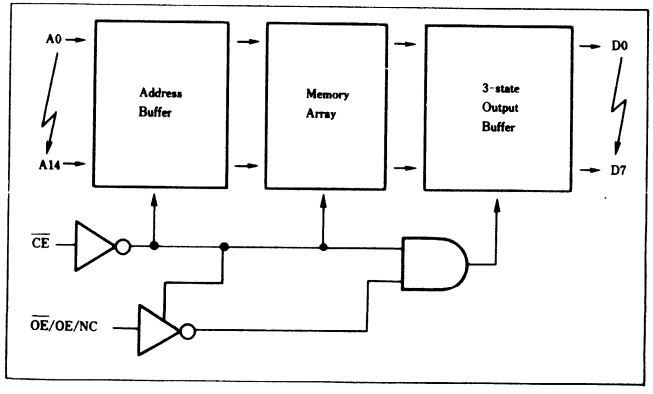


(FP-28DA)

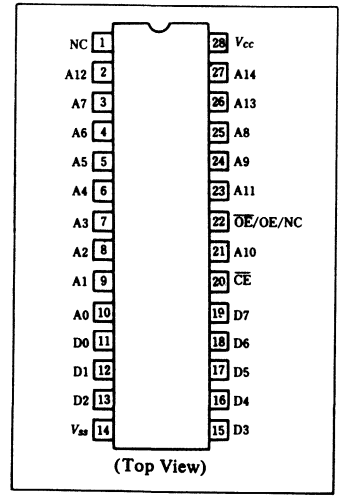
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Address Access Time: 150ns (Max.)
- Low Power Consumption: 100mW (typ.) active
  5μW (typ.) standby
- Byte-Wide Data Organization

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage *1	Vcc	−0.3 to +7.0	V
All Input or Output Voltage *1	V_T	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	−20 to +75	℃
Storage Temperature Range	Tstg	−55 to +125	℃
Temperature Under Bias	Tbias	−20 to +85	℃

Note) *1. With respect to Vss.

Recommended Operating Conditions (V_{SS} = 0V, Ta = -20 to +75°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
	V_{IL}	−0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = -20 to +75°C)

Parameter		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	45	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
	Standby	I_{SB}	—	30	μA	V_{CC}=5.5V, $\overline{CE} \geqq V_{CC}-0.2V$
Input Leakage Current		$\|I_{LI}\|$	—	10	μA	Vin=0 to Vcc
Output Leakage Current		$\|I_{LI}\|$	—	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	$I_{OH}=-205\mu A$
		V_{OL}	—	0.4	V	I_{OL}=3.2mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Parameter	Symbol	min	max	Unit
Input Capacitance	Cin	—	10	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics

(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = -20 to +75°C)

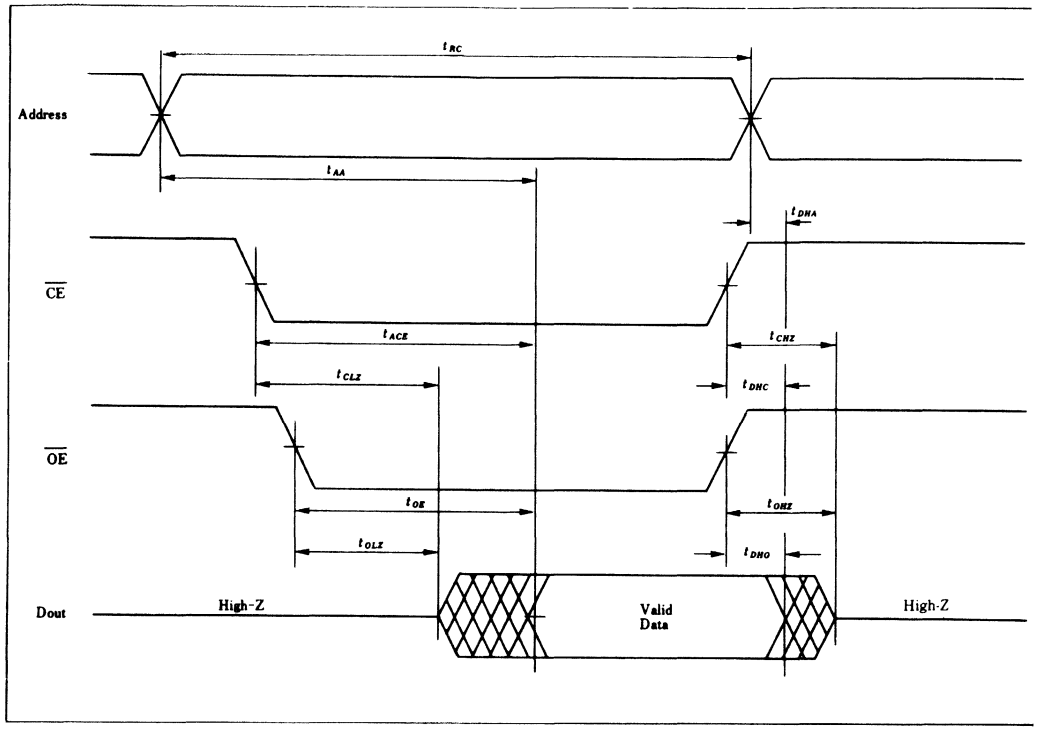
Test Condition

- Input Pulse Level ..... 0.8 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load ..... 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	150	—	ns
Address Access Time	t_{AA}	—	150	ns
$\overline{CE}$ Access Time	t_{ACE}	—	150	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
$\overline{CE}$ to Output in High Z*1	t_{CHZ}	—	70	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
$\overline{OE}$ Access Time	t_{OE}	—	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{OE}$ to Output in High Z*1	t_{OHZ}	—	70	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns

Note) *1. t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Diagram



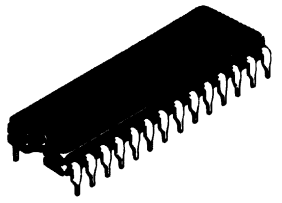
Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA}, t_{DHC} or t_{DHO}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA}, t_{ACE} or t_{OE}, whichever occurs last.
3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ}, whichever occurs last.

HN623257PZ Series
HN623257FZ Series

32768-word x 8-bit CMOS Mask Programmable Read Only Memory

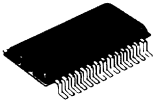
The HN623257PZ/FZ is a 256-kbit CMOS mask-programmable ROM organized as 32768 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

HN623257PZ



(DP-28)

HN623257FZ

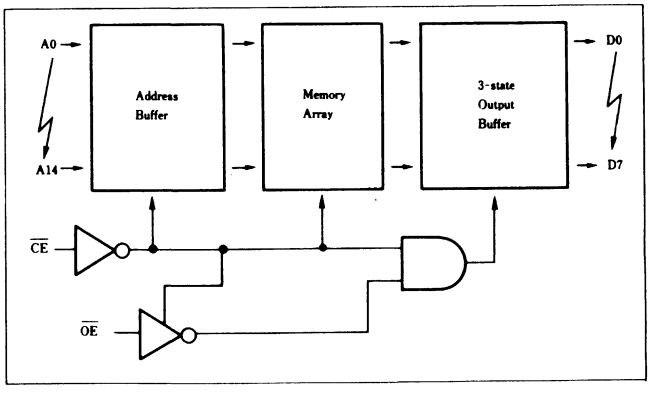


(FP-28DA)

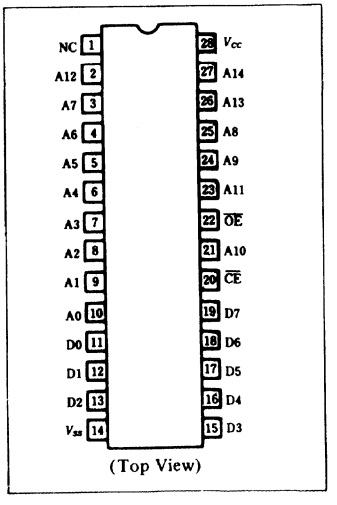
Features

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Address Access Time: 120ns (Max.)
- Low Power Consumption: 100mW (typ.) active
  5μW (typ.) standby
- Byte-Wide Data Organization

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power Supply Voltage *1	Vcc	−0.3 to +7.0	V
All Input or Output Voltage *1	VT	−0.3 to Vcc+0.3	V
Operating Temperature Range	Topr	−20 to +75	°C
Storage Temperature Range	Tstg	−55 to +125	°C
Temperature Under Bias	Tbias	−20 to +85	°C

Note) *1 With respect to Vss.

Recommended Operating Conditions (V_{SS} = 0V, Ta = –0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.4	—	V_{CC}+0.3	V
	V_{IL}	–0.3	—	0.6	V

DC Electrical Characteristics (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = –0 to +70°C)

Parameter		Symbol	min	max	Unit	Test Condition
Supply Current	Active	I_{CC}	—	50	mA	V_{CC}=5.5V, I_{DOUT}=0mA, t_{RC}=min
	Standby	I_{SB}	—	30	μA	V_{CC}=5.5V, $\overline{CE} \geq V_{CC}-0.2V$
Input Leakage Current		$\|I_{LI}\|$	—	10	μA	Vin=0 to Vcc
Output Leakage Current		$\|I_{LI}\|$	—	10	μA	$\overline{CE}$=2.2V, V_{OUT}=0 to V_{CC}
Output Voltage		V_{OH}	2.4	—	V	I_{OH}=–205μA
		V_{OL}	—	0.4	V	I_{OL}=3.2mA

Capacitance (V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 25°C, Vin = 0V, f = 1 MHz)

Parameter	Symbol	min	max	Unit
Input Capacitance	Cin	—	10	pF
Output Capacitance	Cout	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC Electrical Characteristics

(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = –20 to +75°C)

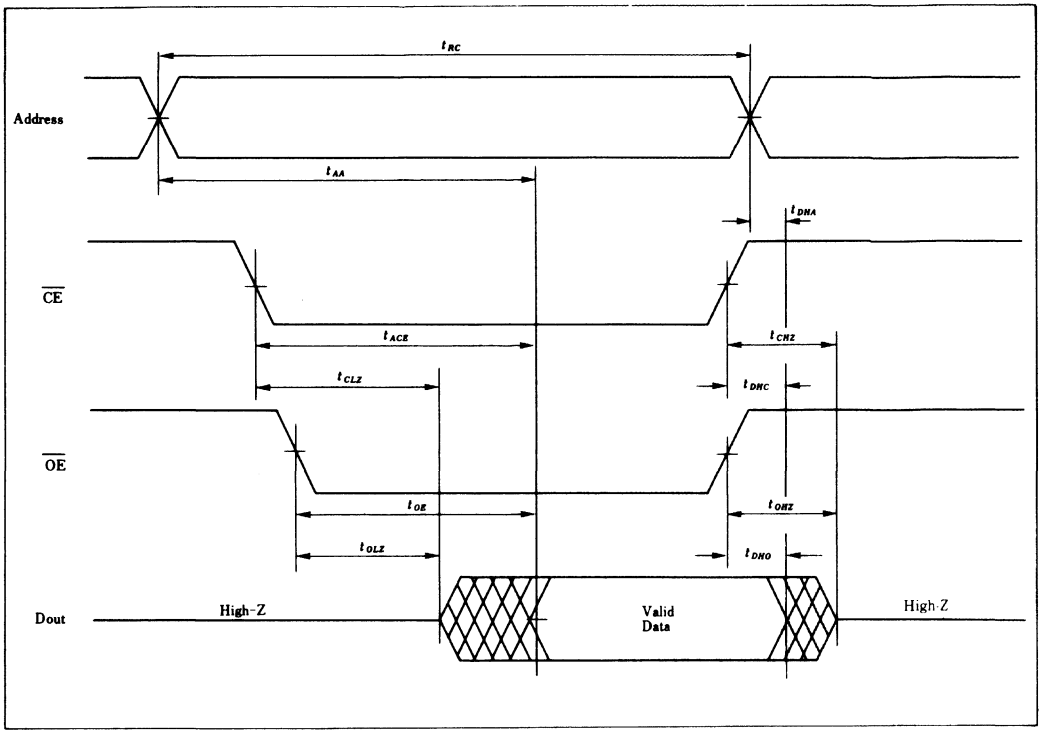
Test Condition

- Input Pulse Level ..... 0.6 to 2.4V
- Input and Output Timing Reference Level 1.5V
- Input Rise and Fall Time 10ns
- Output Load ..... 1 TTL gate + C_L = 100pF (including jig capacitance)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	120	—	ns
Address Access Time	t_{AA}	—	120	ns
$\overline{CE}$ Access Time	t_{ACE}	—	120	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
$\overline{CE}$ to Output in High Z*1	t_{CHZ}	—	60	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
$\overline{OE}$ Access Time	t_{OE}	—	70	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{OE}$ to Output in High Z*1	t_{OHZ}	—	60	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns

Note) *1. t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Diagram



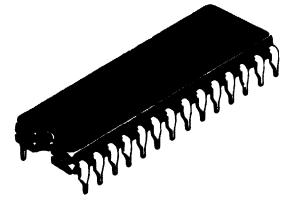
Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA}, t_{DHC} or t_{DHO}, whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA}, t_{ACE} or t_{OE}, whichever occurs last.
3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ}, whichever occurs last.

HN623258P Series
HN623258F Series

32768-Word × 8-Bit CMOS Mask Programmable ROM

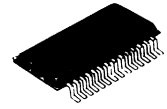
HN623258P/F is a 256-Kbit CMOS mask-programable ROM organized as 32768-word x 8-bit. It can be operated with a battery because of low power consumption.

HN623258P



(DP-28)

HN623258F

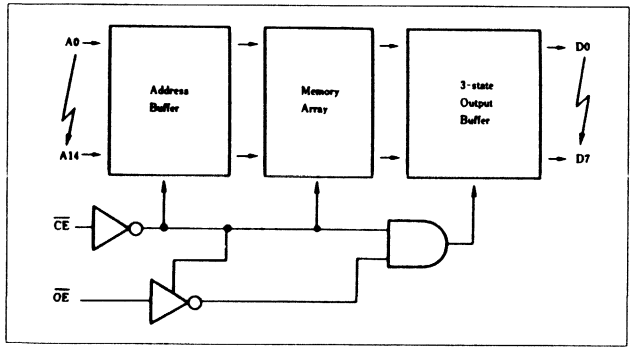


(FP-28DA)

Features

- Low power: Active 100 mW (typ), Standby 5 μW (typ)
- Address access time: 200 ns (max)
- Single 5 V
- TTL compatible
- Wired OR is permitted for the output in three states

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	Vcc	–0.3 to +7.0	V
Terminal voltage*1	VT	–0.3 to Vcc +0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

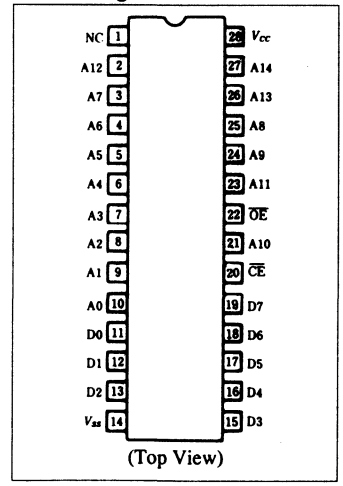
Note: *1. With respect to Vss.

Recommended Operating Conditions

(Vss = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	Vcc	4.5	5.0	5.5	V
Input voltage	VIH	2.2	—	Vcc + 0.3	V
	VIL	–0.3	—	0.8	V

Pin Arrangement



(Top View)

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	45	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current		$\|I_{LI}\|$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacity	Cin	—	10	pF
Output capacity	Cout	—	15	pF

Note: This parameter is samples and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

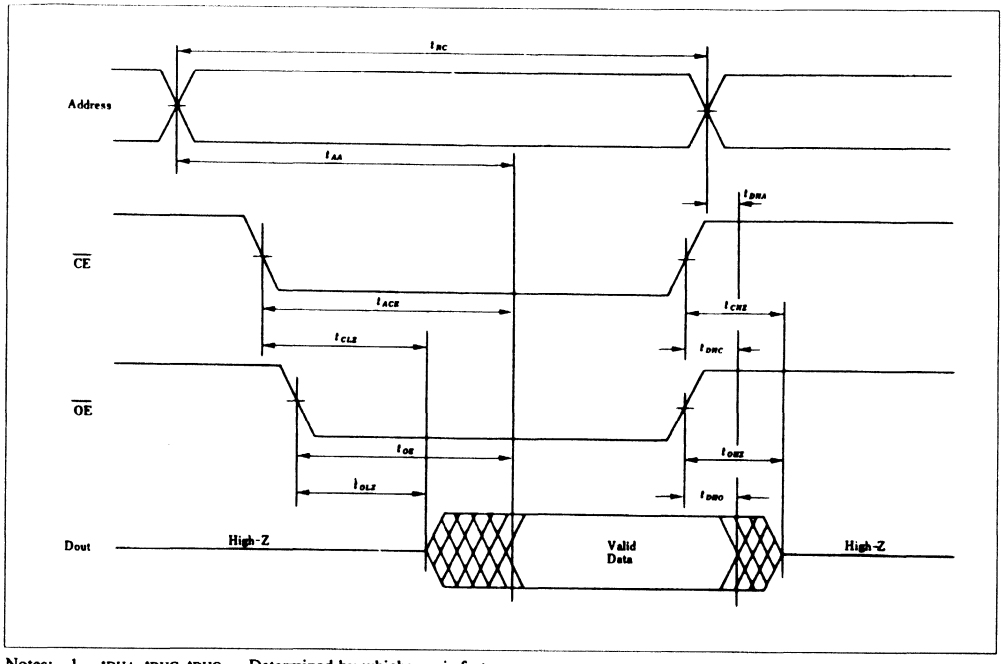
Test Condition

Input pulse level: 0.8 to 2.4V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	Min	Max	Unit
Cycle time	t_{RC}	200	—	ns
Address access time	t_{AA}	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	200	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
Output Holt Time from Address Change	t_{DHA}	0	—	ns
$\overline{CE}$ to Output in High Z*1	t_{CHZ}	—	70	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
$\overline{OE}$ access time	t_{OE}	—	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{OE}$ to Output in High Z*1	t_{OHZ}	—	70	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns

Note: *1 t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

HN62321 Series
HN62331 Series

131072-Word × 8-Bit CMOS Mask Programmable ROM

HN62321, HN62331 Series is a 1-Mbit CMOS mask-programable ROM organized as 131072-word x 8-Bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

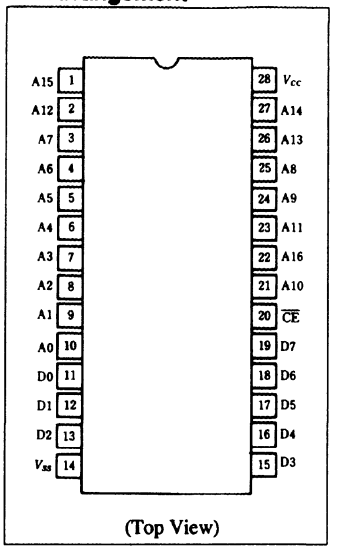
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/150/200 ns (max)
- Low power: Active 100 mW (typ),
  Standby 5 μW (typ)
- Byte-Wide Data Organization

Ordering Information

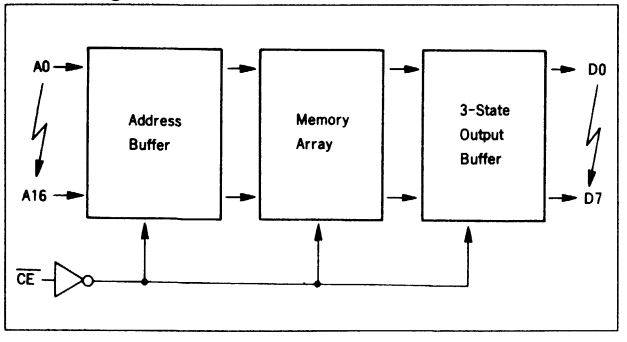
Type No.	Address Access Time	Package
HN62321P	150 ns	600 mil
HN62321BP	200 ns	28-pin
HN62331P	120 ns	plastic DIP
HN62321F	150 ns	
HN62321BF	200 ns	28-pin
HN62331F	120 ns	plastic SOP

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2*	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8*	V

Note: *NH62331 Series is V_{IH}; 2.4 V (min.) and V_{IL}; 0.45 V (max.)

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2* V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Note: *HN62331 Series is 2.4V.

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

Input pulse level: 0.8 to 2.4 V (HN62321 Series)
0.45 to 2.4 V (HN62331 Series)

Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

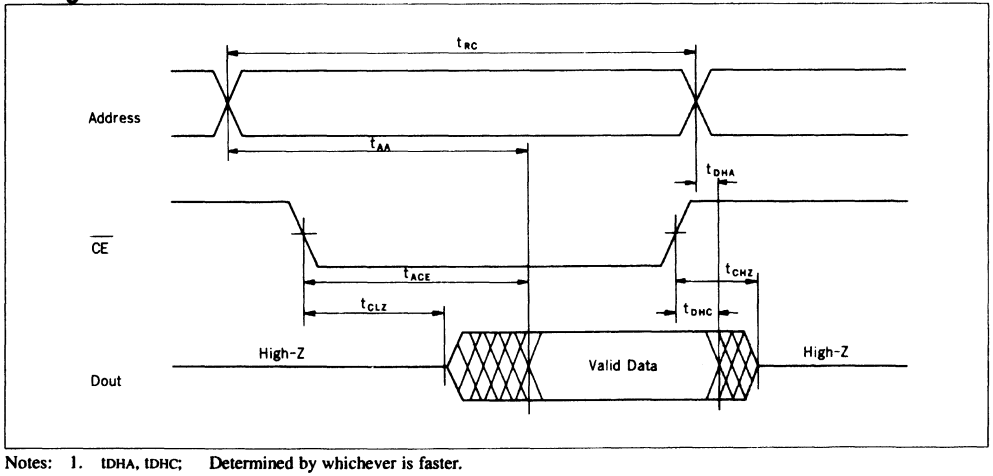
I/O timing reference level: 1.5 V

Input rise/fall time: 10 ns

Item	Symbol	HN62331		HN62321		HN62321B		Unit
		Min	Max	Min	Max	Min	Max	
Cycle time	t_{RC}	120	—	150	—	200	—	ns
Address access time	t_{AA}	—	120	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	60	—	70	—	100	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	10	—	10	—	ns

Note: *1 t_{CHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. t_{DHA}, t_{DHC}; Determined by whichever is faster.
2. t_{AA}, t_{ACE}; Determined by whichever is slower.

HN62321E Series
HN62331E Series

131072-Word × 8-Bit CMOS Mask Programmable ROM

HN62321E, HN62331E Series is a 1-Mbit CMOS mask-programable ROM organized as 131072-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

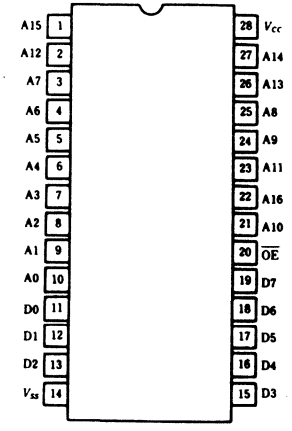
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/200 ns (max)
- $\overline{OE}$ access time: 60/100ns (max)
- Low power: 100 mW (typ)
- Byte-Wide Data Organization

Ordering Information

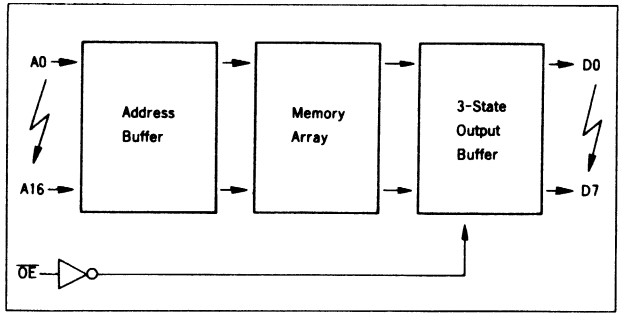
Type No.	Address Access Time	Package
HN62321EP	200 ns	600 mil 28-pin
HN62331EP	120 ns	plastic DIP
HN62321EF	200 ns	28-pin
HN62331EF	120 ns	plastic SOP

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2*	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8*	V

Note: *HN62331 series is V_{IH} : 2.4 V (min) and V_{IL}: 0.45 (max)

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Max	Unit	Test Conditions
Power supply current	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
Input leak current	$\|I_{LI}\|$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current	$\|I_{LO}\|$	—	10	µA	$\overline{OE}$ = 2.2* V, V_{OUT} = 0 to V_{CC}
Output voltage	V_{OH}	2.4	—	V	I_{OH} = –205 µA
	V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Note: *HN62331 series is 2.4 V.

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

Input pulse level: 0.8 to 2.4 V (HN62321E series) 0.45 to 2.4 V (HN62331E series)

Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

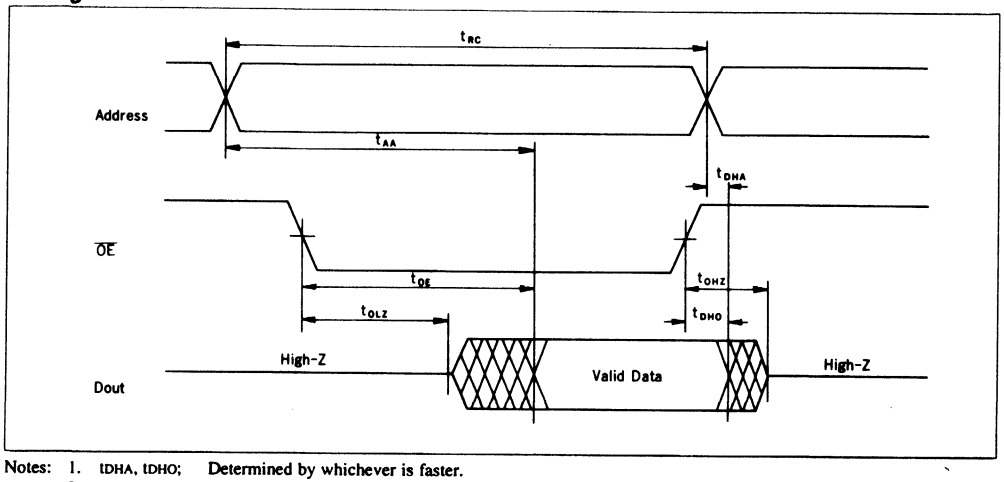
I/O timing reference level: 1.5 V

Input rise/fall time: 10 ns

Item	Symbol	HN62331E		HN62321E		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	120	—	200	—	ns
Address access time	t_{AA}	—	120	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	60	—	100	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	60	—	100	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	—	10	—	ns

Note: *1 t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. tDHA, tDHO; Determined by whichever is faster.
2. tAA, tOE; Determined by whichever is slower.

HN62321A Series
HN62331A Series

131072-Word × 8-Bit CMOS Mask Programmable ROM

HN62321A, HN62331A Series is a 1-Mbit CMOS mask-programable ROM organized to 131072-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 1M bits is optimum for a kanji character generator.

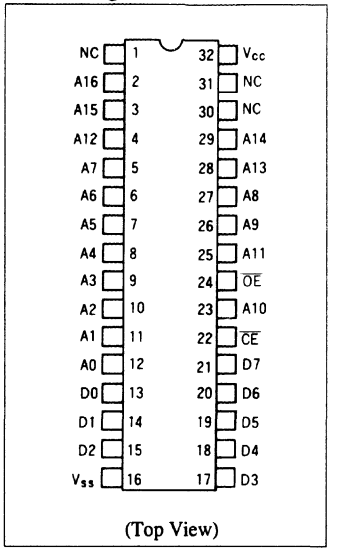
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 120/150 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide Data Organization, JEDEC pin arrangement

Ordering Information

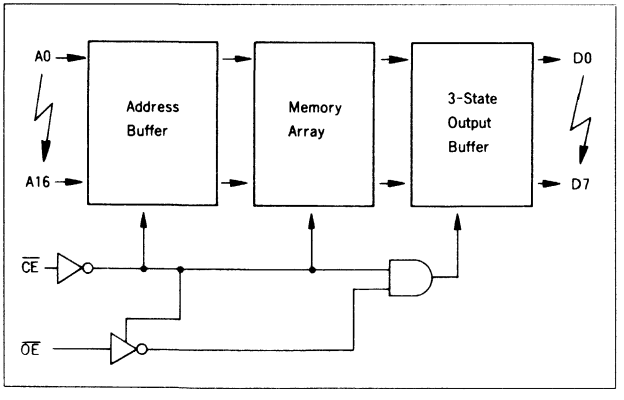
Type No.	Address Access Time	Package
HN62321AP	150 ns	600 mil 32-pin
HN62331AP	120 ns	plastic DIP
HN62321AF	150 ns	32-pin
HN62331AF	120 ns	plastic SOP

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to Vss.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2*	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8*	V

Note: * HN62331A series is V_{IH}: 2.4 V (min) and V_{IL}: 0.45 V (max)

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ –0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 3.2 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

Input pulse level: 0.8 to 2.4 V (HN62321A series)
0.45 to 2.4 V (HN62331A series)

Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

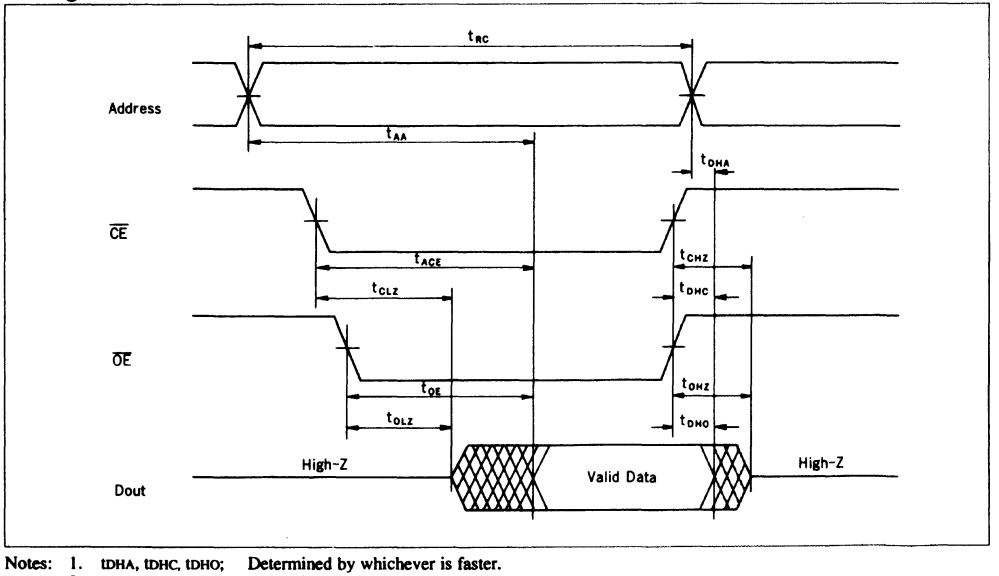
I/O timing reference level: 1.5 V

Input rise/fall time: 10 ns

Item	Symbol	HN62331A		HN62321A		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	120	—	150	—	ns
Address access time	t_{AA}	—	120	—	150	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Input in High Z	t_{CHZ}*1	—	60	—	70	ns
$\overline{OE}$ to Input in High Z	t_{OHZ}*1	—	60	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	5	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	5	—	10	—	ns

Note: *1. t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

Timing Waveform



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by whichever is faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by whichever is slower.
3. t_{CLZ}, t_{OLZ}; Determined by whichever is slower.

HN62412 Series
HN62422 Series

131072-Word × 16-Bit/262144-Word × 8-Bit CMOS Mask Programmable ROM

HN62412, HN62422 Series is a 2-Mbit CMOS mask-programable ROM organized either as 131072-word x 16-bit or as 262144-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 2M bits is optimum for a kanji character generator.

Features

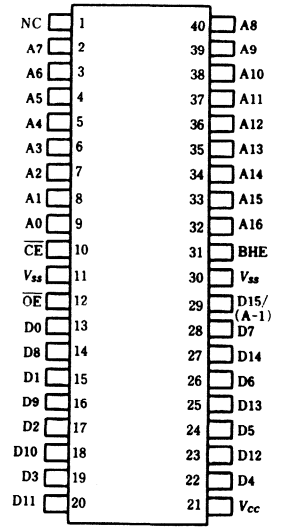
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide or Word-Wide Data Organization (switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62412P	200 ns	600 mil 40-pin
HN62422P	150 ns	plastic DIP
HN62412FP	200 ns	44-pin
HN62422FP	150 ns	plastic QFP

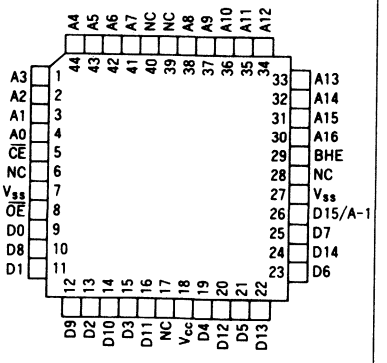
Pin Arrangement

HN62412P, HN62422P



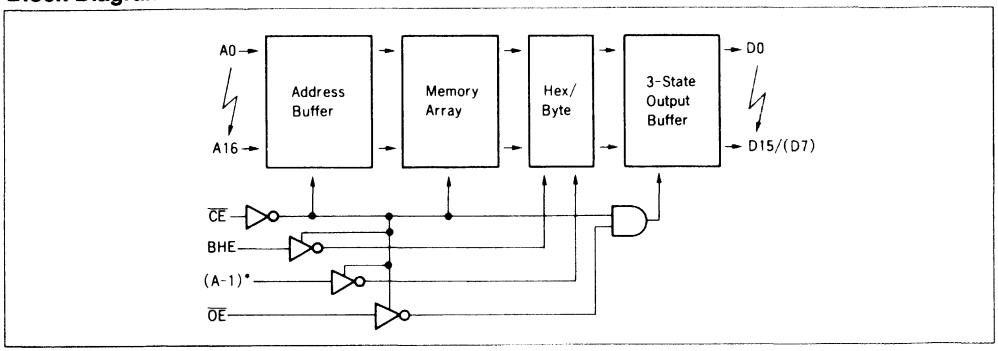
(Top View)

HN62412FP, HN62422FP



(Top View)

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1 A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current		$\|I_{LI}\|$	—	10	µA	V_{IN} =0 to V_{CC}
Output leak current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

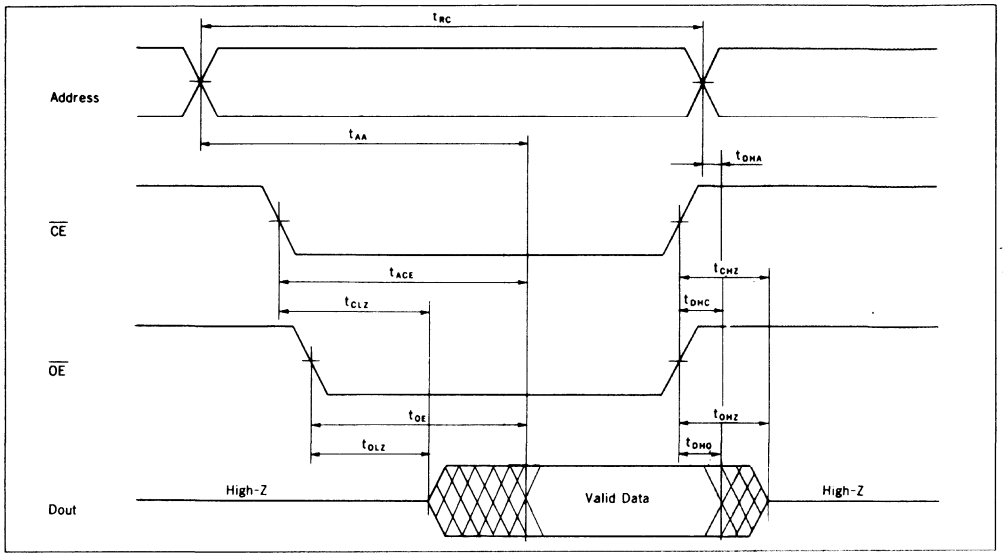
Test Conditions

Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	HN62422		HN62412		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
$\overline{BHE}$ access time	t_{BHE}	—	150	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output Hold Time from $\overline{BHE}$	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns
$\overline{BHE}$ to Output in Low Z	t_{BLZ}	10	—	10	—	ns

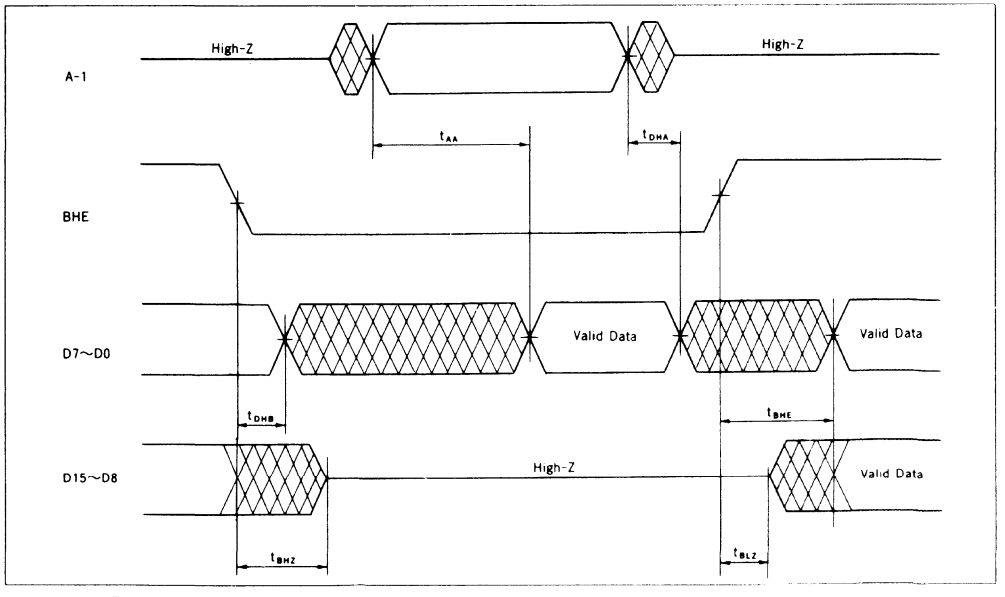
Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

Timing Waveform
Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A16–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = VIH, $\overline{CE}$ and $\overline{OE}$ are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN62404 Series
HN62424 Series

262144-Word × 16-Bit/524288-Word × 8-Bit CMOS Mask Programmable ROM

HN62404, HN62424 Series is a 4-Mbit CMOS mask-programable ROM organized either as 262144-word x 16-bit or as 524288-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

Features

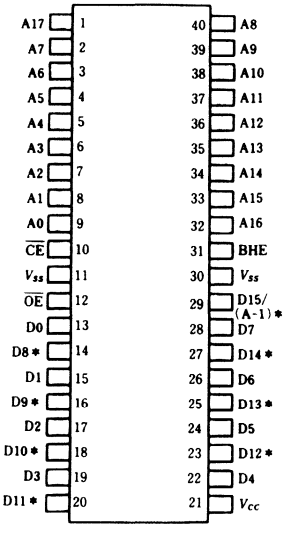
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide or Word-Wide Data Organization (switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62404P	200 ns	600 mil 40-pin
HN62424P	150 ns	plastic DIP
HN62404FP	200 ns	44-pin
HN62424FP	150 ns	plastic QFP
HN62404F	200 ns	48-pin
HN62424F	150 ns	plastic SOP

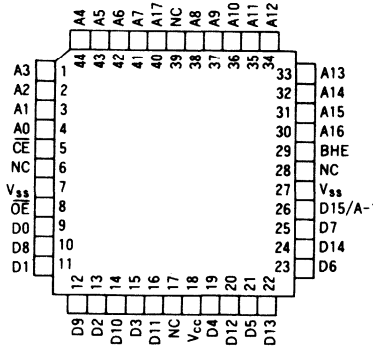
Pin Arrangement

HN62404P, HN62424P



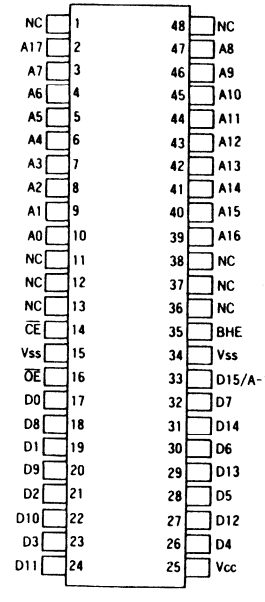
(Top View)

HN62404FP, HN62424FP



(Top View)

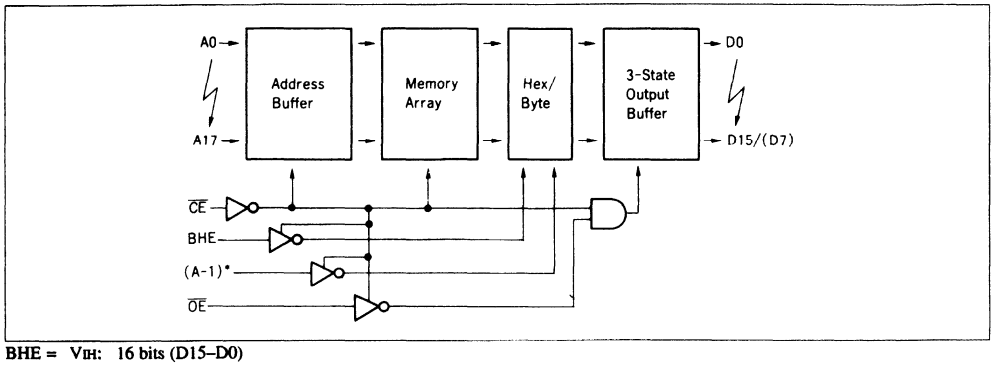
HN62404F, HN62424F



(Top View)

11-12-13 pin and 36-37-38 pin are connected to inner lead frame

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1: A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

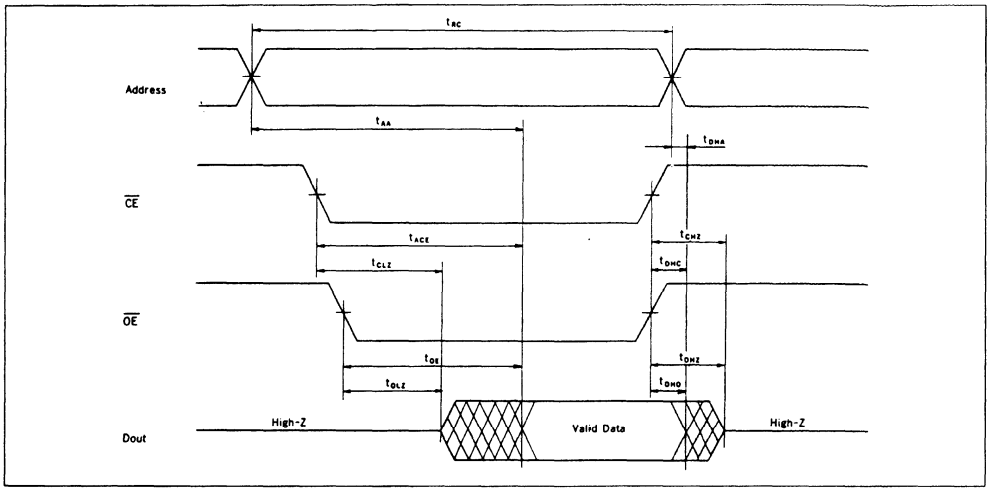
Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	HN62424		HN62404		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
$\overline{BHE}$ access time	t_{BHE}	—	150	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output Hold Time from $\overline{BHE}$	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns
$\overline{BHE}$ to Output in Low Z	t_{BLZ}	10	—	10	—	ns

Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

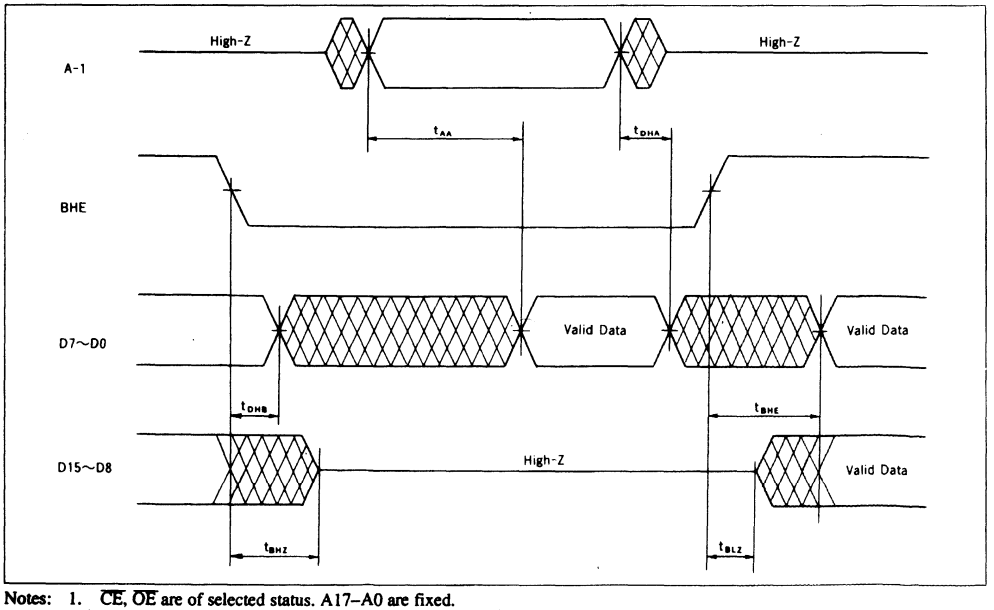
Timing Waveform

Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A17–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = VIH, CE and OE are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN62304B Series
HN62324B Series

524288-Word × 8-Bit CMOS Mask Programmable ROM

HN62304B, HN62324B Series is a 4-Mbit CMOS mask-programable ROM organized as 524288-word x 8-bits. It can be operated with a battery because of low power consumption. The large capacity of 4M bits is optimum for a kanji character generator.

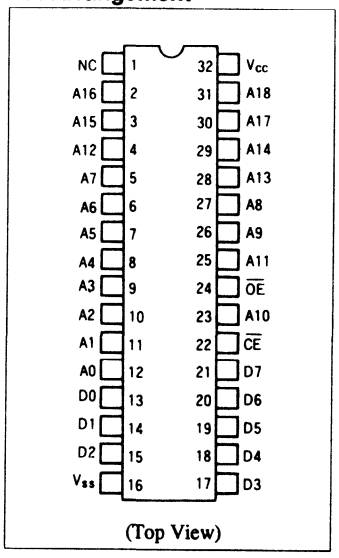
Features

- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 150/200 ns (max.)
- Low power: Active 100 mW (typ)
  Standby 5 µW (typ)
- Byte-Wide Data Organization

Ordering Information

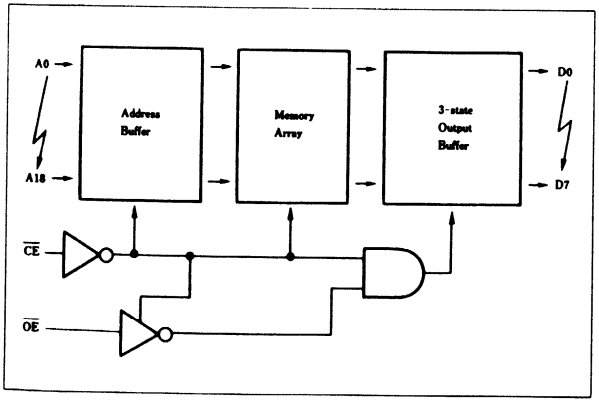
Type No.	Address Access Time	Package
HN62304BP	200 ns	600 mil 32-pin
HN62324BP	150 ns	plastic DIP
HN62304BF	200 ns	32-pin
HN62324BF	150 ns	plastic SOP

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

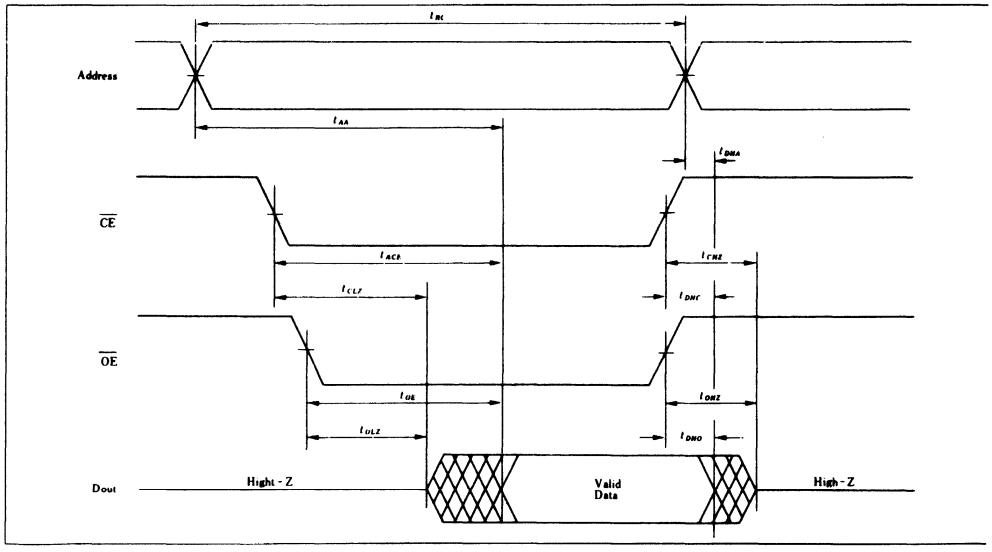
Test Conditions

Input pulse level:	0.8 to 2.4 V	Output load:	1 TTL gate + C_L = 100 pF
I/O timing reference level:	1.5 V		(including jig capacitance)
Input rise/fall time:	10 ns		

Item	Symbol	HN62324B		HN62304B		Unit
		Min	Max	Min	Max	
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
Output Hold Time from Address Change	t_{DHA}	0	—	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	10	—	ns

Note: *1 t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

Timing Waveform



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by whichever is faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by whichever is slower.
3. t_{CLZ}, t_{OLZ}; Determined by whichever is slower.

HN62408 Series

524288-Word × 16-Bit/1048576-Word × 8-Bit CMOS Mask Programmable ROM

HN62408 Series is a 8-Mbit CMOS mask-programable ROM organized either as 524288-word x 16-Bit or as 1048576-Wod x 8-Bit. It can be operated with a battery because of low power consumption. The large capacity of 8M bits is optimum for a kanji character generator.

Features

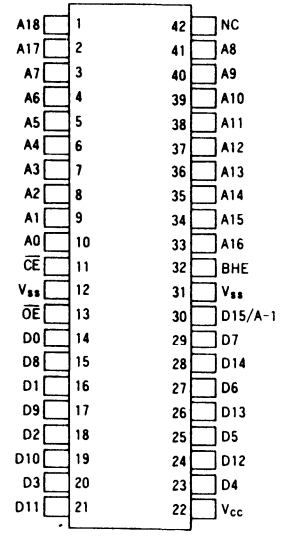
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide or Word-Wide Data Organization (switched by BHE terminal)

Ordering Information

Type No.	Address Access Time	Package
HN62408P	200 ns	600 mil 42-pin plastic DIP
HN62408FP	200 ns	44-pin plastic QFP
HN62408F	200 ns	32-pin plastic SOP

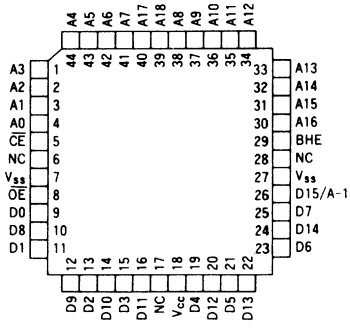
Pin Arrangement

HN62408P



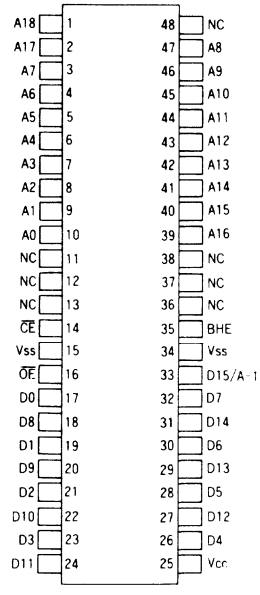
(Top View)

HN62408FP



(Top View)

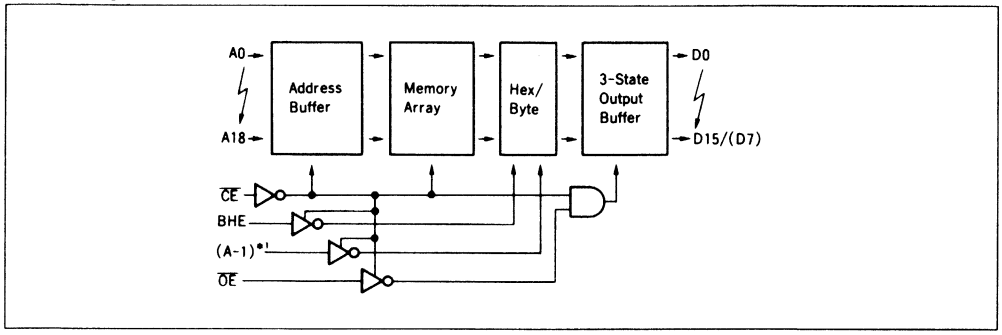
HN62408F



(Top View)

12-13 pin and 36-37 pin are connected to inner lead frame.

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1: A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

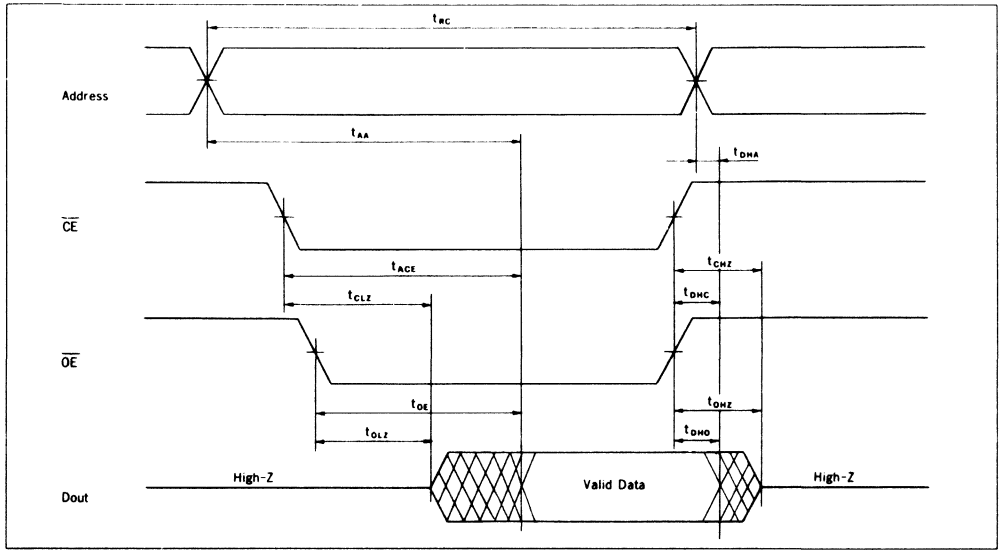
Test Conditions

Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	Min	Max	Unit
Cycle time	t_{RC}	200	—	ns
Address access time	t_{AA}	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	100	ns
$\overline{BHE}$ access time	t_{BHE}	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns
Output Hold Time from $\overline{BHE}$	t_{DHB}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{BHE}$ to Output in Low Z	t_{BLZ}	10	—	ns

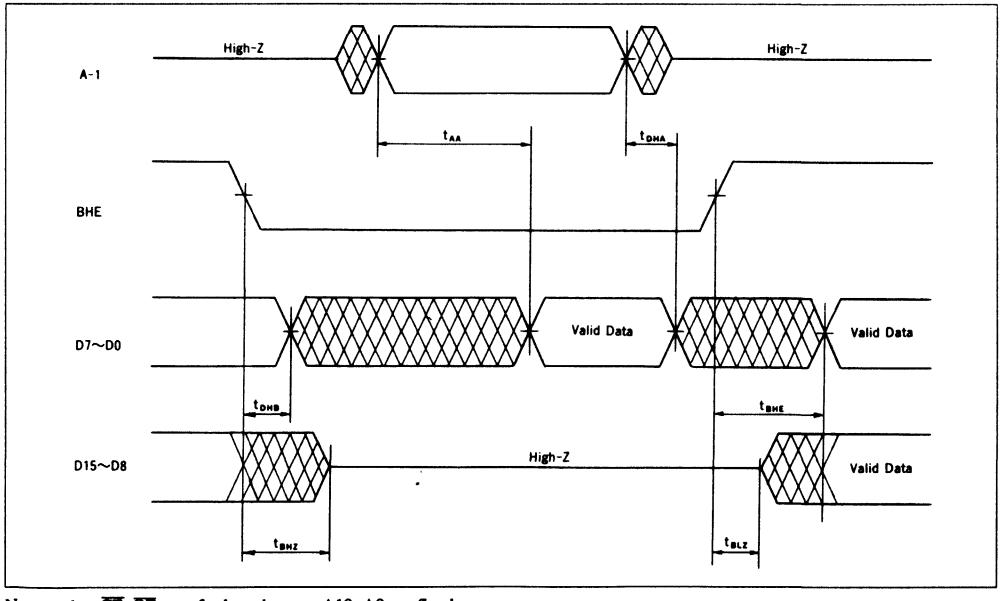
Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

Timing Waveform
Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A18–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = VIH, CE and OE are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN624016 Series

1048576-Word × 16-Bit/2097152-Word × 8-Bit CMOS Mask Programmable ROM

HN624016 Series is a 16-Mbit CMOS mask-programable ROM organized either as 1048576-word x 16-bit or as 2097152-word x 8-bit. It can be operated with a battery because of low power consumption. The large capacity of 16M bits is optimum for a kanji character generator.

Features

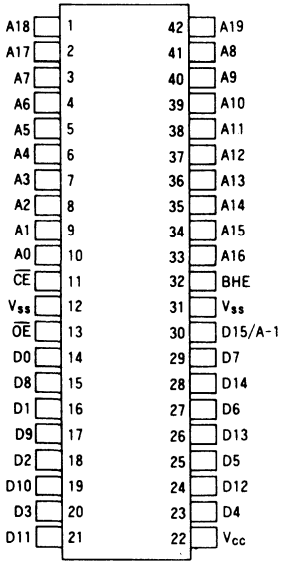
- Single 5 V
- Wired OR is permitted for the output in three states
- TTL compatible
- Address access time: 200 ns (max)
- Low power: Active 100 mW (typ)
  Standby 5 μW (typ)
- Byte-Wide or Word-Wide Data Organization (switched by BHE terminal)

Ordering Information

Type No.	Address Access	Time Package
HN624016P	200 ns	600 mil 42-pin plastic DIP
NH624016F	200 ns	48-pin plastic SOP

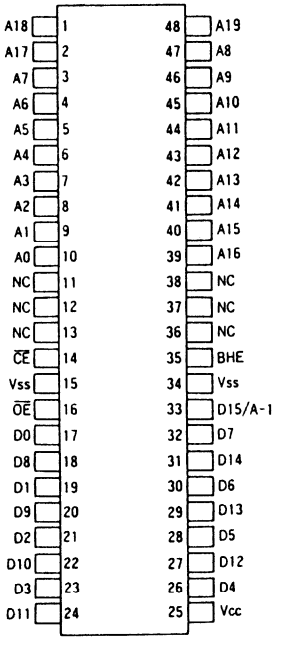
Pin Arrangement

• NH624016P



(Top View)

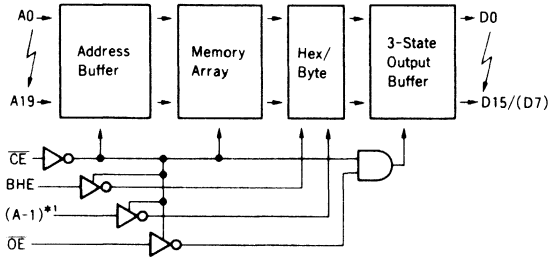
• NH624016F



(Top View)

12-13 PIN AND 36-37 pin are connected to inner lead frame

Block Diagram



BHE = V_{IH}: 16 bits (D15–D0)
BHE = V_{IL}: 8 bits (D7–D0)
*1: A-1 is least significant address input, and D14–D8 are of high impedance.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage*1	V_{CC}	–0.3 to +7.0	V
Terminal voltage*1	V_T	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: *1. With respect to Vss.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test Conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leak current		$\lvert I_{LI} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leak current		$\lvert I_{LO} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: *1. This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

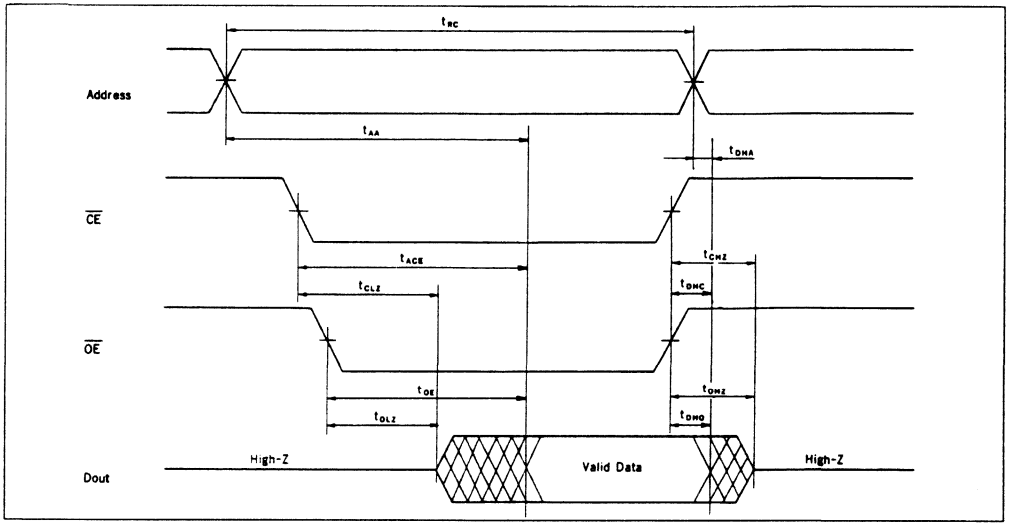
Test Conditions

Input pulse level: 0.8 to 2.4 V
I/O timing reference level: 1.5 V
Input rise/fall time: 10 ns
Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

Item	Symbol	Min	Max	Unit
Cycle time	t_{RC}	200	—	ns
Address access time	t_{AA}	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	100	ns
$\overline{BHE}$ access time	t_{BHE}	—	200	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Output Hold Time from $\overline{CE}$	t_{DHC}	0	—	ns
Output Hold Time from $\overline{OE}$	t_{DHO}	0	—	ns
Output Hold Time from $\overline{BHE}$	t_{DHB}	0	—	ns
$\overline{CE}$ to Output in High Z	t_{CHZ}*1	—	70	ns
$\overline{OE}$ to Output in High Z	t_{OHZ}*1	—	70	ns
$\overline{BHE}$ to Output in High Z	t_{BHZ}*1	—	70	ns
$\overline{CE}$ to Output in Low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to Output in Low Z	t_{OLZ}	10	—	ns
$\overline{BHE}$ to Output in Low Z	t_{BLZ}	10	—	ns

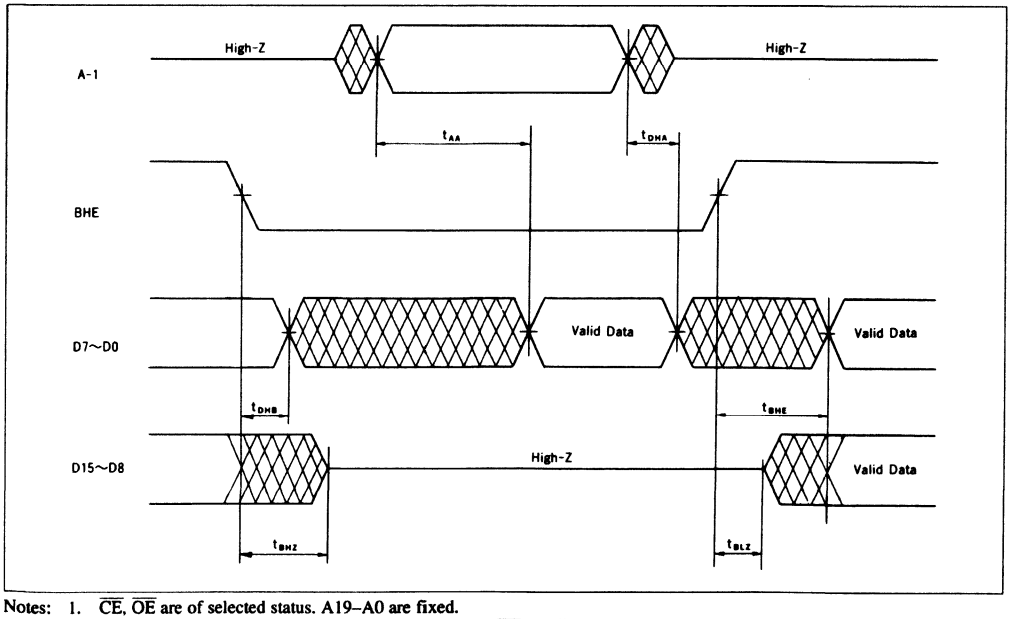
Note: *1 t_{CHZ}, t_{OHZ}, and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

Timing Waveform
Word Mode (BHE = "VIH") or Byte Mode (BHE = "VIL")



Notes: 1. tDHA, tDHC, tDHO; Determined by whichever is faster.
2. tAA, tACE, tOE; Determined by whichever is slower.
3. tCLZ, tOLZ; Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A19–A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = VIH, $\overline{CE}$ and $\overline{OE}$ are of selected state.
At this time, an input signal that is of the inverse phase to the output should not be impressed.

HN62308B Series

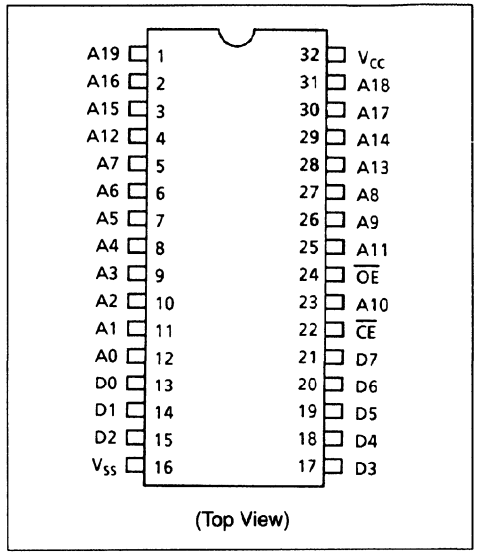
1048576 8-Bit CMOS MASK Programmable Read Only Memory

The HN62308B is a 8-Mbit CMOS mask-programmable ROM organized as 1048576 words by 8-bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62308B, which provides large capacity of 8 Mbits, is ideally suited for kanji character generators.

Features

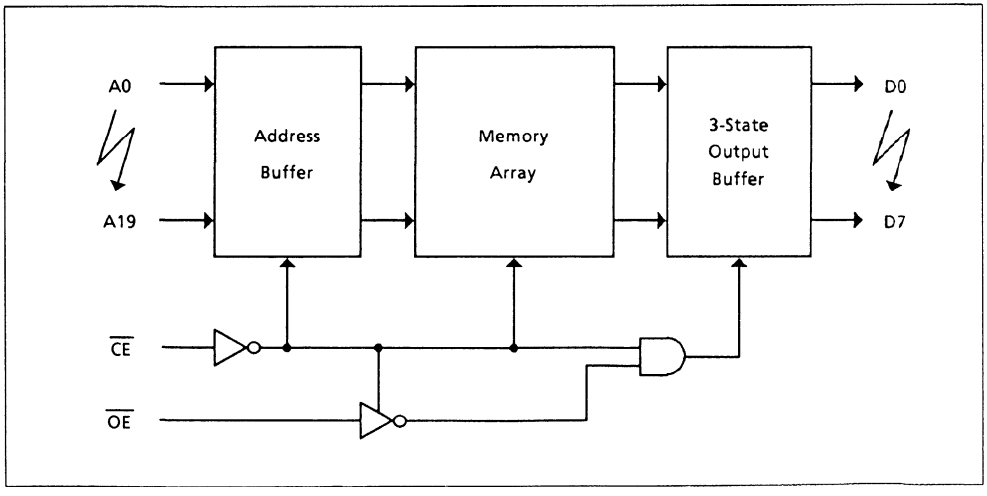
- Single +5 V power supply
- Three-state data output for OR-tieing
- TTL compatible
- Maximum access time: 200 ns (max)
- Low power consumption: 100 mW (typ) active
  5 µW (typ) standby
- Byte-wide data organization
- Pin compatible with JEDEC

Pin Arrangement



(Top View)

Block Diagram



Ordering Information

Type No.	Access time	Package
HN62308BP	200 ns	600 mil 32-pin plastic DIP
HN62308BF	200 ns	32-pin plastic SOP

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C) (cont)

Item	Symbol	Min	Max	Unit	Test conditions
Output leakage current	$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage	V_{OH}	2.4	—	V	I_{OH} = –205 µA
	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin= 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested.

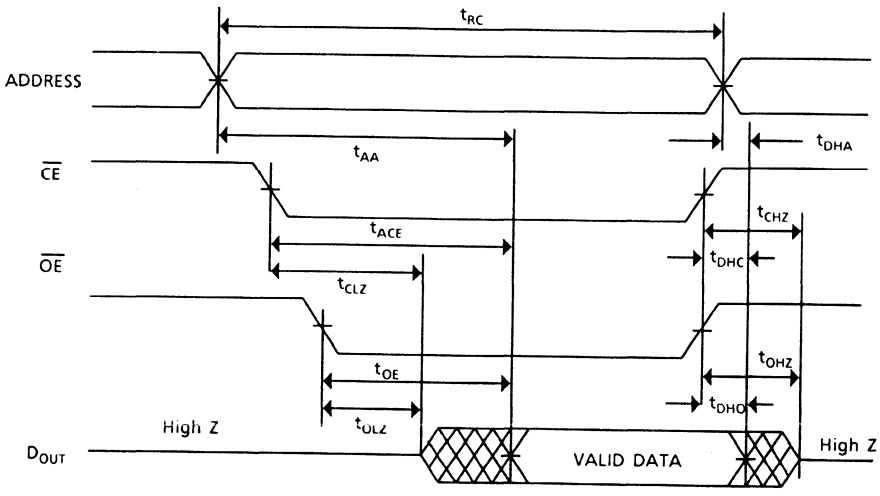
AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	200	—	ns
Address access time	t_{AA}	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	100	ns
Output hold time from address change	t_{DHA}	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*	—	70	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*	—	70	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	10	—	ns

Note: *; t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circut conditions and are not referred to output voltage levels.

- Output load; 1 TTL gate + CL = 100 pF (including jig capacitance)
- Input pulse level; 0.8 to 2.4 V
- Input and output timing reference level; 1.5 V
- Input rise and fall time; 10 ns

Timing Diagram



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by slower.
3. t_{CLZ}, t_{OLZ}; Determined by slower.

HN62414 Series

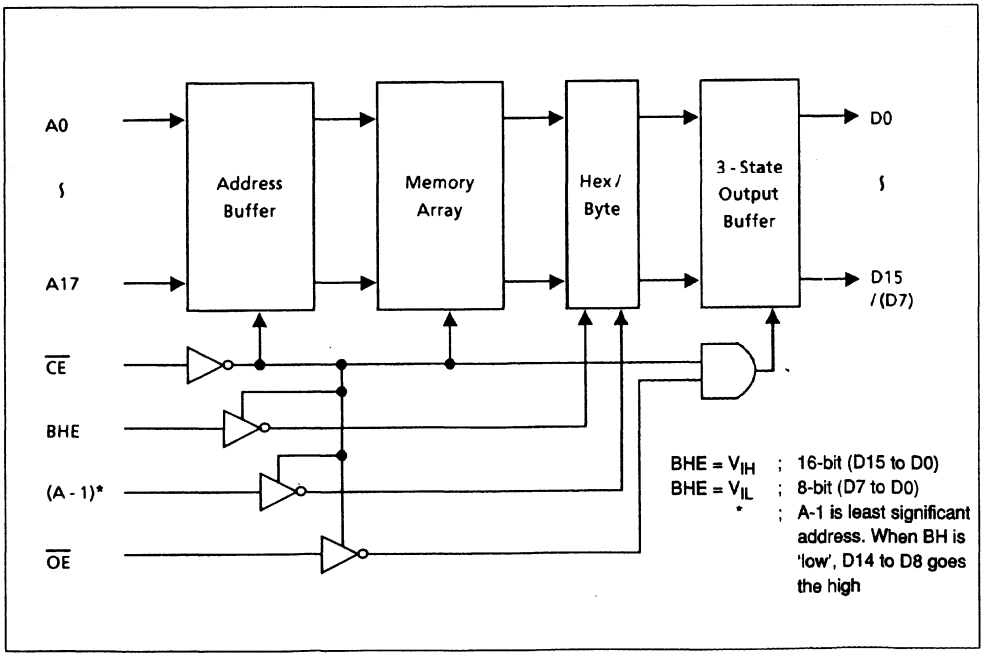
262114 × 16-Bit/524288 × 8-Bit CMOS MASK Programmable Read Only Memory

The HN62414 is a 4-Mbit CMOS mask-programmable ROM organized either as 262414 words by 16 bits or as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62414, which provides large capacity of 4M bits, is ideally suited for kanji character generators.

Features

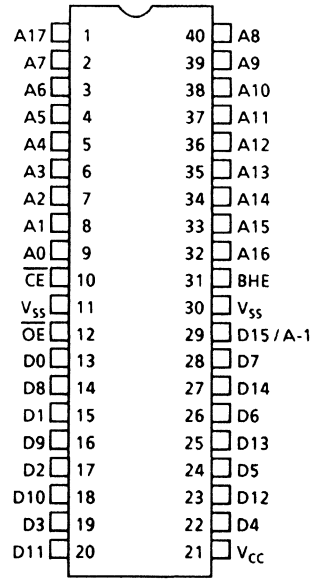
- Single +5 V power supply
- Three-state data output for OR-tieing
- TTL compatible
- Maximum access time: 170/200 ns (max)
- Low power consumption: 100 mW (Typ) active
  5 μW (Typ) standby
- Byte-wide or word-wide data organization with BHE

Block Diagram



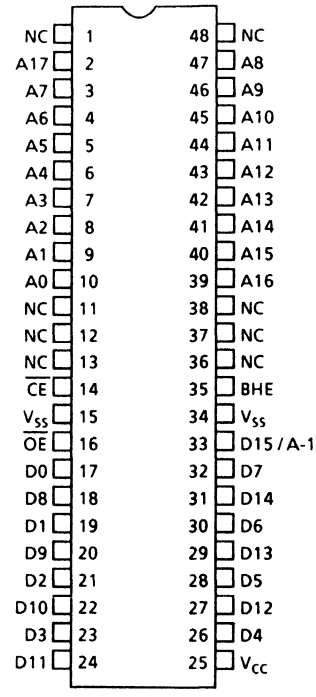
Pin Arrangement

• HN62414P



(Top View)

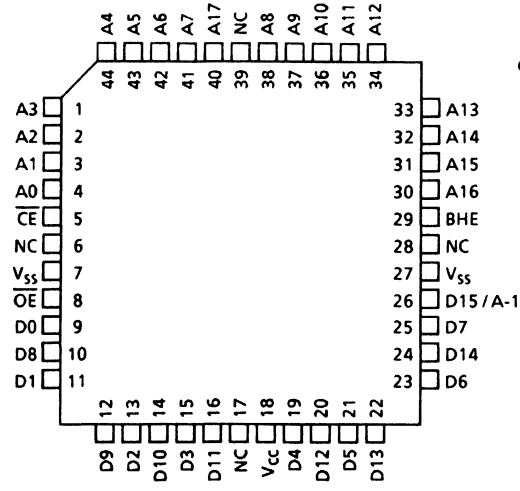
• HN62414F



(Top View)

11-12-13 pin and 36-37-38 pin are connected to inner lead frame.

• HN62414FP



(Top View)

Ordering Information

Type No.	Access time	Package
HN62414P-17/-20	170/200 ns	600 mil 40-pin plastic DIP
HN62414FP-17/-20	170/200 ns	44-pin plastic QFP
HN62414F-17/-20	170/200 ns	48-pin plastic SOP

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to + 70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

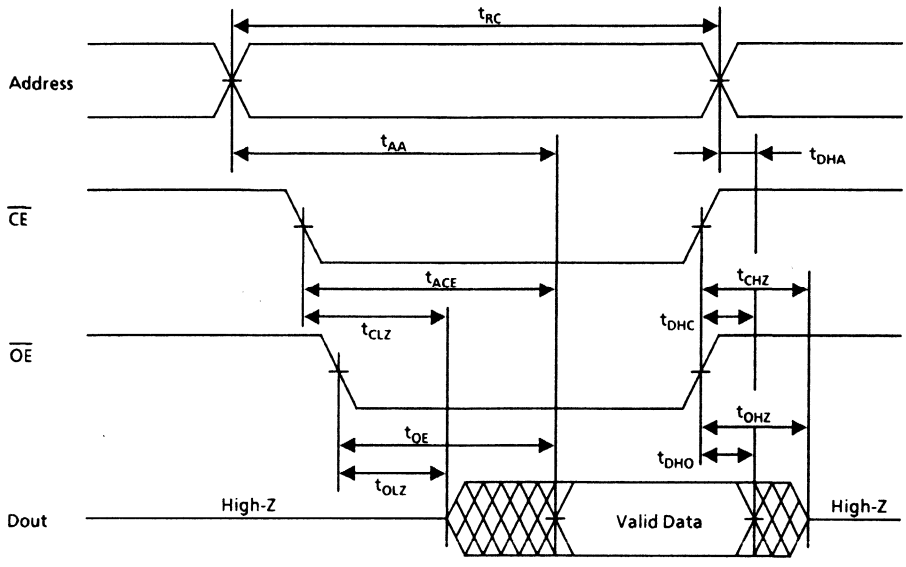
- Output load; 1 TTL gate + CL = 100 pF (including jig capacitance)
- Input pulse level; 0.8 to 2.4 V
- Input and output timing reference level; 1.5 V
- Input rise and fall time; 10 ns

		HN62414-17		HN62414-20		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	170	—	200	—	ns
Address access time	t_{AA}	—	170	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	170	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
BHE access time	t_{BHE}	—	170	—	200	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*	—	70	—	70	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*	—	70	—	70	ns
BHE to output in high Z	t_{BHZ}*	—	70	—	70	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	10	—	10	—	ns
BHE to output in low Z	t_{BLZ}	10	—	10	—	ns

Note: *; t_{CHZ} t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circut conditions and are not referred to output voltage levels.

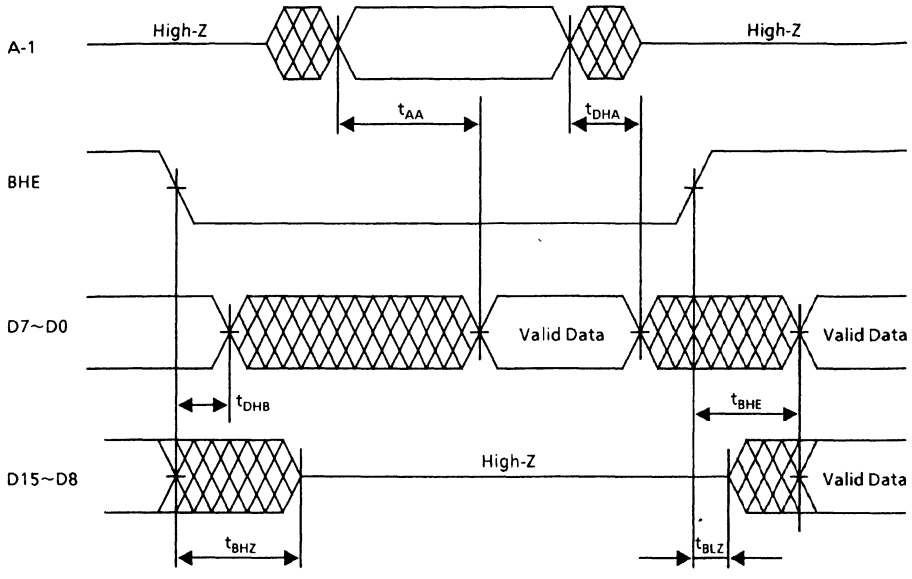
Timing Diagram

(1) Word Mode (BHE = 'VIH') or Byte Mode (BHE = 'VIL')



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by slower.
3. t_{CLZ}, t_{OLZ}; Determined by slower.

(2) Word Mode, Byte Mode Switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A17 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not applied to them.

HN62444 Series

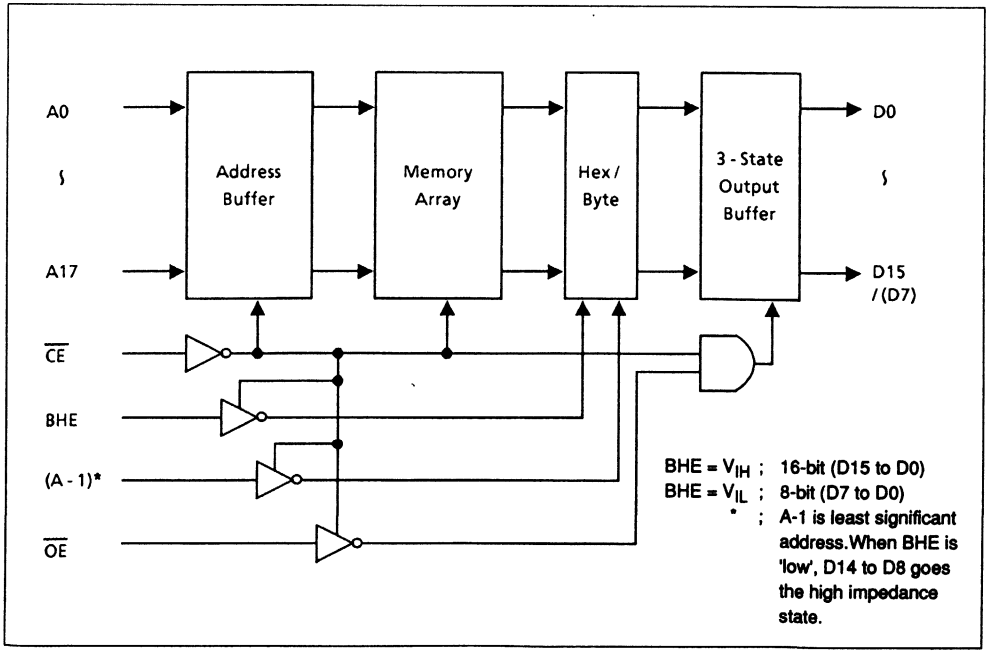
262144 × 16-Bit/524288 × 8-Bit CMOS Mask Programmable Read Only Memory

The HN62444 is a 4-Mbit CMOS mask-programmable ROM organized either as 262144 words by 16 bits or as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62444, which provides large capacity of 4 Mbits, is ideally suited for kanji character generators.

Features

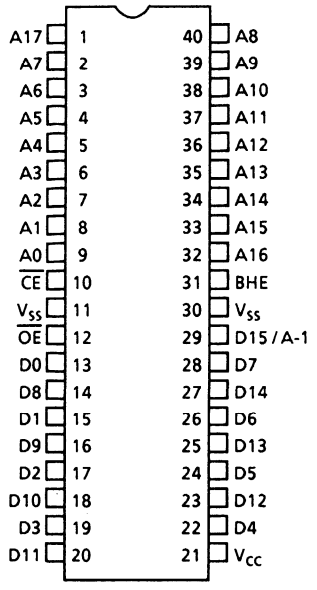
- Single +5 V power supply
- Three-state data output for OR-Tieing
- TTL compatible
- Maximum access time: 100 ns (Max)
- Low power consumption: 150 mW (Typ) active
  5 µW (Typ) standby
- Byte-wide or word-wide data organization with BHE

Block Diagram



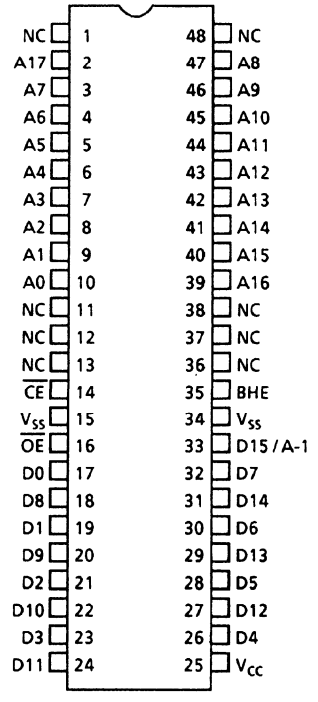
Pin Arrangement

• HN62444P



(Top View)

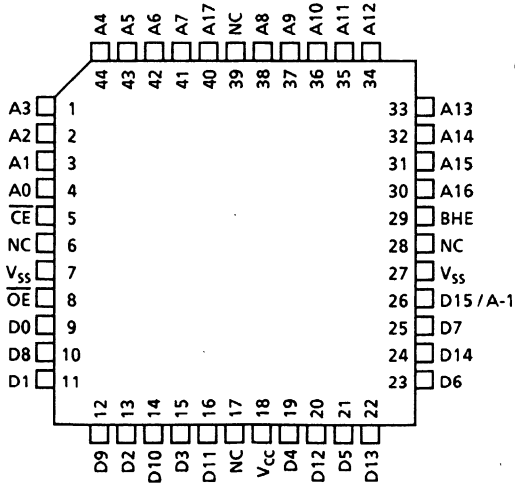
• HN62444F



(Top View)

11-12-13 pin and 36-37-38 pin are connected to inner lead frame.

• HN62444FP



(Top View)

Ordering Information

Type No.	Access time	Package
HN62444P	100 ns	600 mil 40-pin plastic DIP
HN62444FP	100 ns	44-pin plastic QFP
HN62444F	100 ns	48-pin plastic SOP

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.45	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	60	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ – 0.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.4 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: *; This parameter is sampled and not 100% tested.

AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

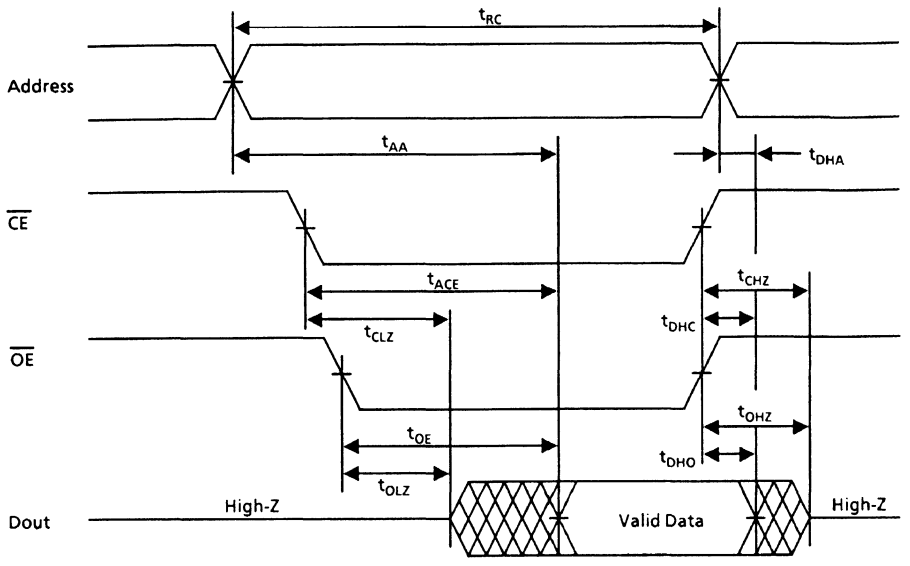
- Output load; 1 TTL gate + CL = 100 pF (including jig capacitance)
- Input pulse level; 0.45 to 2.4 V
- Input and output timing reference level; 1.5 V
- Input rise and fall time; 10 ns

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	100	—	ns
Address access time	t_{AA}	—	100	ns
$\overline{CE}$ access time	t_{ACE}	—	100	ns
$\overline{OE}$ access time	t_{OE}	—	55	ns
BHE access time	T_{BHE}	—	100	ns
Output hold time from address change	t_{DHA}	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*	—	40	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*	—	40	ns
BHE to output in high Z	tBHZ*	—	40	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	ns
BHE to output in low Z	t_{BLZ}	5	—	ns

Note: *; t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

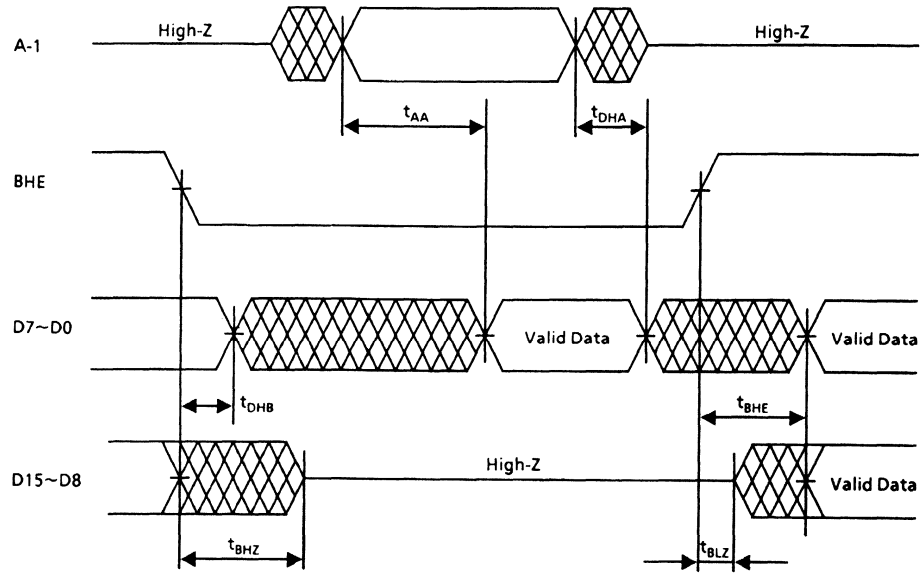
Timing Diagram

(1) Word mode (BHE = 'V_{IH}') or byte mode (BHE = 'V_{IL}')



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by slower.
3. t_{CLZ}, t_{OLZ}; Determined by slower.

(2) Word mode, byte mode switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A17 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

HN62444BP — Product preview

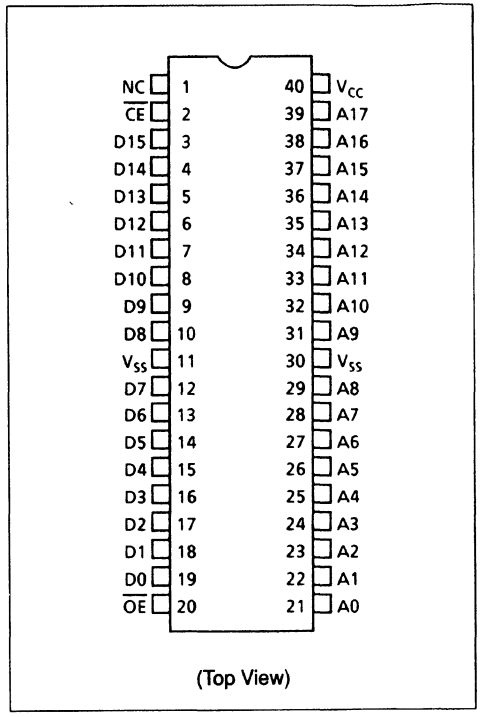
262144 × 16-Bit CMOS Mask Programmable Read Only Memory

The HN62444BP is a 4-Mbit CMOS mask-programmable ROM by 16 bits. The HN62444BP is pin-compatible to the EPROM organized as 262144 words by 16 bits. And a high speed access of 100 ns is the most suitable to the system using a high speed microcomputer by 16 bits as 8086 and 68000, etc.

Features

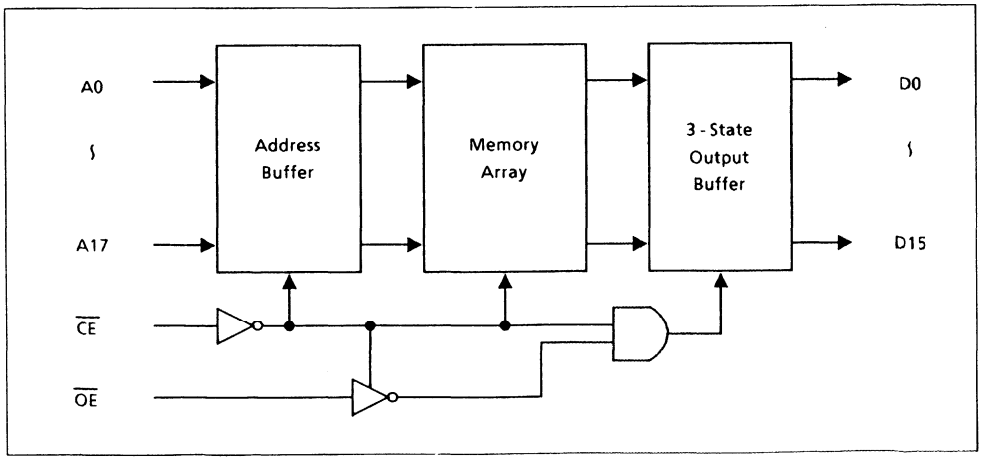
- Single +5 V power supply
- Three-state data output for OR-tieing
- TTL compatible
- Maximum access time: 100 ns (max)
- Low power consumption: 150 mW (typ) active
  5 µW (typ) standby
- Word-wide data organization
- Pin compatible with JEDEC

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	V_T	–0.3 to V_{CC} +0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.45	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	60	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ –0.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.4 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin= 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

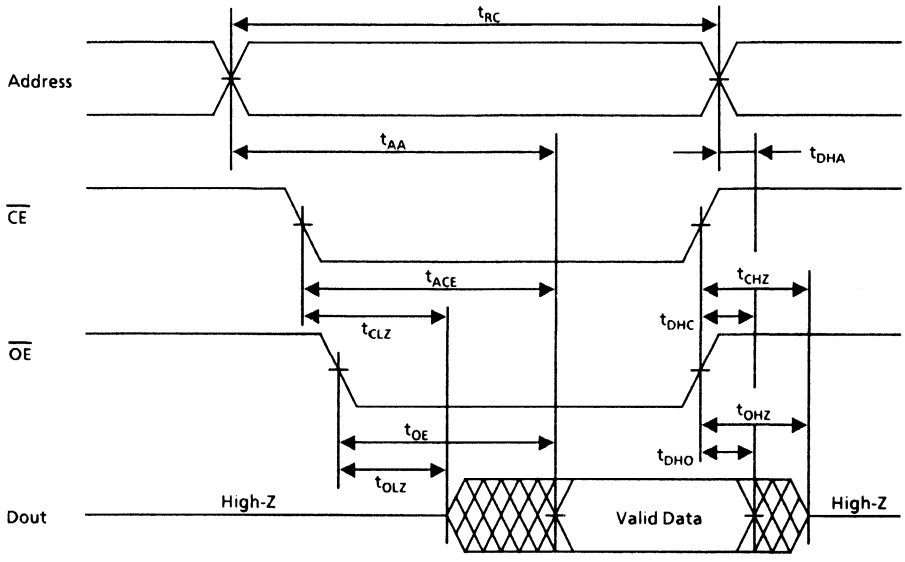
AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta= 0 to +70°C)

- Output load: 1 TTL gate + C_L = 100 pF (Including jig capacitance)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	100	—	ns
Address access time	t_{AA}	—	100	ns
$\overline{CE}$ access time	t_{ACE}	—	100	ns
$\overline{OE}$ access time	t_{OE}	—	55	ns
Output hold time from address change	t_{DHA}	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*	—	40	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*	—	40	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	ns

Note: *; t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

Timing Diagram



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by slower.
3. t_{CLZ}, t_{OLZ}; Determined by slower.

HN62314B Series

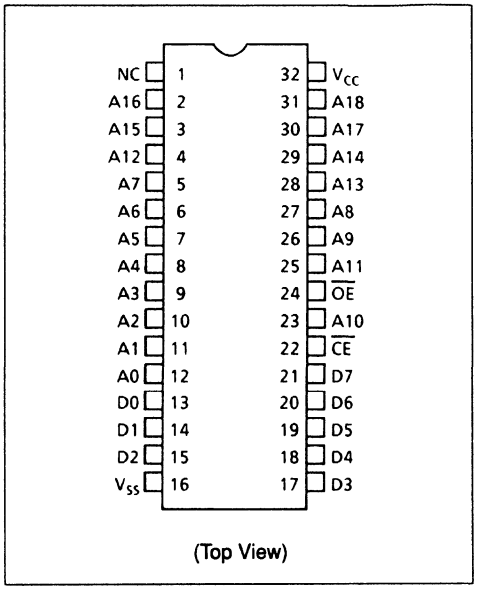
524288 × 8-Bit CMOS Mask Programmable Read Only Memory

The HN62314B is a 4-Mbit CMOS mask-programmable ROM organized as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62314B, which provides large capacity of 4 Mbits, is ideally suited for kanji character generators.

Features

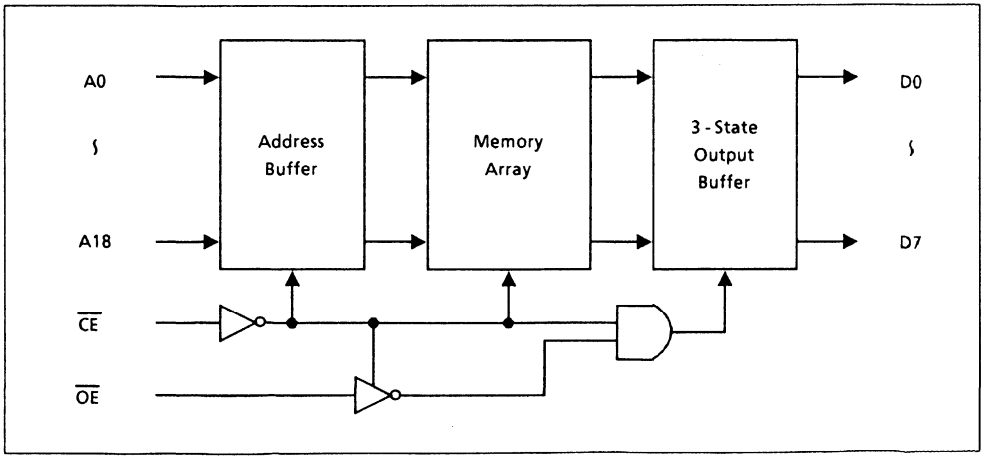
- Single +5 V power supply
- Three-state data output for OR-tieing
- TTL compatible
- Maximum access time: 200 ns (max)
- Low power consumption: 100 mW (typ) active
  5 µW (typ) standby
- Byte-wide data organization
- Pin compatible with JEDEC

Pin Arrangement



(Top View)

Block Diagram



Ordering Informations

Type No.	Access time	Package
HN62314BP-17/20	170/200 ns	600-mil 32-pin plastic DIP
HN62314BF-17/20	170/200 ns	32-pin plastic SOP

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

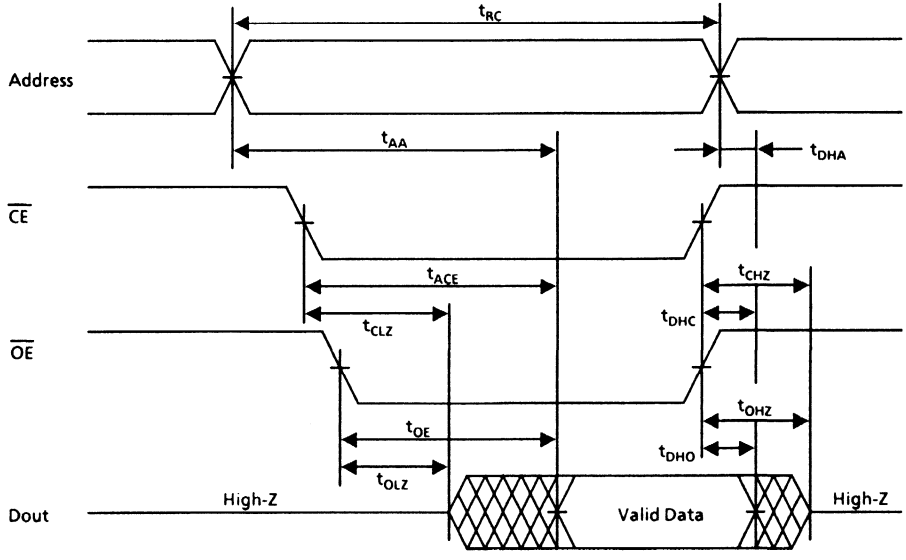
AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

- Output load; 1 TTL gate + CL = 100 pF (including jig capacitance)
- Input pulse level; 0.8 to 2.4 V
- Input and output timing reference level; 1.5 V
- Input rise and fall time; 10 ns

		HN62314B-17		HN62314B-20		
Item	Symbol	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	170	—	200	—	ns
Address access time	t_{AA}	—	170	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	170	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*	—	70	—	70	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*	—	70	—	70	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	10	—	10	—	ns

Note: *; t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

Timing Diagram



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by slower.
3. t_{CLZ}, t_{OLZ}; Determined by slower.

HN62344B Series — Preliminary

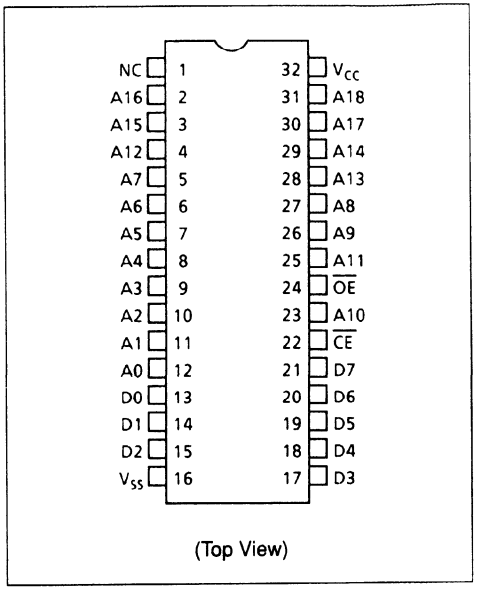
524288 × 8-Bit CMOS Mask Programmable Read Only Memory

The HN62344B is a 4-Mbit CMOS mask-programmable ROM organized as 524288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62344B, which provides large capacity of 4 Mbits, is ideally suited for kanji character generators.

Features

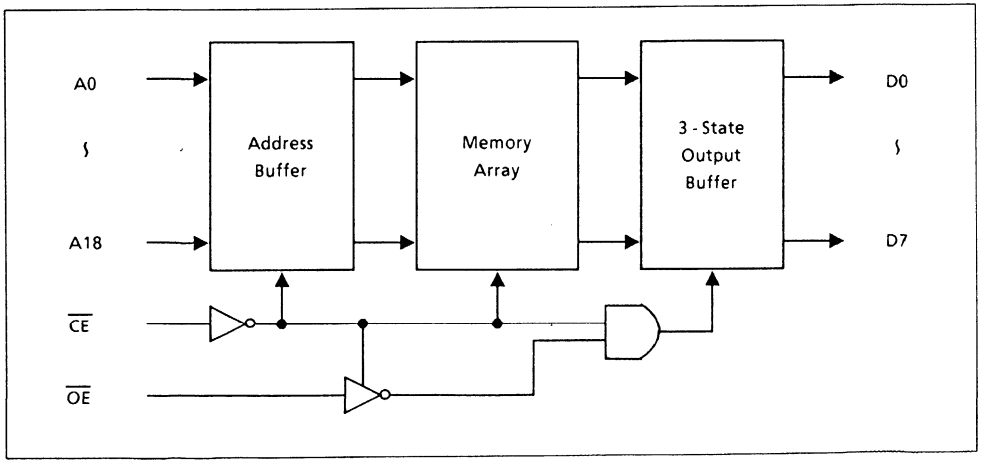
- Single +5 V power supply
- Three-state data output for OR-tieing
- TTL compatible
- Maximum access time: 100 ns (max)
- Low power consumption: 150 mW (typ) active
  5 µW (typ) standby
- Byte-wide data organization
- Pin compatible with JEDEC

Pin Arrangement



(Top View)

Block Diagram



Ordering Informations

Type No.	Access time	Package
HN62344BP	100 ns	600-mil 32-pin plastic DIP
HN62344BF	100 ns	32-pin plastic SOP

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	V_T	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.45	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	60	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.4 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

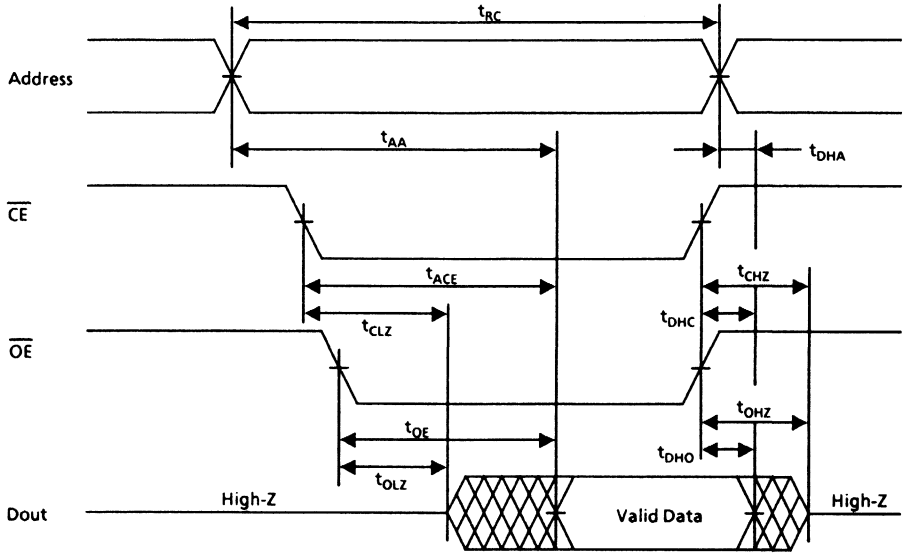
AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

- Output load; 1 TTL gate + CL = 100 pF (including jig capacitance)
- Input pulse level; 0.45 to 2.4 V
- Input and output timing reference level; 1.5 V
- Input rise and fall time; 10 ns

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	100	—	ns
Address access time	t_{AA}	—	100	ns
$\overline{CE}$ access time	t_{ACE}	—	100	ns
$\overline{OE}$ access time	t_{OE}	—	55	ns
Output hold time from address change	t_{DHA}	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*	—	40	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*	—	40	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	ns

Note: *; t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

Timing Diagram



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}; Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}; Determined by slower.
3. t_{CLZ}, t_{OLZ}; Determined by slower.

MOS PROM

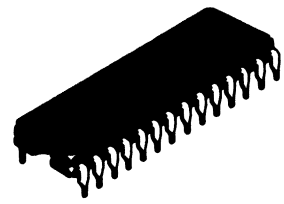
HN58C65 Series

8192-word x 8-bit Electrically Erasable and Programmable CMOS ROM

■ FEATURES

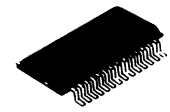
- Single 5V Supply
- On Chip Latches; Address, Data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic Byte Write . . . . . 10ms max.
- Automatic Page Write
  (32byte) . . . . . 10ms max.
- Fast Access Time . . . . . 250ns max.
- Low Power Dissipation . . . 20mW/MHz typ. (Active)
  . . . 2mW typ. (Standby)
- $\overline{DATA}$ Polling and Ready/$\overline{Busy}$
- Data Protection Circuity on Power On/Power Off
- Conforms to JEDEC Byte-Wide Standard
- Reliable CMOS with MNOS Cell Technology
- 10^5 Erase/Write Cycles in page mode
- 10-year Data Retention

HN58C65P Series



(DP-28)

HN58C65FP Series



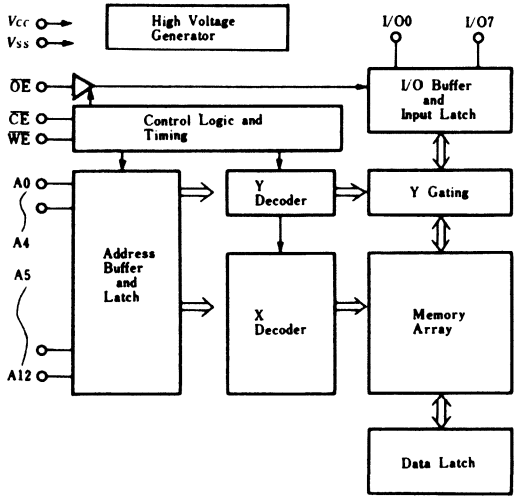
(FP-28D/DA)

■ ORDERING INFORMATION

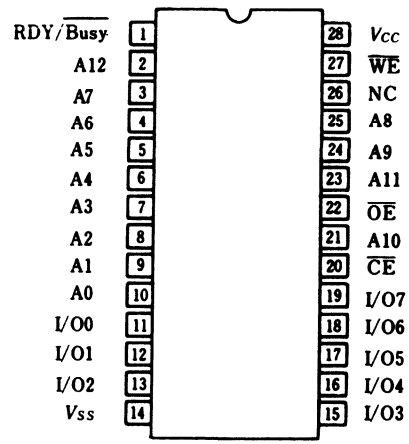
Type No.	Access Time	Package
HN58C65P-25	250ns	600 mil 28 pin Plastic DIP
HN58C65FP-25	250ns	28 pin Plastic SOP

Note) T is added to the end of the type no. for a SOP of 3.0mm (max.) thickness.

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

A0 – A12	Address Input
I/O1 – I/O7	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No Connect

■ MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	RDY/$\overline{Busy}$ (1)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	V_{IH}	High Z	Dout
Standby	V_{IH}	X	X	High Z	High Z
Write	V_{IL}	V_{IH}	V_{IL}	High Z→ V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Write Inhibit	X	X	V_{IH}	High Z	–
Write Inhibit	X	V_{IL}	X	High Z	–
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data Out (I/O7)

Note: X: V_{IL} or V_{IH}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*1	V_{CC}	–0.6 to +7.0	V
Input Voltage*1	V_{in}	–0.5*2 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Notes: *1. With respect to V_{SS}.
*2. –3.0V for pulse width ≦ 50ns.

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	–0.3	–	0.8	V
	V_{IH}	2.2	–	V_{CC}+1	V
Operating Temperature	T_{opr}	0	–	70	°C

■ DC AND OPERATING CHARACTERISTICS (T_a =0 to +70°C, V_{CC} =5V±10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = 5.5V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{CC} = 5.5V V_{out} = 5.5/0.4V	–	–	2	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	1	mA
V_{CC} Current (Active)	I_{CC2}	Iout=0mA, duty=100%, cycle 1μs	–	–	8	mA
		Iout=0mA, duty=100%, Min. Cycle	–	–	25	mA
Input Low Voltage	V_{IL}		–0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –400μA	2.4	–	–	V

Note: *1. –1.0V for pulse width ≦ 50ns

■ CAPACITANCE (T_a =25°C, f=1MHz)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	6	pF
Output Capacitance	C_{out}	V_{out} =0V	–	–	12	pF

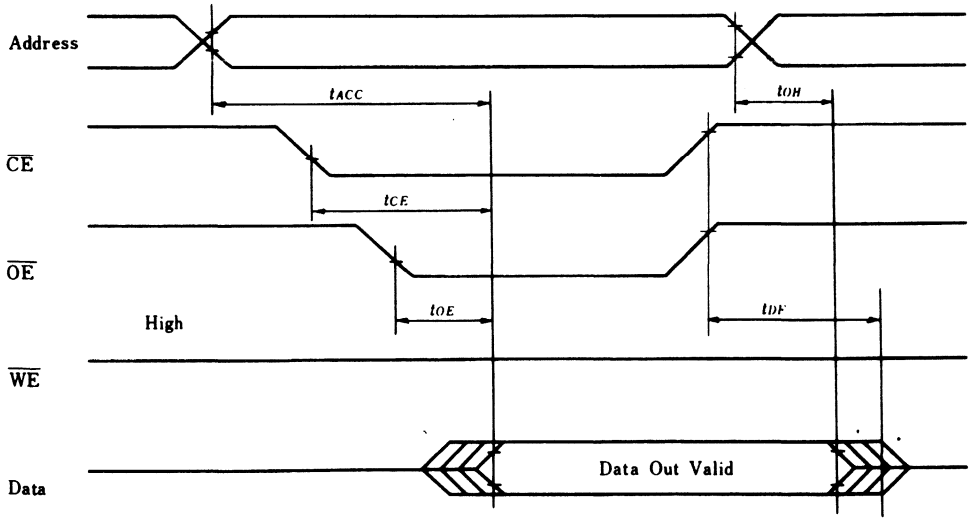
■ AC CHARACTERISTICS (T_a=0 to +70°C, V_{CC}=5V±10%)

• AC Test Conditions

Input Pulse Levels: 0.40V to 2.4V
Input Rise and Fall Time: ≤20ns
Output Load: 1TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2V
Outputs; 0.8V and 2V

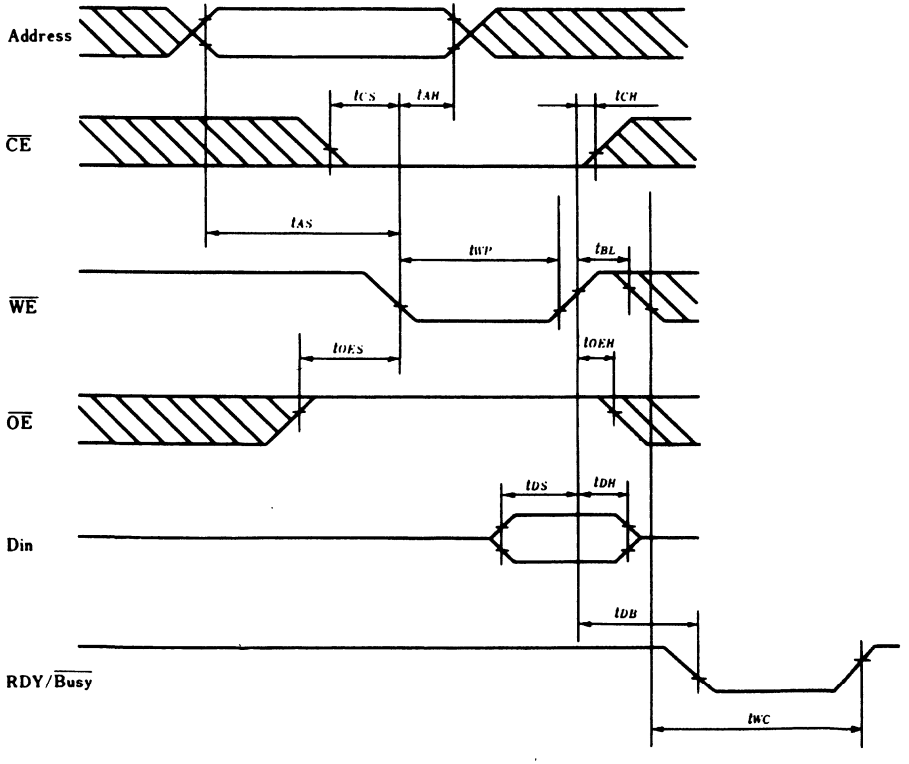
• Read Operation

Parameter	Symbol	Test Condition	HN58C65-25		Unit
			min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	10	100	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	–	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL} $\overline{WE}$ = V_{IH}	0	90	ns



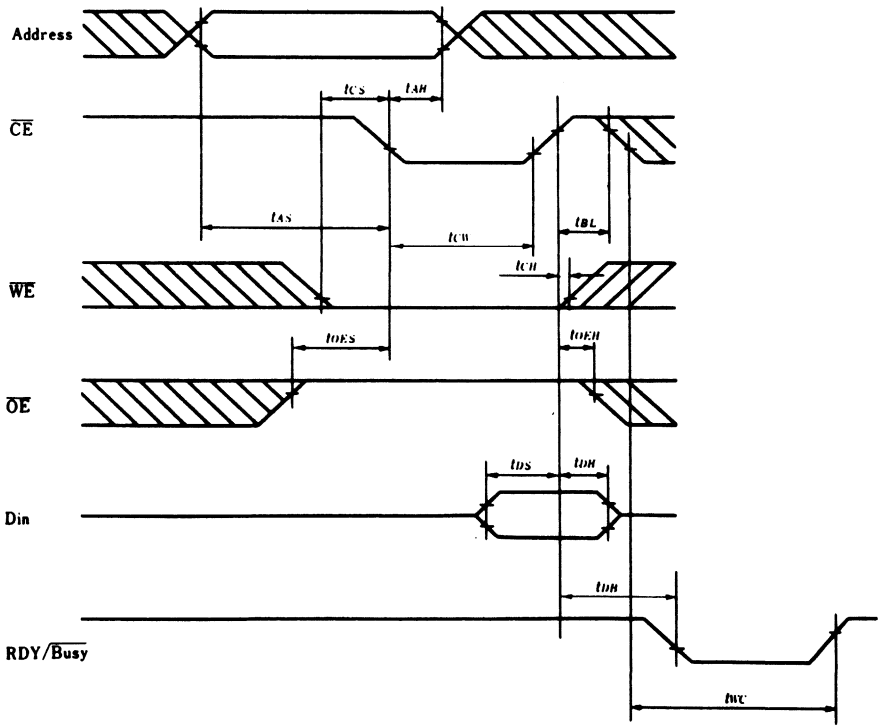
- **Byte Erase and Byte Write Operation** ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	μs



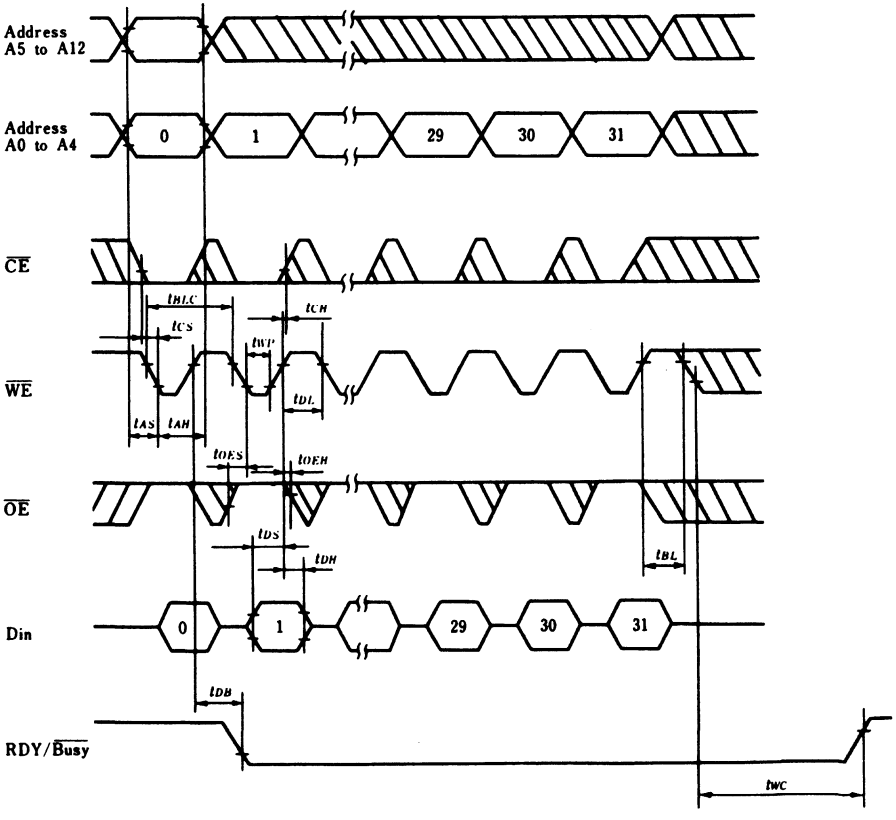
● **Byte Erase and Byte Write Operation** ($\overline{CE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	μs



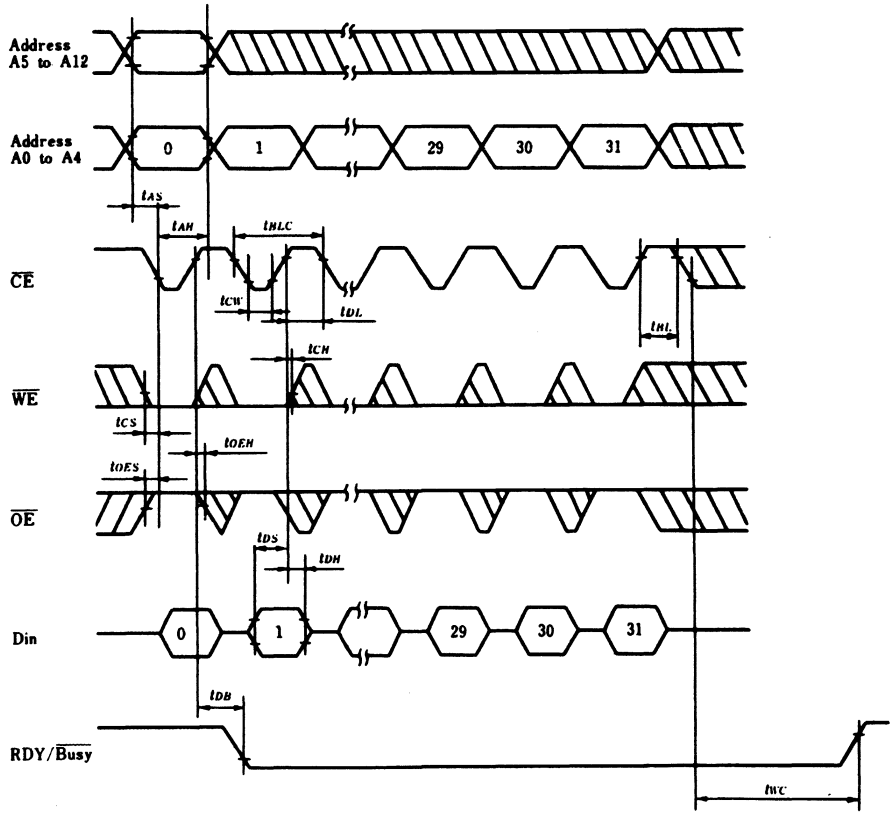
- **Page Erase and Page Write Operation** ($\overline{WE}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
Write Pusle Width	t_{WP}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	µs
Byte Load Cycle	t_{BLC}	0.3	–	30	µs



● **Page Erase and Page Write Operation** ($\overline{CE}$ Controlled Write Cycle)

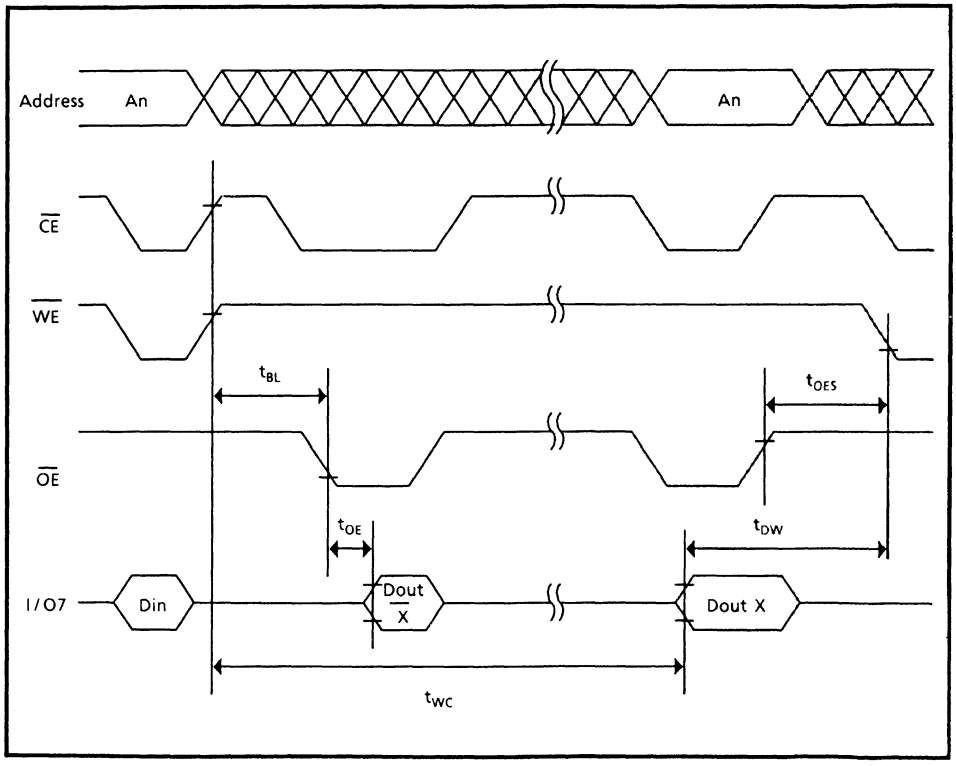
Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	–	–	ns
$\overline{CE}$ to Write Setup Time	t_{CS}	0	–	–	ns
$\overline{CE}$ Pulse Width	t_{CW}	200	–	–	ns
Address Hold Time	t_{AH}	150	–	–	ns
Data Setup Time	t_{DS}	100	–	–	ns
Data Hold Time	t_{DH}	20	–	–	ns
$\overline{CE}$ Hold Time	t_{CH}	0	–	–	ns
$\overline{OE}$ to Write Setup Time	t_{OES}	0	–	–	ns
$\overline{OE}$ Hold Time	t_{OEH}	0	–	–	ns
Data Latch Time	t_{DL}	100	–	–	ns
Time to Device Busy	t_{DB}	120	–	–	ns
Write Cycle Time	t_{WC}	–	–	10	ms
Byte Load Window	t_{BL}	100	–	–	μs
Byte Load Cycle	t_{BLC}	0.3	–	30	μs



- **Data Polling Operation**

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Byte load window	t_{BL}	100	—	—	µs	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
Write start time	t_{DW}	150	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
$\overline{OE}$ to output delay	t_{OE}	10	—	90	ns	

- **Wave Form**



- **Automatic Page Write**

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30μs of the preceding rising edge of the $\overline{WE}$.

- **$\overline{DATA}$ Polling**

$\overline{Data}$ polling allows comparison operation to determine the status of the EEPROM. During a write cycle, an attempted read of the last byte written in the EEPROM results in the complement data of that byte at I/O7.

- **RDY/$\overline{Busy}$ Signal**

RDY/$\overline{Busy}$ signal can be also used to determine the status of the EEPROM. The RDY/$\overline{Busy}$ signal has high impedance, except in a write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

- **$\overline{WE}$, $\overline{CE}$ Pin Operation**

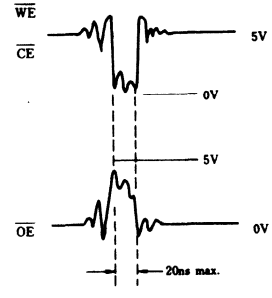
During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$ and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

- **Data Protection**

To protect the data during operation and power on/off, the HN58C65 has the internal functions described below.

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.
To prevent this phenomenon, the HN58C65 has the noise cancelation function of that cuts the noise if its width is 20ns or less in program mode.
Be careful not to allow noise of a width of more than 20ns on the control pins.



2. Data Protection at V_{CC} On/Off

2-1 Prevention of unintentional programming at V_{CC} on/off.

When V_{CC} is turned on or off, the noise on the control pins generated by external circuits (CPU, etc.) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

In addition, when V_{CC} is turned on or off, the input level of on control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	X	X
$\overline{OE}$	X	V_{SS}	X
$\overline{WE}$	X	X	V_{CC}

X: Don't care.

HN58C66 Series

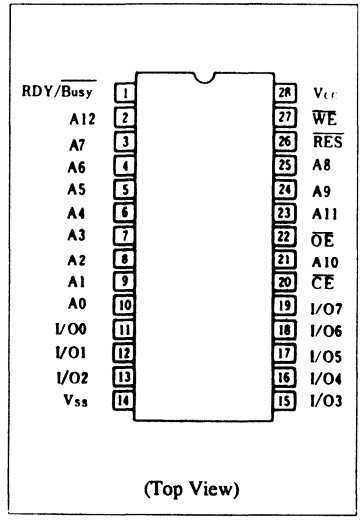
8192-Word × 8-Bit CMOS Electrically Erasable and Programmable ROM

The Hitachi HN58C66 is a 64k CMOS EEPROM (electrically erasable and programmable ROM), featuring data protection by program reset. It realizes low power consumption (60 mW typ) and a high level of reliability (10^5 erase/write cycles and 10 year data retention), employing MNOS memory technology and CMOS process and circuitry technology. No external circuit for data protection is required since a program reset function is added, so its system design is easy. It is suitable for IC cards and memory cards.

Features

- Single 5 V supply
- On chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (32 bytes): 10 ms max
- High speed: Access time 250 ns max
- Low power dissipation
  - Active mode: 20 mW/MHz typ
  - Standby mode: 2 mW typ
- $\overline{Data}$ polling and RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10-year data retention
- Program reset by $\overline{RES}$

Pin Arrangement



(Top View)

Ordering Information

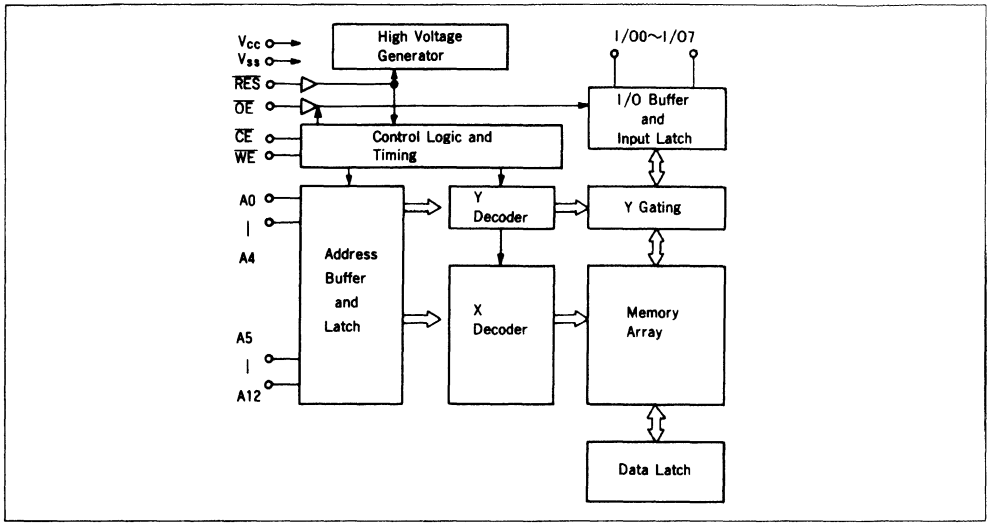
Type No.	Access Time	Package
HN58C66P-25	250 ns	600-mil 28-pin plastic DIP (DP-28)
HN58C66FP-25	250 ns	28-pin plastic SOP*1 (FP-28D/DA)

Note: T is added to the end of the type no. for an SOP of 3.00 mm (max) thickness.

Pin Description

Pin Name	Function
A0–A12	Address
I/O0–I/O7	Input/Output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
Vcc	Power supply (+5 V)
Vss	Ground
RDY/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Program reset

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	RDY/$\overline{Busy}$ (1)	$\overline{RES}$ (26)	I/O (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	V_H*1	Dout
Standby	V_{IH}	×	×	High-Z	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z→V_{OL}	V_H	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write inhibit	×	×	V_{IH}	High-Z	×	—
	×	V_{IL}	×	High-Z	×	—
Data polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	V_H	Data out (I/O7)
Program reset	×	×	×	High-Z	V_{IL}	High-Z

Notes: *1. Refer to the recommended DC operating condition.
*2. × = Don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage*1	Vcc	–0.6 to +7.0	V
Input voltage*1	Vin	–0.5*2 to +7.0	V
Operating temperature range*3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: *1. Relative to Vss
*2. Vin min = –3.0 V for pulse width ≤ 50 ns
*3. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 1	V
	V_H	V_{CC}–0.5	—	V_{CC} + 1	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10 %)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2 *1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC2}	—	—	8	mA	Iout = 0 mA, duty = 100% cycle = 1µs
		—	—	25	mA	Iout = 0 mA, duty = 100% maximum cycle
Input low voltage	V_{IL}	–0.3 *2	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 1	V	
	V_H	V_{CC} – 0.5	—	V_{CC} + 1	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes : *1. I_{LI} on $\overline{RES}$ = 100 µA max.
*2. V_{IL} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

AC Characteristics (Ta = 0 to + 70°C, V_{CC} = 5 V ± 10%)

Test Conditions

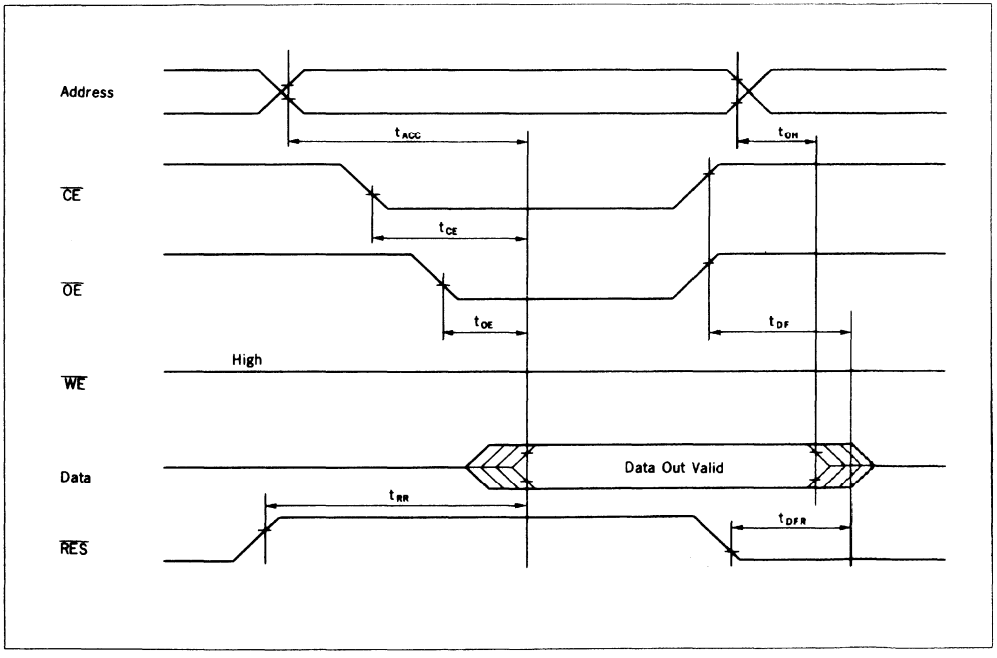
Input pulse levels: 0.4 V to 2.4 V
Input rise and fall time: ≤ 20 ns

Output load: 1TTL Gate + 100 pF
Reference levels for measuring timing:
Inputs; 0.8 V and 2.0 V
Outputs; 0.8 V and 2.0 V

Read Cycle

Item	Symbol	Min	Max	Unit	Test Conditions
Address to output delay	t_{ACC}	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	—	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	—	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

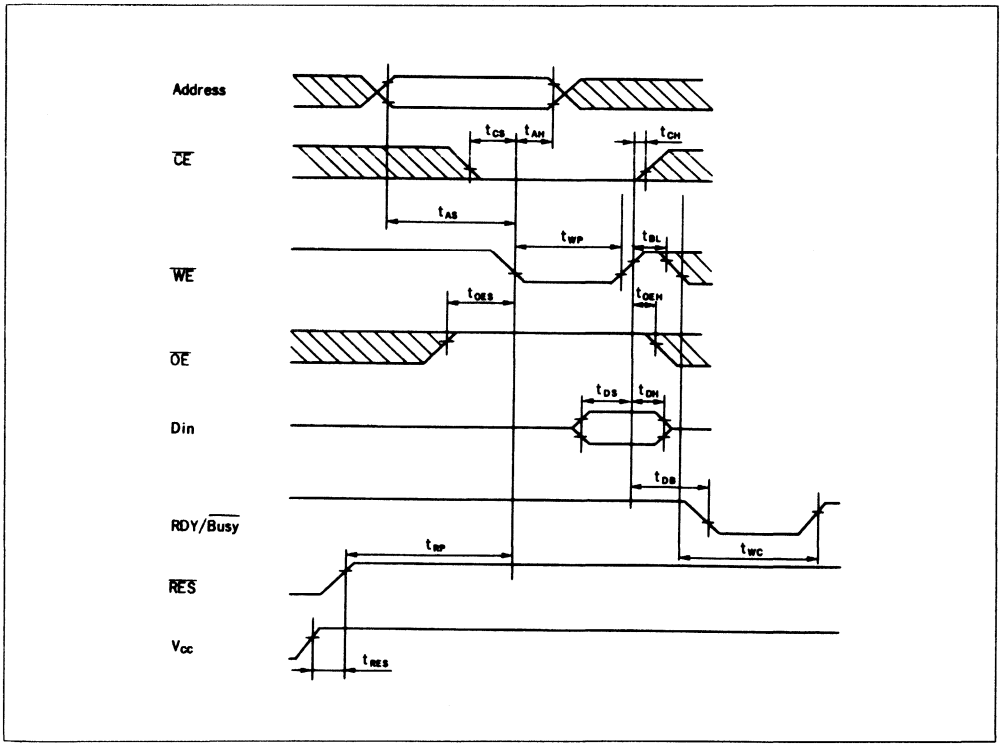
Read Timing Waveform



Byte Erase and Byte Write Cycle ($\overline{WE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{WP}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

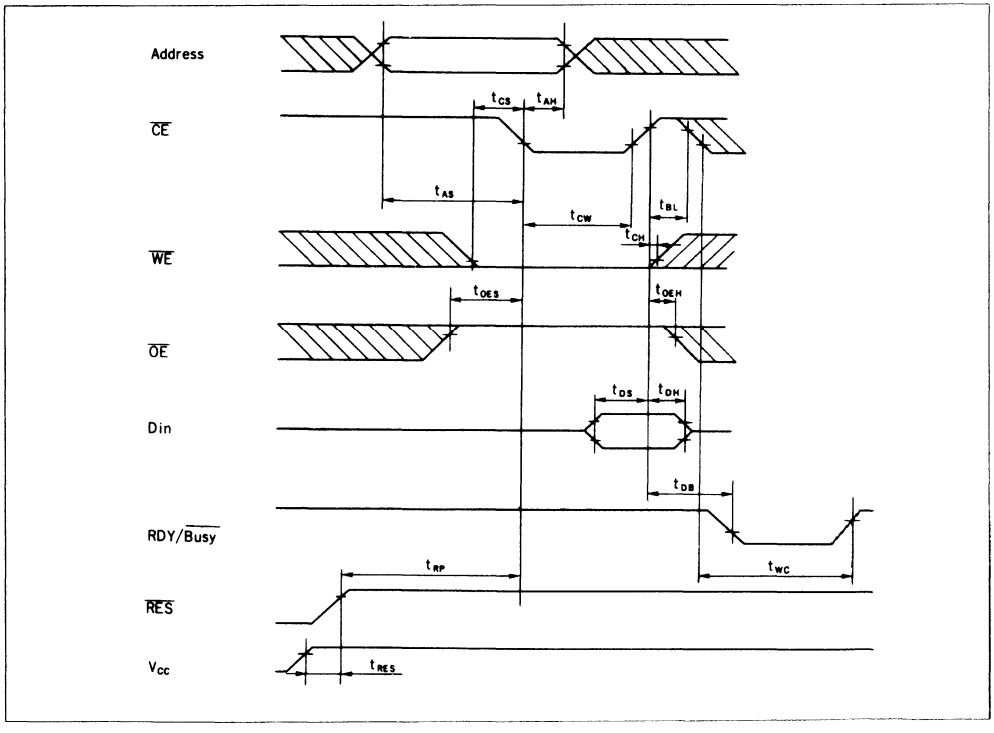
Byte Erase and Byte Write Timing Waveform (1) ($\overline{WE}$ controlled)



Byte Erase and Byte Write Cycle ($\overline{CE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{CW}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

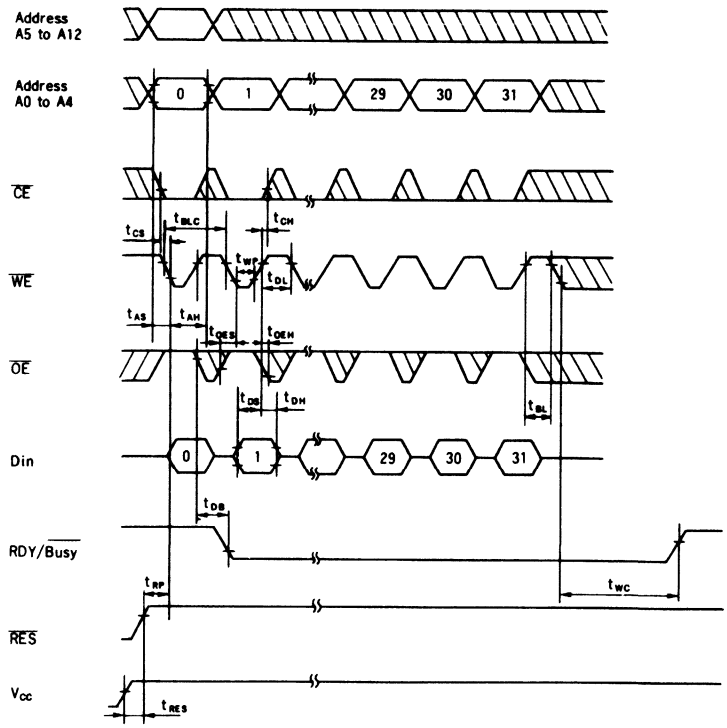
Byte Erase and Byte Write Timing Waveform (2) ($\overline{CE}$ controlled)



Page Erase and Page Write Cycle ($\overline{WE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{CW}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Data latch time	t_{DL}	100	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Byte load cycle	t_{BLC}	0.3	—	30	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

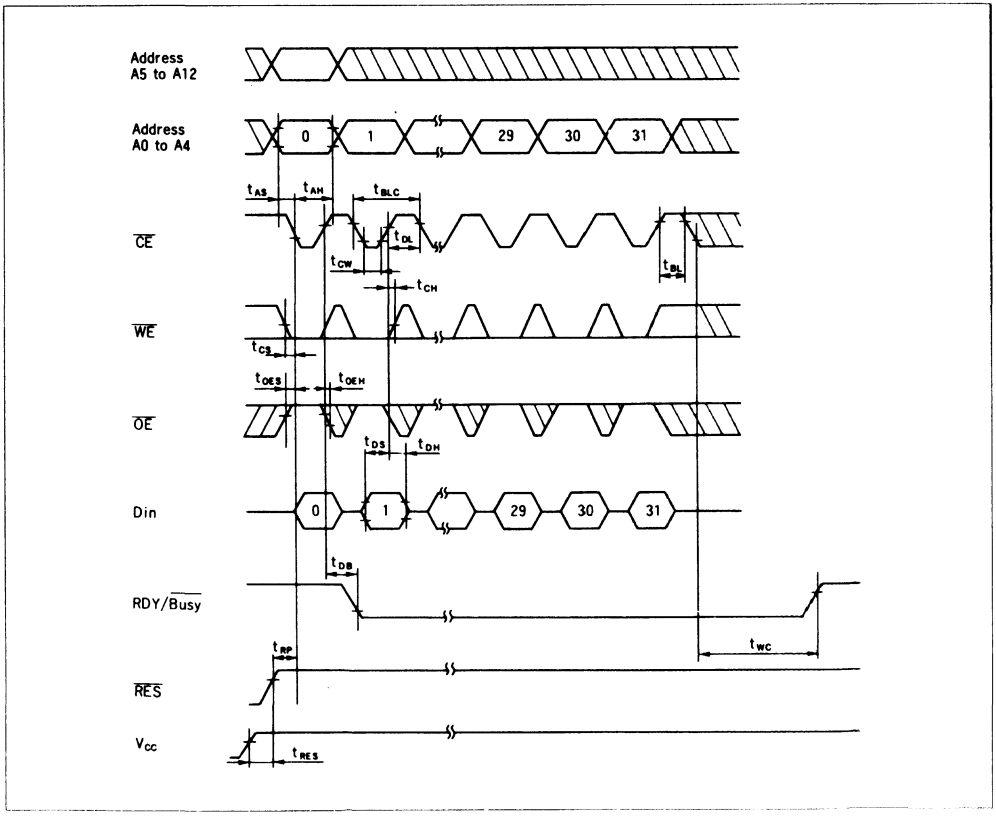
Page Erase and Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Erase and Page Write Cycle ($\overline{CE}$ Controlled)

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	0	—	—	ns
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns
Write pulse width	t_{CW}	200	—	—	ns
Address hold time	t_{AH}	150	—	—	ns
Data setup time	t_{DS}	100	—	—	ns
Data hold time	t_{DH}	20	—	—	ns
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns
Data latch time	t_{DL}	100	—	—	ns
Time to device busy	t_{DB}	120	—	—	ns
Write cycle time	t_{WC}	—	—	10	ms
Byte load window	t_{BL}	100	—	—	µs
Byte load cycle	t_{BLC}	0.3	—	30	µs
Reset protect time	t_{RP}	100	—	—	µs
Reset high time	t_{RES}	1	—	—	µs

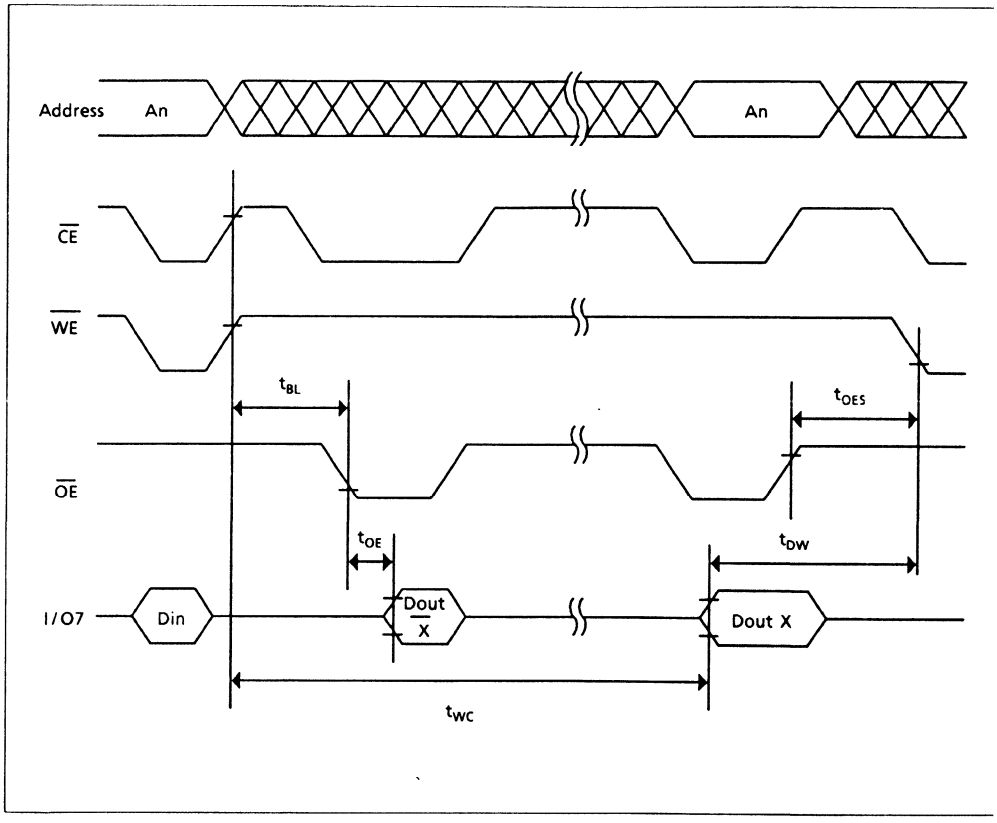
Page Erase and Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Data Polling Operation

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Byte load window	t_{BL}	100	—	—	µs	
$\overline{OE}$ to write set up time	t_{OES}	0	—	—	ns	
Write start time	t_{DW}	150	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
$\overline{OE}$ to output delay	t_{OE}	10	—	90	ns	

Wave Form



Functional Description

*** Automatic Page Write**

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. Data can be written and accessed 10^5 times per page. Therefore, page write allows the data to be written 10^5 times in 32-byte units, 2×10^5 times in 16-byte units, or 4×10^5 times in 8-byte units.

*** $\overline{Data}$ Polling**

$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

*** RDY/$\overline{Busy}$ Signal**

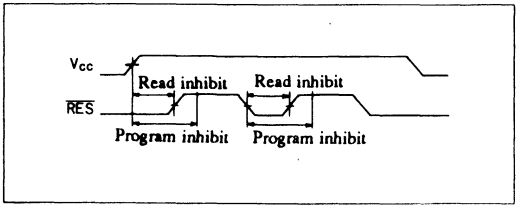
RDY/$\overline{Busy}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

*** $\overline{WE}$, $\overline{CE}$ Pin Operation**

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

*** $\overline{RES}$ Signal**

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when Vcc is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



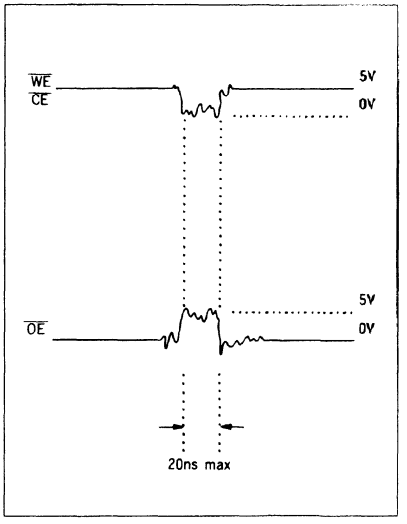
*** Data Protection**

Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.

To prevent this phenomenon, the HN58C66 has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



HN58C256 Series

32768-Word × 8-Bit Electrically Erasable and Programmable CMOS ROM

The Hitachi HN58C256 is an electrically erasable and programmable ROM organized as 32768-word × 8-bit. It realizes high speed, low power consumption, and a high reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64–byte page reprogramming function to make its erase and write operations faster.

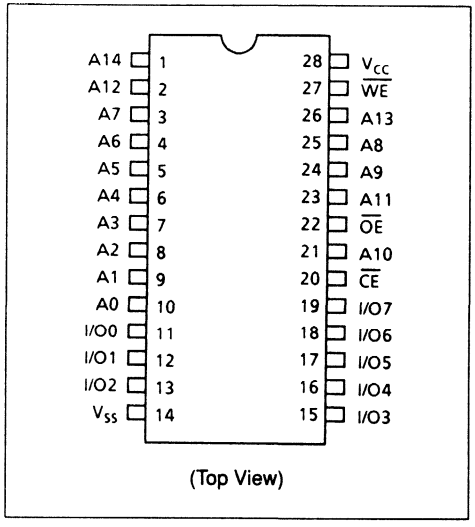
Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 200 ns max
- Low power dissipation: 20 mW/MHz, typ (Active)
  100 µW max (Standby)
- $\overline{\text{Data}}$ polling
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology

Ordering Information

Type no.	Access time	Package
HN58C256P-20	200 ns	600-mil 28-pin plastic DIP (DP-28)
HN58C256FP-20	200 ns	28-pin plastic SOP (FP-28D)

Pin Arrangement

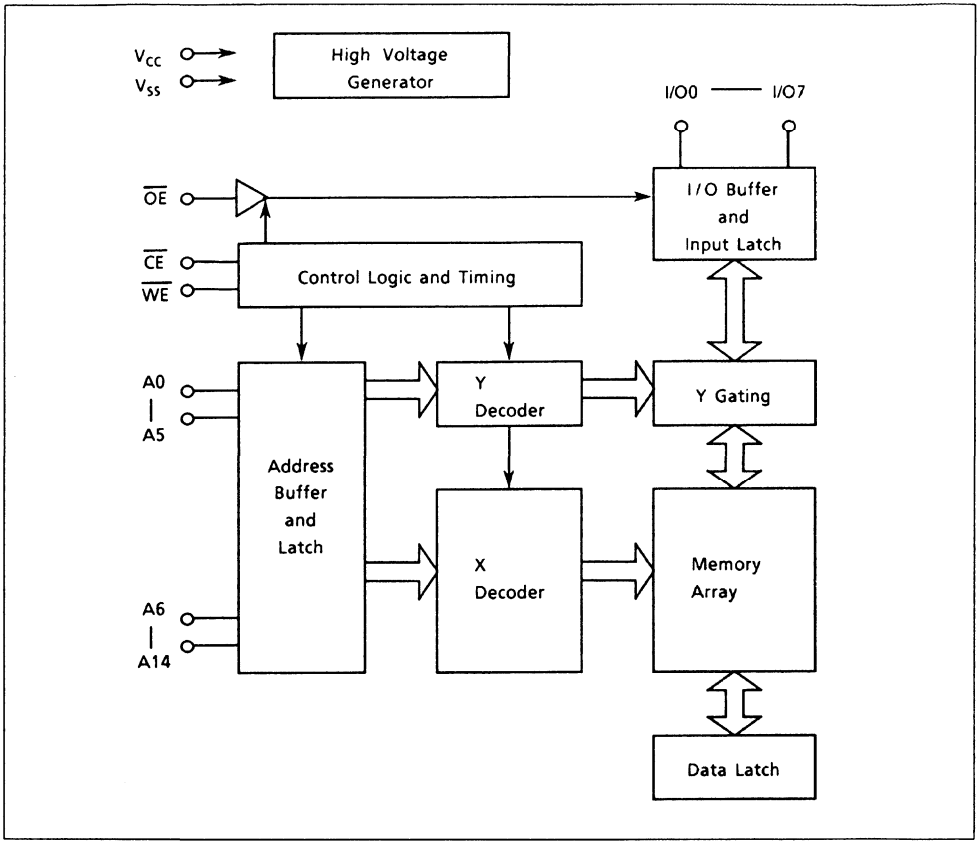


(Top View)

Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)
Read	V_{IL}	V_{IL}	VIH	Dout
Standby	V_{IH}	×	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z
Write inhibit	×	×	V_{IH}	—
	×	V_{IL}	×	—
DATA polling	V_{IL}	V_{IL}	V_{IH}	Data out (I/O7)

Note: × = Don't care

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns

Recommended DC Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}+1	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{IL}	—	—	2	µA	V_{CC} = 5.5 V Vin = 5.5V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V Vout = 5.5 V/0.4 V
V_{CC} current (Standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (Active)	I_{CC3}	—	—	12	mA	Iout = 0 mA Duty = 100% Cycle = 1 µs
		—	—	30	mA	Iout = 0 mA Duty = 100% Cycle = 150 ns
Input low voltage	V_{IL}	–0.3 *1	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC+1}	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Note: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vin = 0 V

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

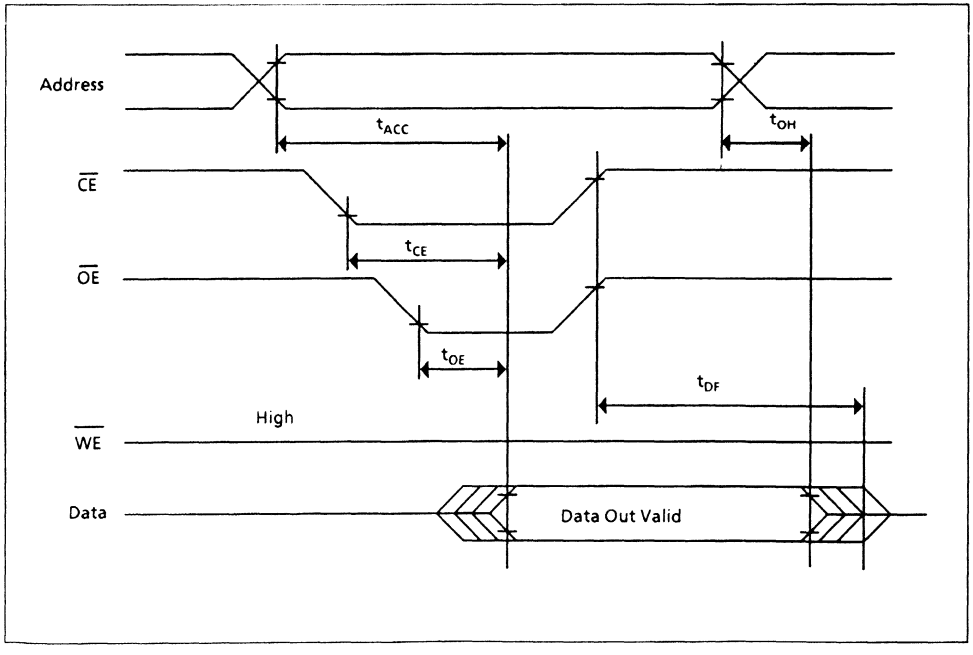
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: ≤ 20 ns
- Output load: 1TTL gate + 100 pF
- Reference levels for measuring timing:
  inputs; 0.8 V and 2.0 V
  outputs; 0.8 V and 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DF}	0	70	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

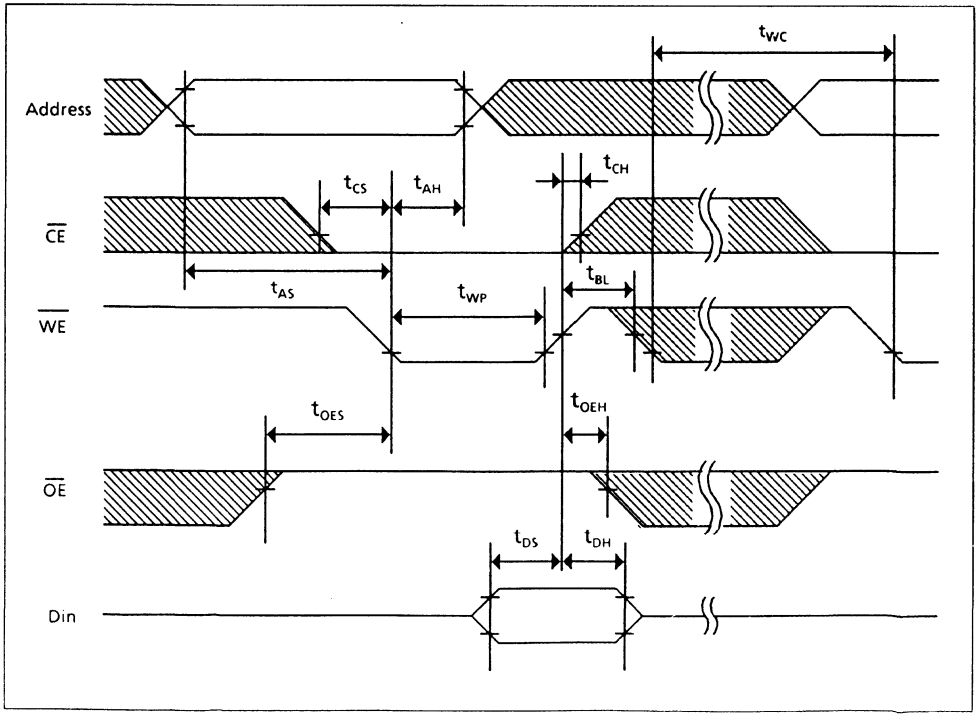
Read Timing Waveform



Byte Erase and Byte Write Cycle ($\overline{WE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{WP}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	

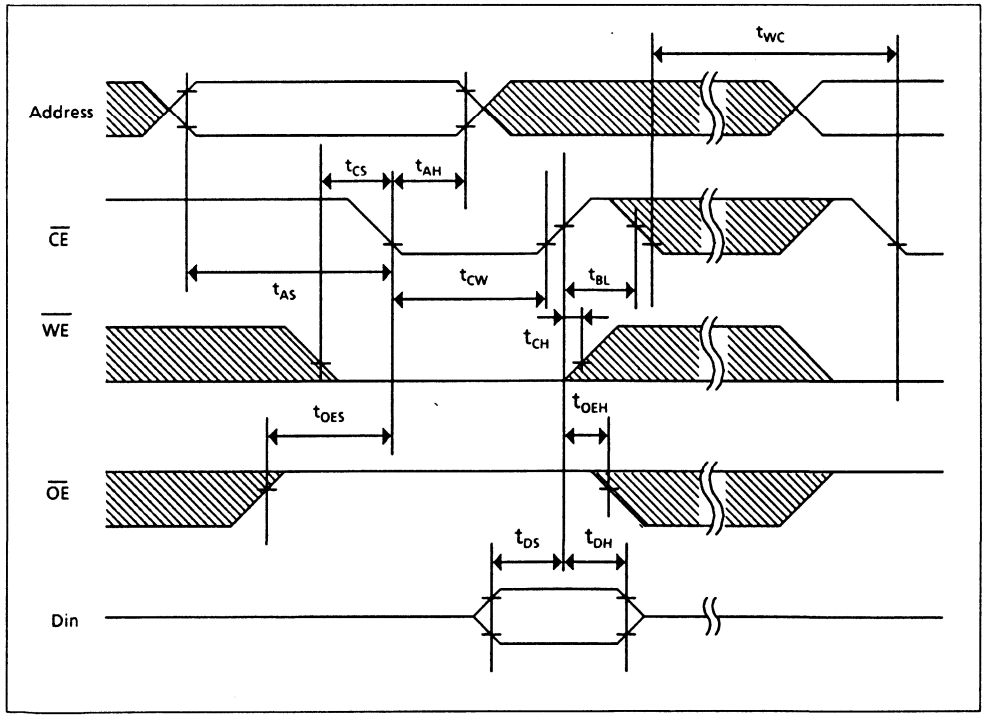
Byte Erase and Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Byte Erase and Byte Write Cycle ($\overline{CE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{CW}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	

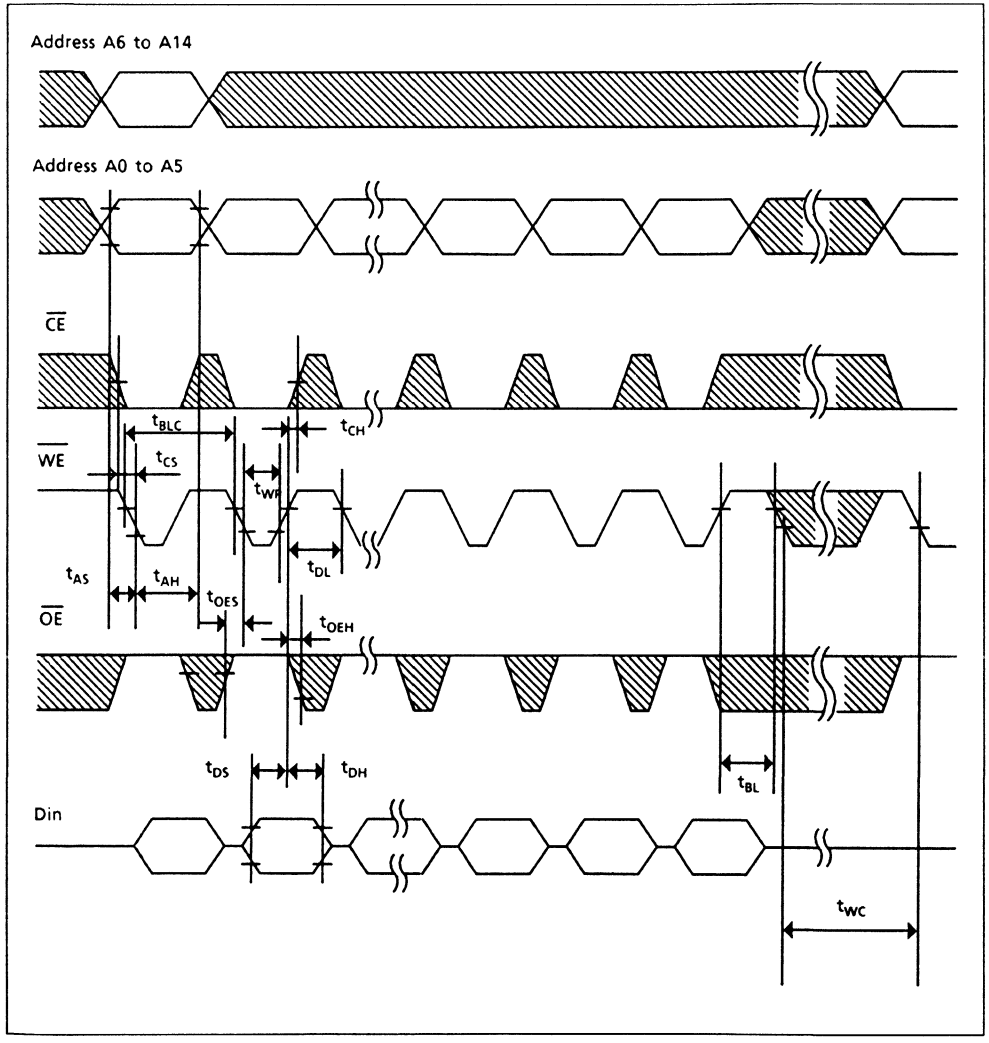
Byte Erase and Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Page Erase and Page Write Cycle ($\overline{WE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{WP}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data latch time	t_{DL}	200	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Byte load cycle	t_{BLC}	0.3	—	30	µs	

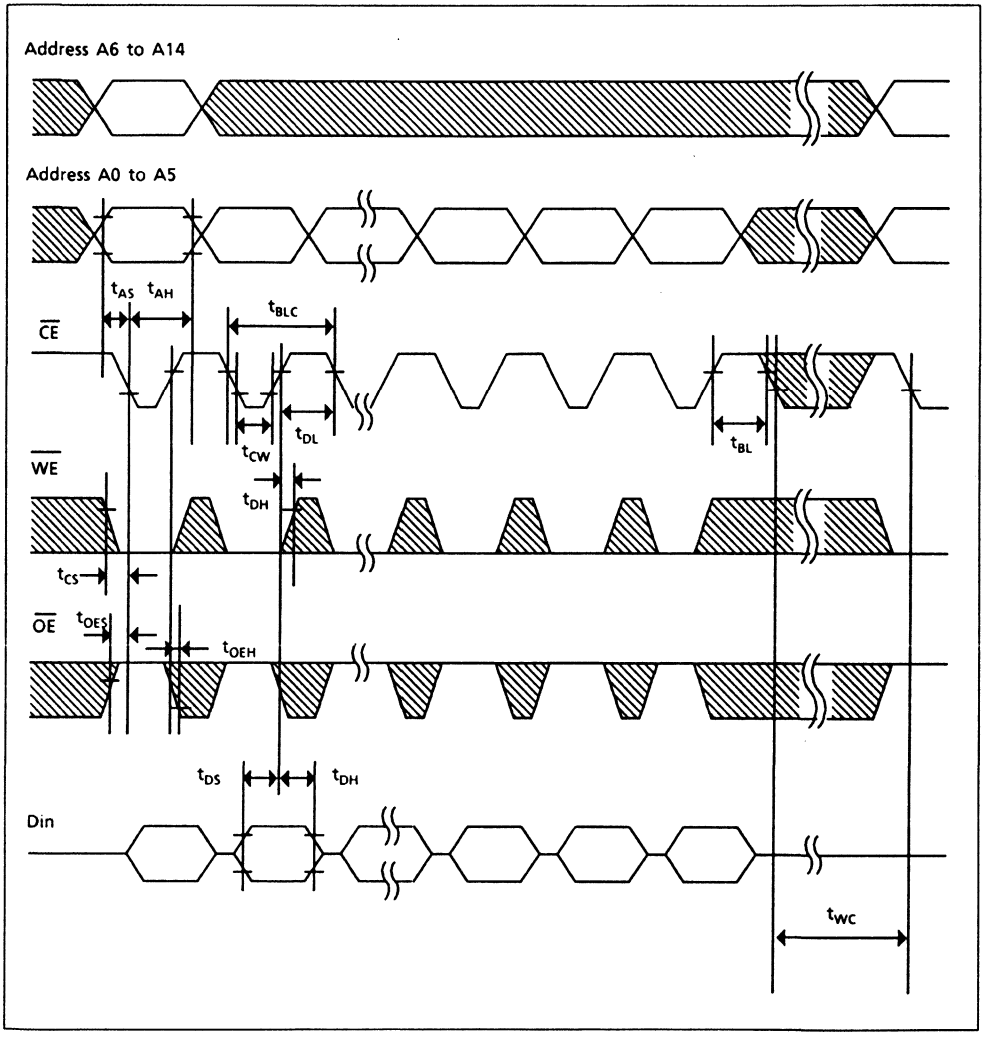
Page Erase and Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Erase and Page Write Cycle ($\overline{CE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{CW}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data latch time	t_{DL}	200	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Byte load cycle	t_{BLC}	0.3	—	30	µs	

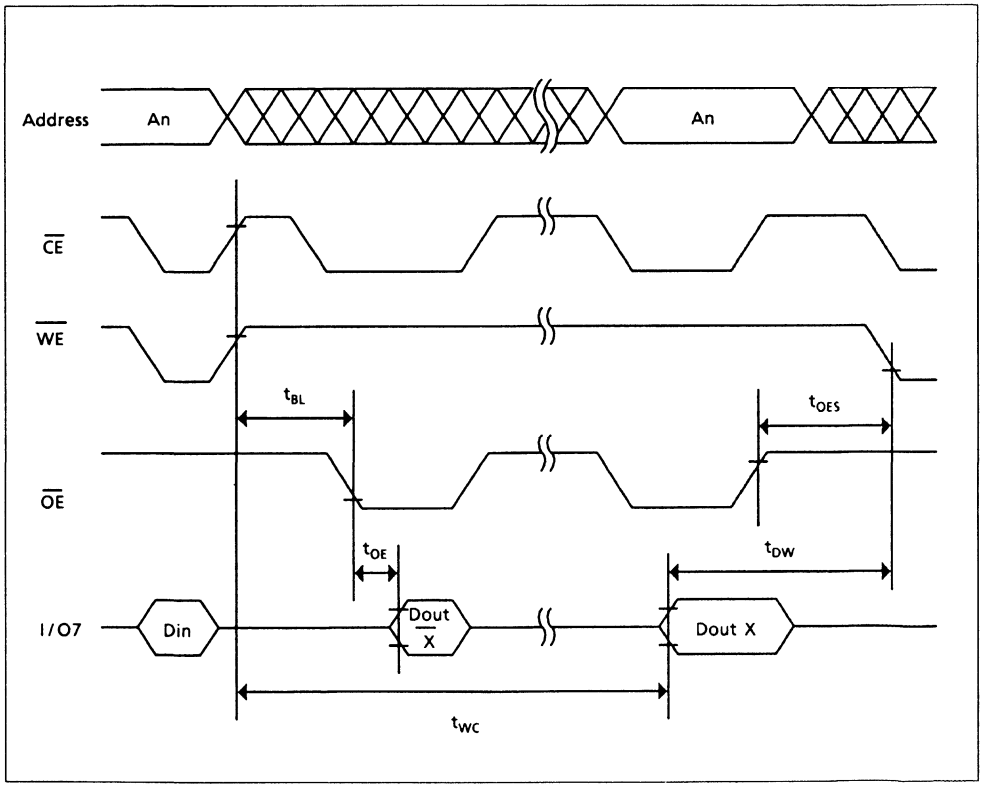
Page Erase and Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Cycle

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Byte load window	t_{BL}	100	—	—	µs	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
Write start time	t_{DW}	150	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
$\overline{OE}$ to output delay	t_{OE}	10	—	90	ns	

$\overline{\text{Data}}$ Polling Timing Waveform



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μs of the preceding rising edge of the $\overline{WE}$. When $\overline{CE}$ or $\overline{OE}$ is high for 100 μs after data input, the EEPROM enters erase and write mode automatically and only the input data are written into the EEPROM.

$\overline{Data}$ Polling

$\overline{Data}$ polling allows a comparison operation to determine the status of the EEPROM. During a write cycle, an attempted read of the last byte written in the EEPROM results in complement data of that byte at I/O7.

Write Protection

There are three features that protect the data from an inadvertent write.

- Noise protection: A write cycle will not be initiated with a $\overline{WE}$ pulse of less than 20 ns.
- V_{CC} sense: When the V_{CC} is approximately 3.0 volt, write and erase functions are not initiated.
- Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ and data is latched by the rising edge of $\overline{WE}$.

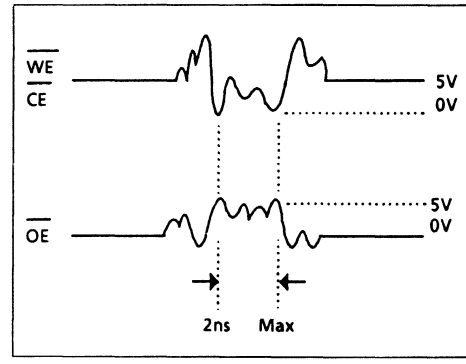
Notes on Using HN58C256

Data Protection

To protect the data during operation and power on/off, the HN58C256 has the internal functions described below.

1. Data protection against noise on control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during operation

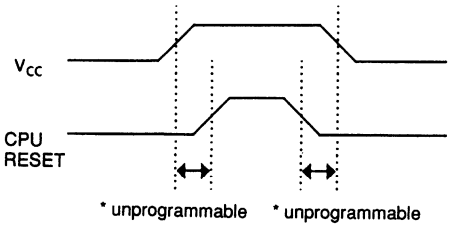
During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.
To prevent this phenomenon, the HN58C256 has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc.) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

[Example]



- The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.

In addition, when V_{CC} is turned on or off, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don't care.

HN58C257 Series — Preliminary

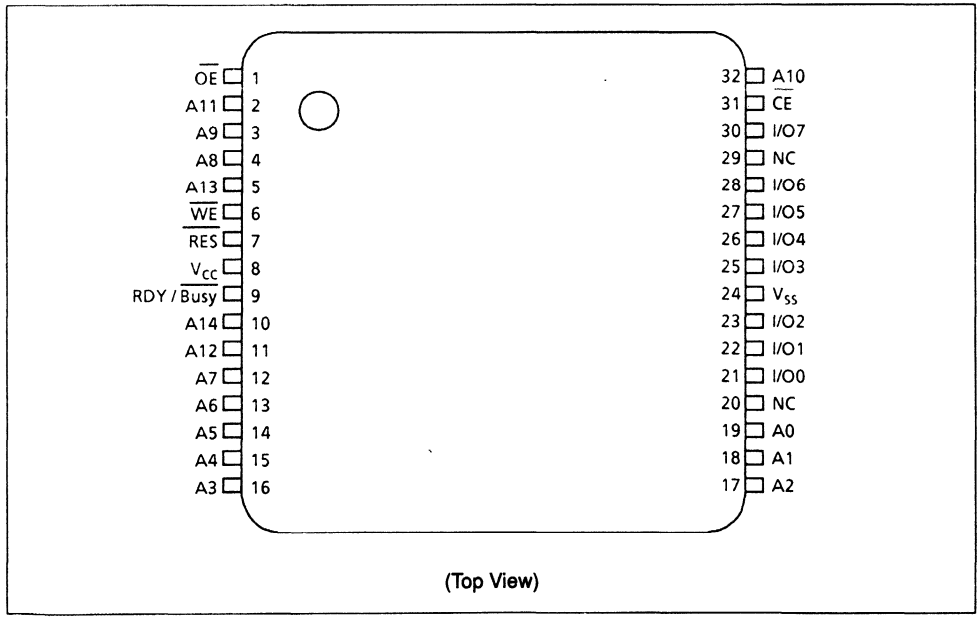
32768-Word × 8-Bit Electrically Erasable and Programmable CMOS ROM

The Hitachi HN58C257 is a electrically erasable and programmable ROM organized as 32768-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 64-byte page reprogramming function to make its erase and write operations faster.

Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 200 ns max
- Low power dissipation: 20 mW/MHz, typ (active)
  100 μW max (standby)
- $\overline{Data}$ polling and Ready/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Write protection by $\overline{RES}$ pin

Pin Arrangement



(Top View)

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

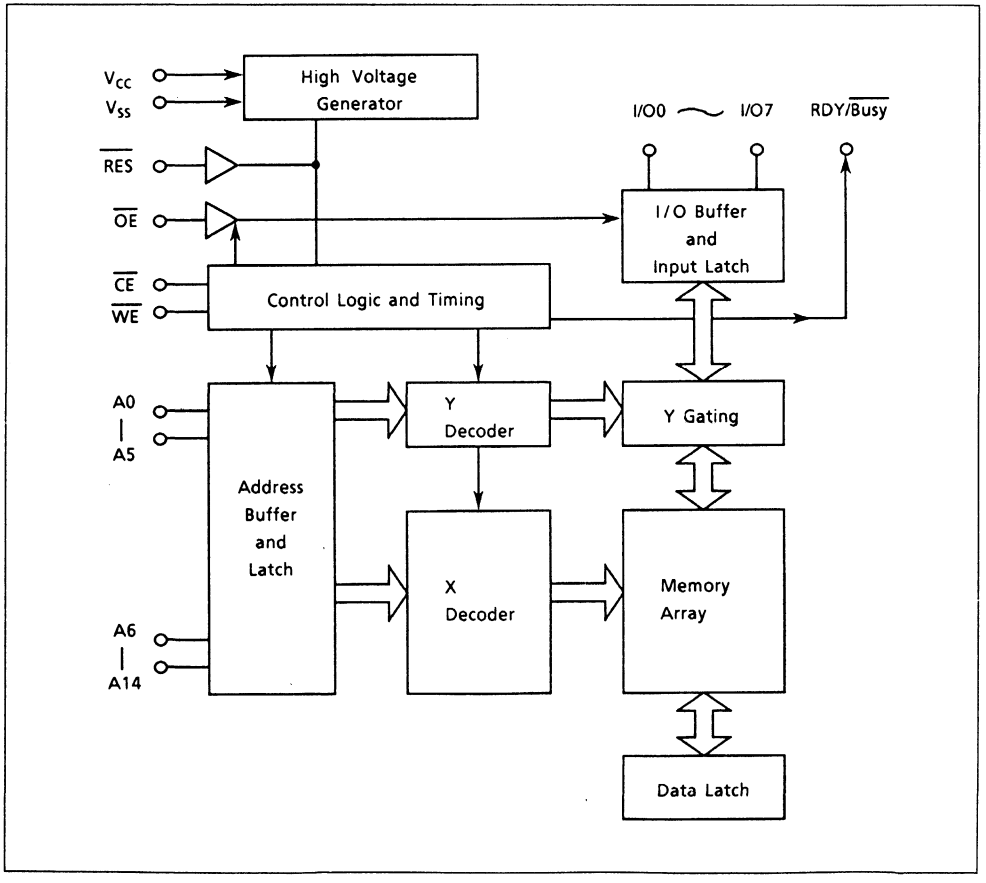
Ordering Information

Type No.	Access time	Package
HN58C257TS-20	200 ns	32-pin TSOP (TFP-32DA)

Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
$\overline{RES}$	Reset
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (31)	$\overline{OE}$ (1)	$\overline{WE}$ (6)	Ready/$\overline{Busy}$ (9)	$\overline{RES}$ (7)	I/O (21-23, 25-29)
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	V_H*1	Dout
Standby	V_{IH}	×*2	×	High-Z	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z → V_{OL}	V_H	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write inhibit	×	×	V_{IH}	High-Z	×	—
	×	V_{IL}	×			
$\overline{Data}$ polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	V_H	Data out (I/O7)
Program reset	×	×	×	High-Z	V_{IL}	High-Z

Notes: 1. Refer to the recommended DC operating condition.
2. × = Don't care

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operating temperature range	Topr*3	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}+1	V
Input voltage	V_H	V_{CC}–0.5	—	V_{CC}+1	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta=0 to +70°C, V_{CC} = 5 V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 5.5 V Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V Vout = 5.5/0.4 V
Vcc current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
Vcc current (active)	I_{CC3}	—	—	12	mA	Iout = 0 mA Duty =100% Cycle = 1 µs
		—	—	30	mA	Iout = 0 mA Duty =100% Cycle = 150 ns
Input low voltage	V_{IL}	–0.3*2	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC}+1	V	
	V_H	V_{CC}–0.5	—	V_{CC}+1	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = -400 µA

Notes: 1. I_{LI} on $\overline{RES}$ = 100 mA max
2. V_{IL} min = –1.0 V for pulse width ≤ 50 ns.

Capacitance (Ta=25°C, f=1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vin = 0 V

AC Characteristics (Ta=0 to +70°C, V_{CC}=5 V ± 10%)

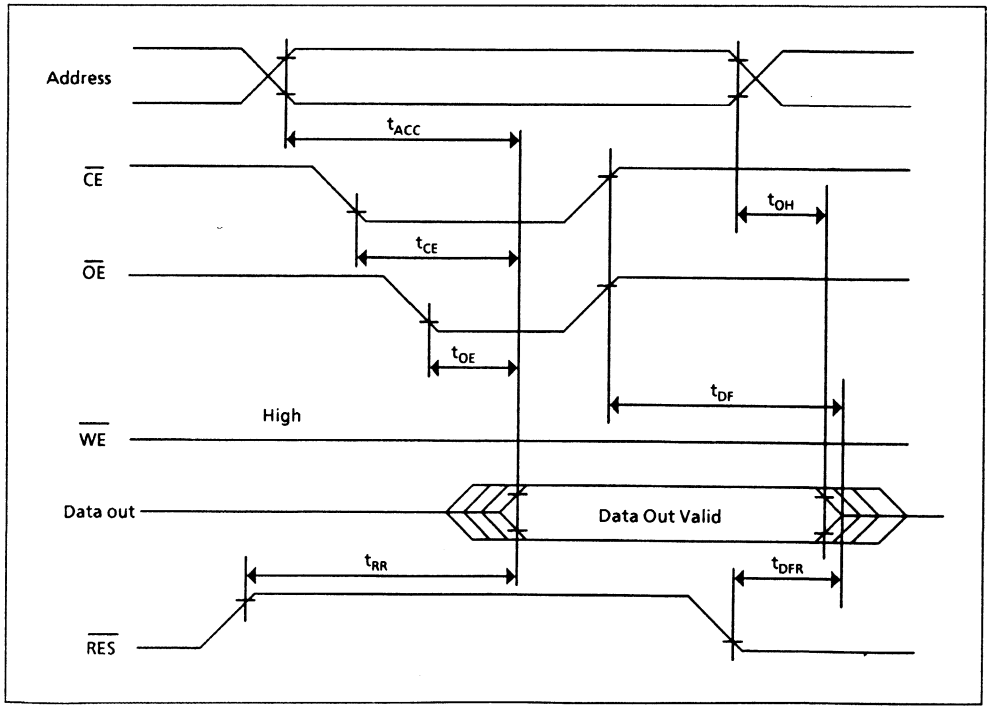
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: ≤ 20 ns
- Output load: 1TTL gate +100 pF
- Reference levels for measuring timing:
  Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	200	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DF}	0	70	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	—	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DFR}	—	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

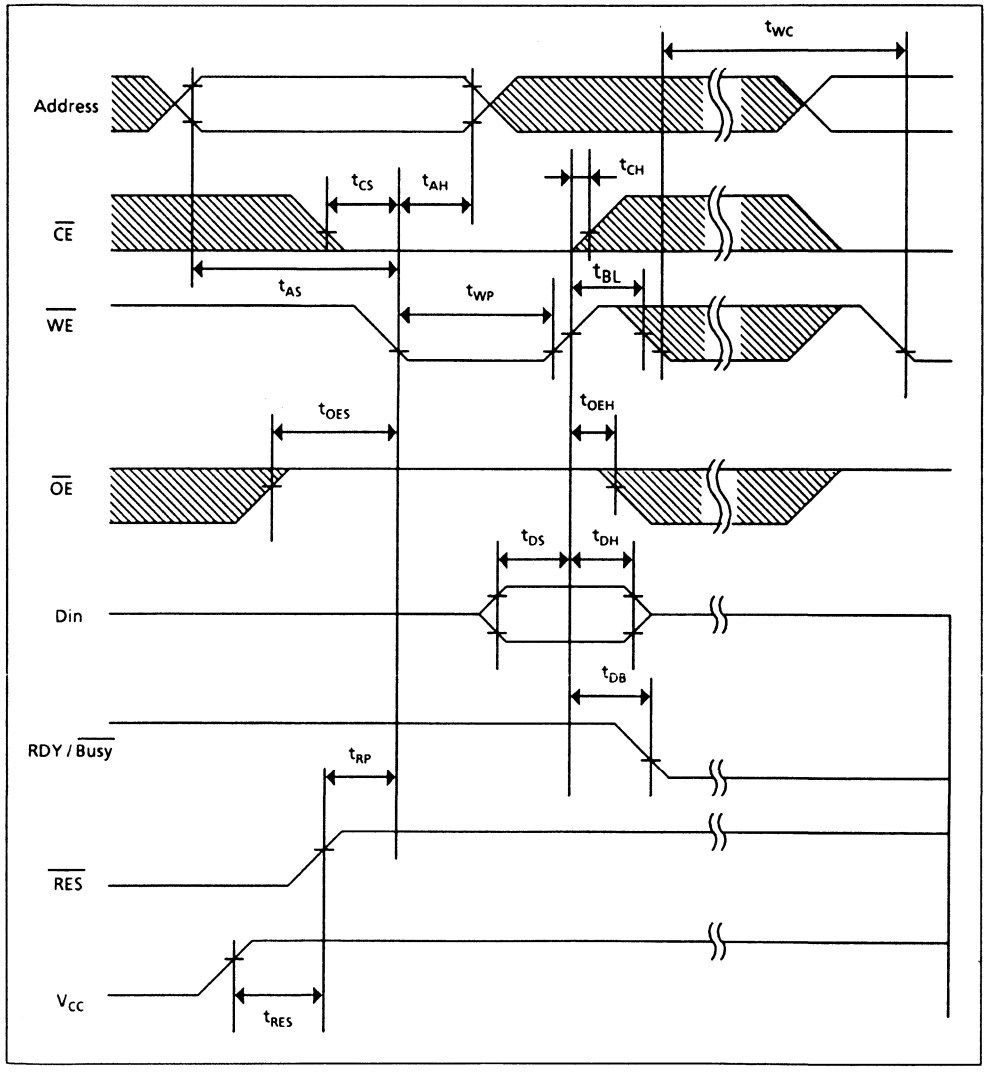
Read Timing Waveform



Byte Erase and Byte Write Cycle ($\overline{WE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{WP}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Time to device busy	t_{DB}	120	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time	t_{RES}	1	—	—	µs	

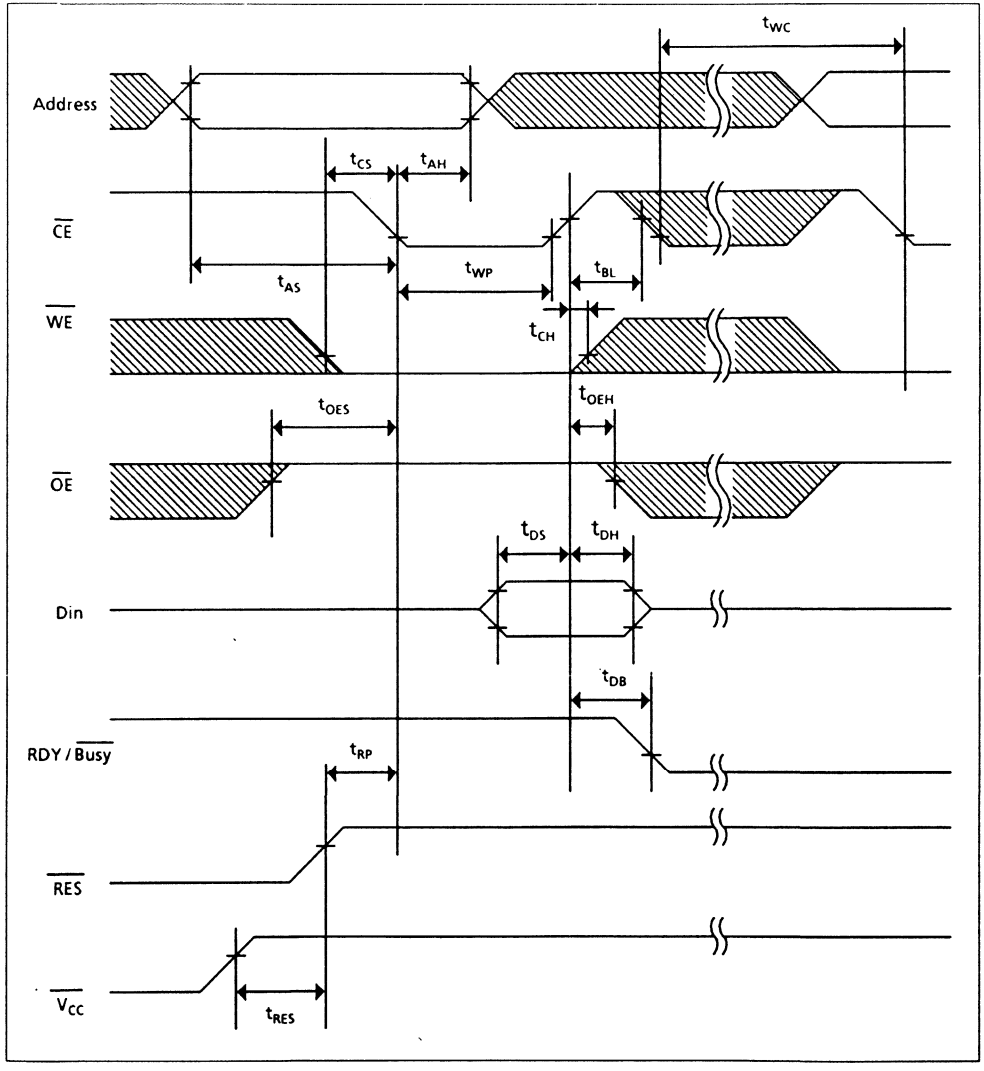
Byte Erase and Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Byte Erase and Byte Write Cycle ($\overline{CE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{CW}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Time to device busy	t_{DB}	120	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time	t_{RES}	1	—	—	µs	

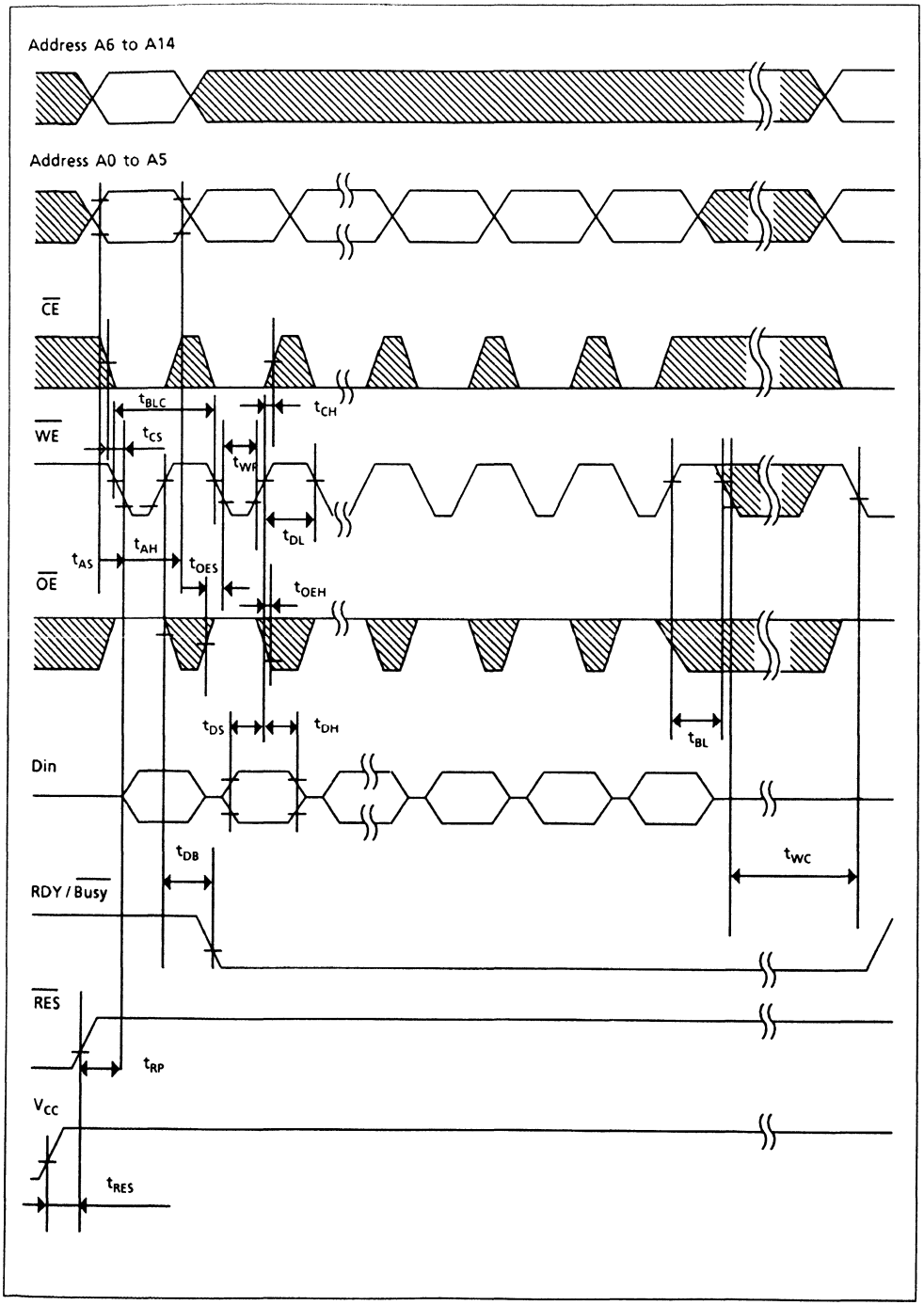
Byte Erase and Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Page Erase and Page Write Cycle ($\overline{WE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{WP}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data latch time	t_{DL}	200	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Byte load cycle	t_{BLC}	0.3	—	30	µs	
Time to device busy	t_{DB}	120	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time	t_{RES}	1	—	—	µs	

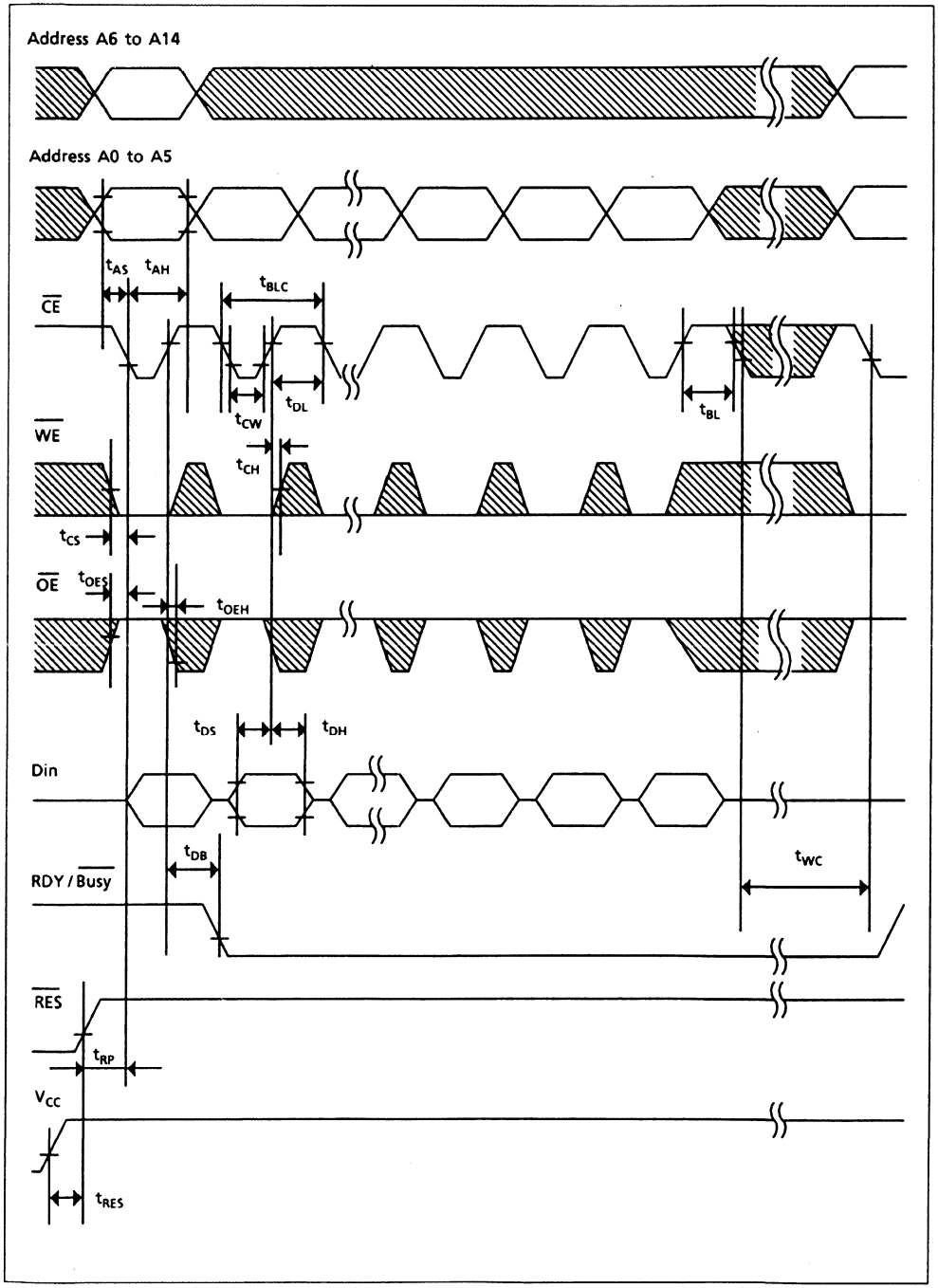
Page Erase and Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Erase and Page Write Cycle ($\overline{CE}$ Controlled)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
$\overline{CE}$ to write setup time	t_{CS}	0	—	—	ns	
Write pulse width	t_{CW}	150	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{CE}$ hold time	t_{CH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data latch time	t_{DL}	200	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
Byte load window	t_{BL}	100	—	—	µs	
Byte load cycle	t_{BLC}	0.3	—	30	µs	
Time to device busy	t_{DB}	120	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time	t_{RES}	1	—	—	µs	

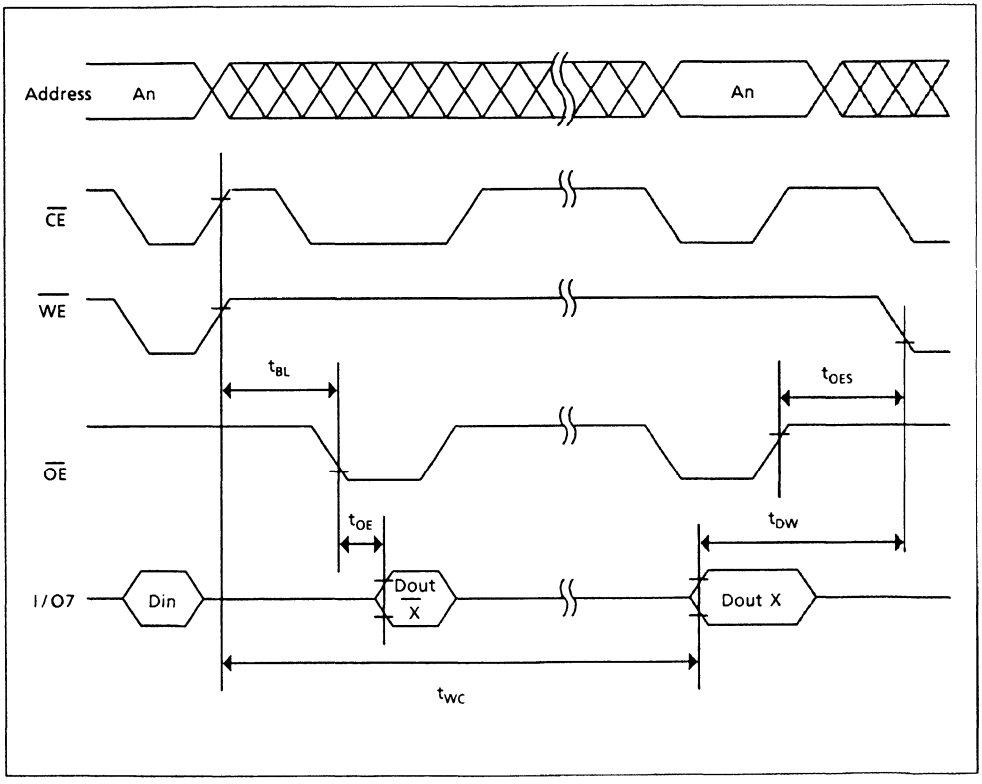
Page Erase and Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Cycle

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Byte load window	t_{BL}	100	—	—	µs	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
Write start time	t_{DW}	150	—	—	ns	
Write cycle time	t_{WC}	10	—	—	ms	
$\overline{OE}$ to output delay	t_{OE}	10	—	90	ns	

$\overline{\text{Data}}$ Polling Timing Waveform



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. Data can be written and accessed 10^5 times per page. Therefore, page write allows the data to be written 10^5 times in 64-byte units.

$\overline{Data}$ Polling

$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal

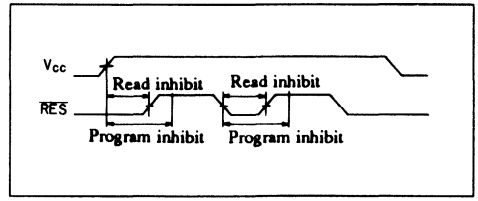
RDY/$\overline{Busy}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

$\overline{RES}$ Signal

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



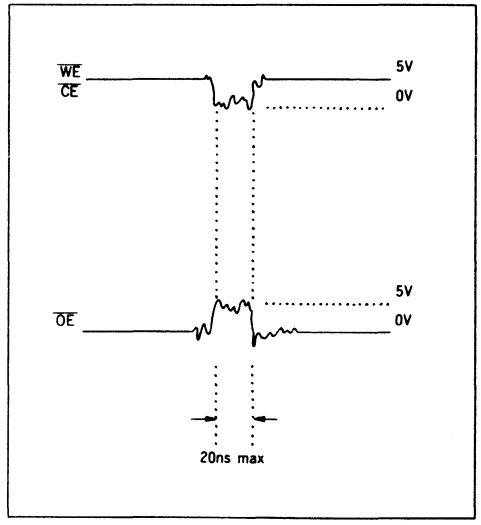
Data Protection

Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.

To prevent this phenomenon, the HN58C257 has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



HN29C101 Series — Preliminary

131072-Word × 8-Bit CMOS Flash Erase Type EEPROM

The Hitachi HN29C101 is a 131072-word × 8-bit CMOS flash erase type EEPROM, realizing on-board programming. It programs or erases data only on on-board power supply (V_{CC}/V_{PP}). The logic level of V_H (12 V) is unnecessary for address pins and control pins and command inputs are unnecessary because it provides an erase control pin ($\overline{EE}$). When erasing, its control pins, address bus and data bus become free, by control latch. It also provides the status polling function to inform the erase completion to CPU.

Features

- On-board power supply (V_{CC}/V_{PP}):
  V_{CC} = 5 V ± 10%
  V_{PP} = V_{CC} − 1 V to V_{CC} (Read)
  V_{PP} = 12.0 V ± 0.4 V (Erase/program)
- High speed: Access time 120 ns/150 ns/200 ns (max)
- Single high speed programming: Byte program
  Program time: (200 µs typ) One shot pulse
- On-board erase function: Chip erase
  Erase time: (2s typ)
  Address, data, control latch function
  Status polling function
- Low power dissipation: I_{CC} = 30 mA typ (Read)
  I_{CC} = 20 µA max (Standby)
  I_{PP} = 30 mA typ (Erase/program)
  I_{PP} = 20 µA max (Read/standby)
- Erasing endurance: More than 100 times
- Pin arrangement: 32-pin JEDEC standard
- Package: 32-pin DIP
  32-pin TSOP

Ordering Information

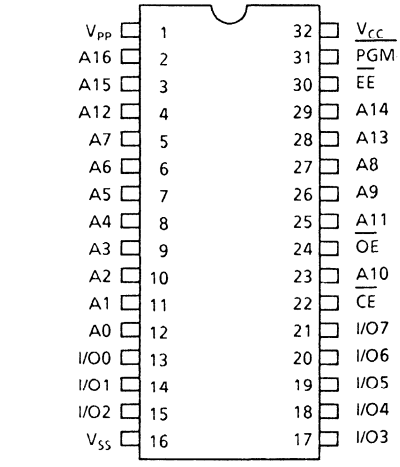
Type No.	Access time	Package
HN29C101P-12	120 ns	32-pin plastic DIP (DP-32)
HN29C101P-15	150 ns	
HN29C101P-20	200 ns	
HN29C101TS-12	120 ns	32-pin thin small outline package (TFP-32DA)
HN29C101TS-15	150 ns	
HN29C101TS-20	200 ns	

Pin Description

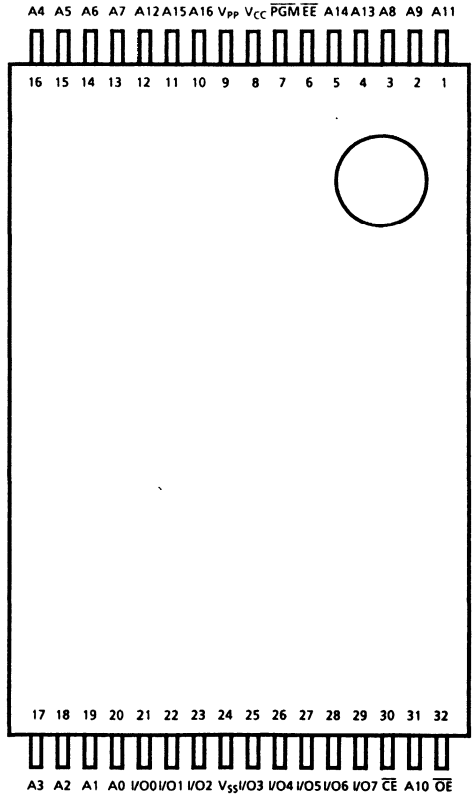
Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{PGM}$	Programming enable
$\overline{EE}$	Erase enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitach's Sales Dept. regarding specifications.

Pin Arrangement

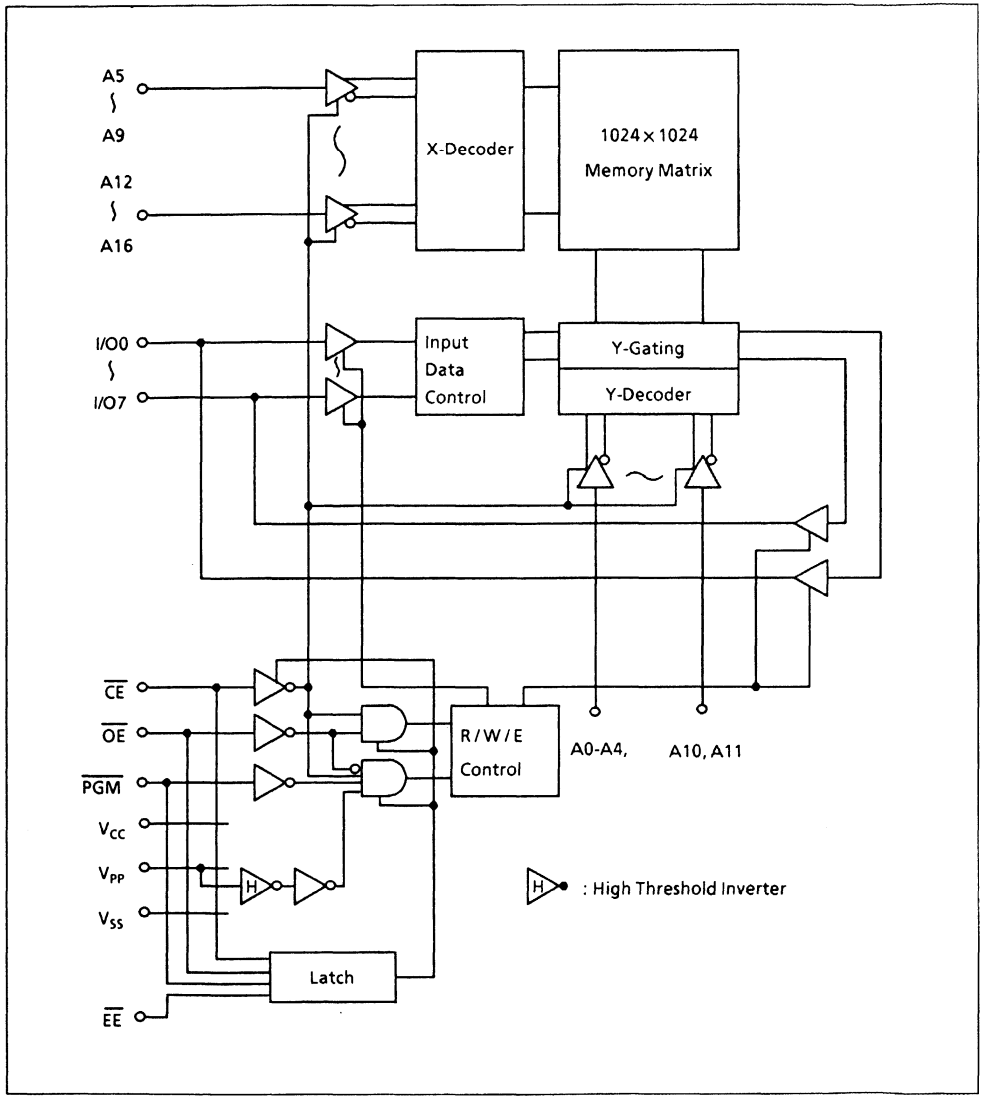


(DIP Top View)



(TSOP Top View)

Block Diagram



Mode Selection

Mode	Pin DIP TSOP	$\overline{CE}$ (22) (30)	$\overline{OE}$ (24) (32)	$\overline{PGM}$ (31) (7)	$\overline{EE}$ (30) (6)	V_{CC} (32) (8)	V_{PP} (1) (9)	Outputs (13 – 15, 17 – 21) (21 – 23, 25 – 29)
Read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	Dout
Output disable		V_{IL}	V_{IH}	×	×	V_{CC}	V_{CC}	High-Z
		V_{IL}	V_{IL}	V_{IL}	×	V_{CC}	V_{CC}	High-Z
		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{CC}	High-Z
Standby		V_{IH}	×	×	×	V_{CC}	V_{CC}	High Z
On-board program		V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	Din
On-board erase		V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	High-Z
Inhibit		V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{CC}	V_{PP}	High-Z
		V_{IL}	V_{IL}	V_{IL}	×	V_{CC}	V_{PP}	High-Z
		V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{CC}	V_{PP}	High-Z
		V_{IH}	×	×	×	V_{CC}	V_{PP}	High-Z
Erase wait		V_{IH}	×	×	×	V_{CC}	V_{PP}	High-Z
Status polling		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	I/O7 "0"→ "1"
Program verify, Erase verify		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{PP}	Dout

Note: ×: Don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages[*1]	Vin, Vout	–0.6[*2] to +7.0	V
V_{PP} voltage[*1]	V_{PP}	–0.6 to +13.0	V
V_{CC} voltage[*1]	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range[*3]	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –2.0 V for pulse width ≤ 20 ns.
3. Storage temperature range of device before programming.

Capacitance (Ta = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC} –1 V to V_{CC}, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = 0 to V_{CC}
V_{PP} current	I_{PP1}	—	—	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	—	20	µA	$\overline{CE}$ = V_{CC}
Operating V_{CC} current	I_{CC1}	—	6	15	mA	Iout = 0 mA, f = 1 MHz
	I_{CC2}	—	25	50	mA	Iout = 0 mA, f = 8 MHz
Input voltage*3	V_{IL}	–0.3*1	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} +1*2	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{IL} min = –2.0 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} +1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
3. Only defined for DC and long cycle function test.
V_{IL} max = 0.45 V, V_{IH} min = 2.4 V for AC function test.

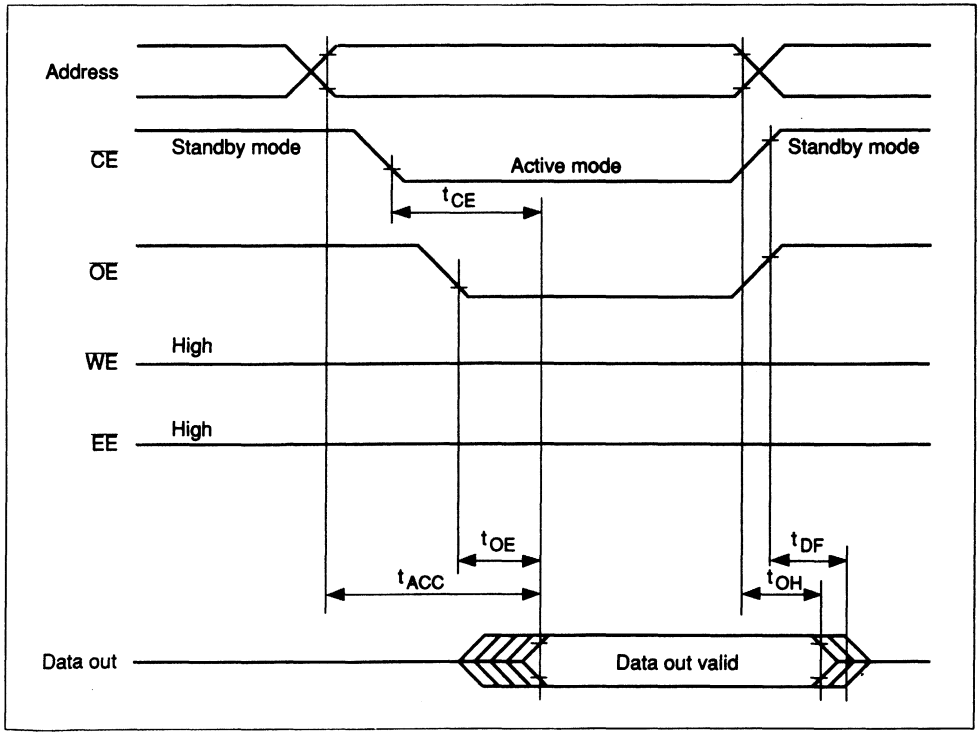
AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC} −1 V to V_{CC}, Ta = 0 to +70°C)

Test Conditions
- Input pulse levels: 0.45 V/2.4 V
- Input rise and fall times: 10 ns
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

		HN29C101-12		HN29C101-15		HN29C101-20			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Address to output delay	t_{ACC}	—	120	—	150	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	120	—	150	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	60	—	70	—	80	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float*	t_{DF}	0	40	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	—	5	—	5	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Program Operation

DC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = 12.0 V ± 0.4 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
Operating V_{CC} current	I_{CC}	—	9	30	mA	
V_{PP} supply current	I_{PP}	—	5	30	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Input voltage	V_{IL}	–0.3*4	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} +1*5	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. A influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.0 V.
4. V_{IL} min = –1.0 V for pulse width ≤ 20 ns.
5. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

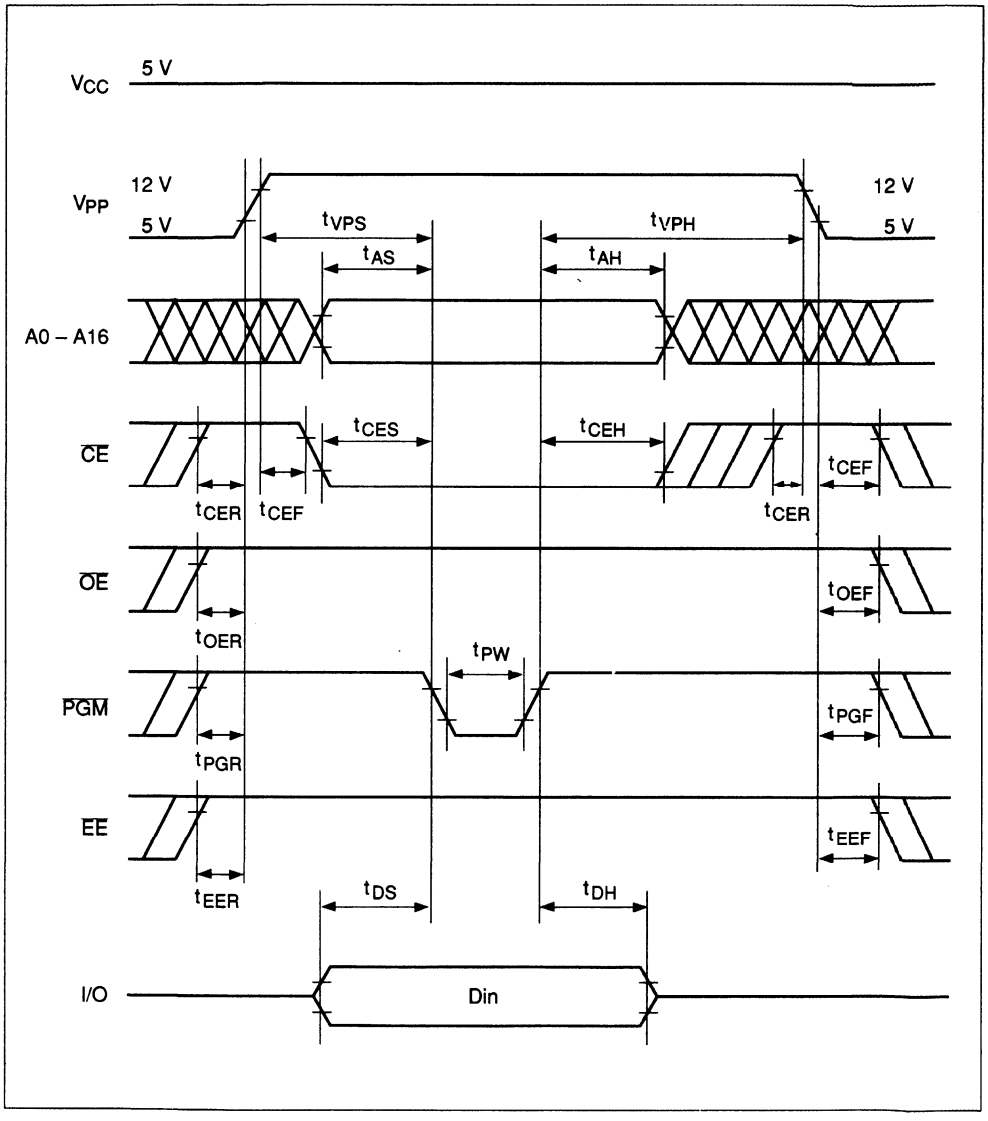
AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = 12.0 V ± 0.4 V, Ta = 0 to +70°C)

Test Condition
- Input pulse levels: 0.45 V/2.4 V
- Input rise and fall times: 10 ns
- Reference levels for measuring timing: 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	50	—	—	ns	
Chip enable setup time	t_{CES}	50	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Program pulse width	t_{PW}	190	200	210	µs	
Data hold time	t_{DH}	50	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
Chip enable hold time	t_{CEH}	50	—	—	ns	
V_{PP} setup time	t_{VPS}	100	—	—	ns	
V_{PP} hold time	t_{VPH}	100	—	—	ns	
$\overline{CE}$ setup time	t_{CER}*1	50	—	—	ns	
$\overline{OE}$ setup time	t_{OER}	50	—	—	ns	
$\overline{PGM}$ setup time	t_{PGR}*1	50	—	—	ns	
$\overline{EE}$ setup time	t_{EER}*1	50	—	—	ns	
$\overline{CE}$ hold time	t_{CEF}*1	50	—	—	ns	
$\overline{OE}$ hold time	t_{OEF}	50	—	—	ns	
$\overline{PGM}$ hold time	t_{PGF}*1	50	—	—	ns	
$\overline{EE}$ hold time	t_{EEF}*1	50	—	—	ns	

Note: 1. $\overline{CE}$, $\overline{EE}$ and $\overline{WE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.

Program Timing Waveform



Erase Operation

DC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = 12.0 V ± 0.4 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
Operating V_{CC} current	I_{CC}	—	10	40	mA	
Erase current	I_{PP}	—	35	80	mA	$\overline{CE}$ = $\overline{EE}$ V_{IL}, after control latch
Input voltage	V_{IL}	–0.3[*4]	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} +1[*5]	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. A influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.0 V.
4. V_{IL} min = –1.0 V for pulse width ≤ 20 ns.
5. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

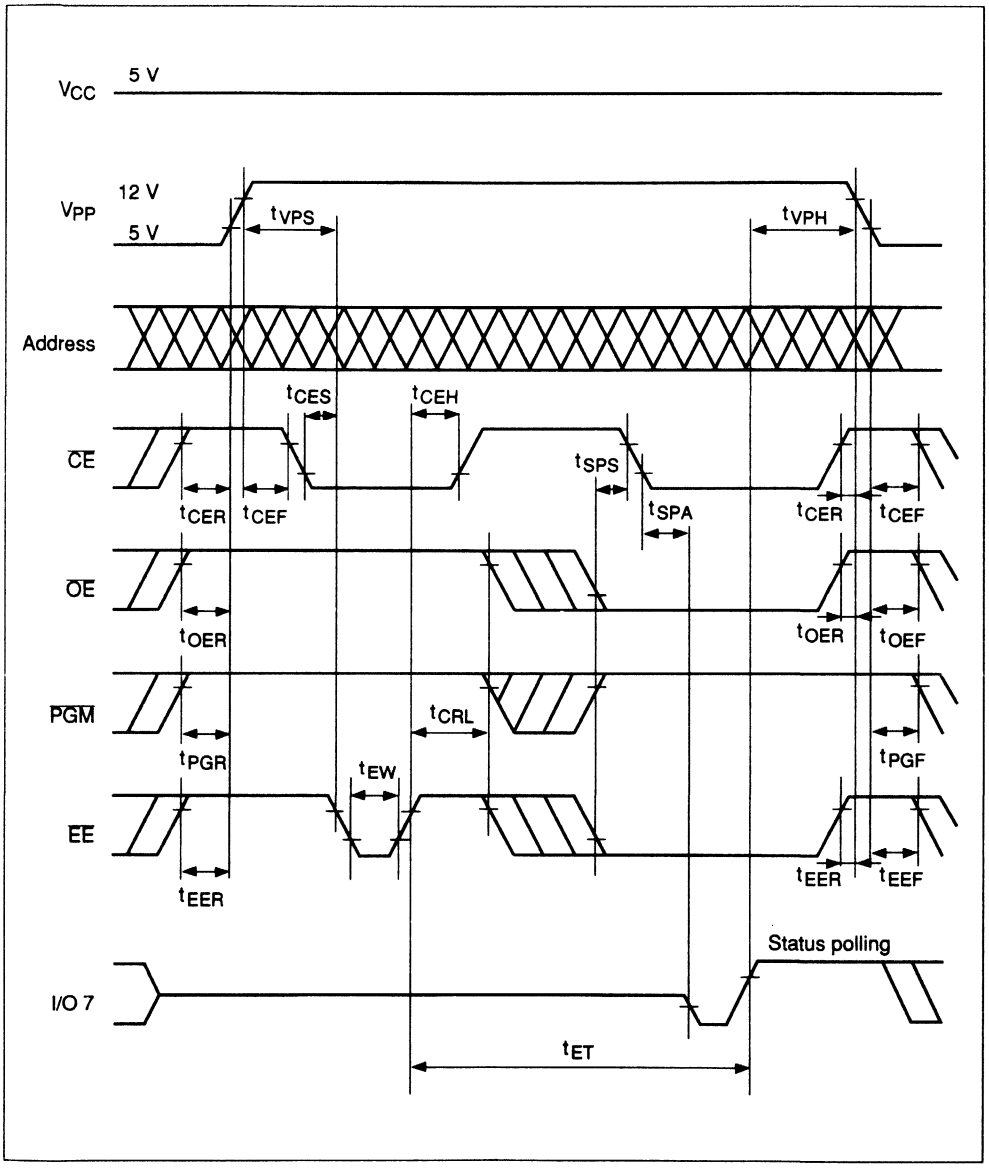
AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = 12.0 V ± 0.4 V, Ta = 0 to +70°C)

Test Condition
- Input pulse levels: 0.45 V/2.4 V
- Input rise and fall times: 10 ns
- Reference level for measuring timing: 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Chip enable setup time	t_{CES}	50	—	—	ns	
Chip enable hold time	t_{CEH}	50	—	—	ns	
Erase pulse width	t_{EW}	100	—	—	ns	
Control latch time	t_{CRL}	50	—	—	ns	
Status polling setup time	t_{SPS}	50	—	—	ns	
Status polling access time	t_{SPA}	—	60	200	ns	
V_{PP} setup time	t_{VPS}	100	—	—	ns	
V_{PP} hold time	t_{VPH}	100	—	—	ns	
Total erase time	t_{ET}	0.5	2	12	s	
$\overline{CE}$ setup time	t_{CER}*1	50	—	—	ns	
$\overline{OE}$ setup time	t_{OER}	50	—	—	ns	
$\overline{PGM}$ setup time	t_{PGR}*1	50	—	—	ns	
$\overline{EE}$ setup time	t_{EER}*1	50	—	—	ns	
$\overline{CE}$ hold time	t_{CEF}*1	50	—	—	ns	
$\overline{OE}$ hold time	t_{CEF}	50	—	—	ns	
$\overline{PGM}$ hold time	t_{PGF}*1	50	—	—	ns	
$\overline{EE}$ hold time	t_{EEF}*1	50	—	—	ns	

Note: 1. $\overline{CE}$, $\overline{EE}$ and $\overline{WE}$ must be fixed high during V_{PP} transition from 5 V to 12 V or from 12 V to 5 V.

Erase Timing Waveform



HN27C256AG Series

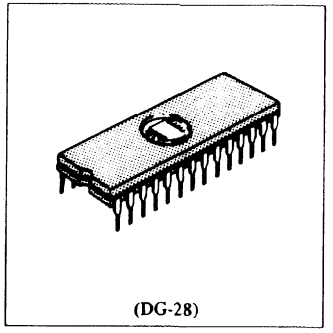
32768-Word x 8-Bit UV Erasable and Programmable ROM

This Hitachi HN27C256AG is a 256-kbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation.

Fabricated on advanced fine process and high speed circuitry technique, the HN27C256AG makes high speed access time possible for 16 bit microprocessors such as the 8086 and 68000. And low power dissipation in active and standby modes matches our CMOS 256-kbit EPROM.

In programming operation, the HN27C256AG realizes faster programming time than our conventional 256-kbit EPROM by Hitachi's Fast High-Reliability Programming Algorithm.

Pin arrangement, pin configuration and programming voltage are compatible with our 256-kbit EPROM series, therefore existing programmers can be used with the HN27C256AG.



(DG-28)

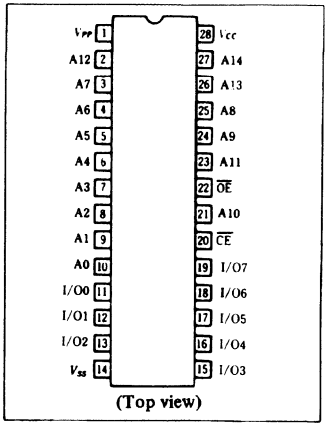
Features

- High speed
  - Access time . . . . . 100/120/150ns (max.)
- Low power dissipation
  - Active mode . . . . . 25 mW (typ.) (f = 1 MHz)
  - Standby mode . . . . . 5 μW (typ.)
- High reliability and fast programming
  - Programming voltage: +12.5V DC
  - Fast High-Reliability Programming Algorithm available
- Device identifier mode
  - Manufacturer code and device code

Ordering Information

Type No.	Access Time	Package
HN27C256AG-10	100 ns	600-mil 28-pin cerdip
HN27C256AG-12	120 ns	
HN27C256AG-15	150 ns	

Pin Arrangement

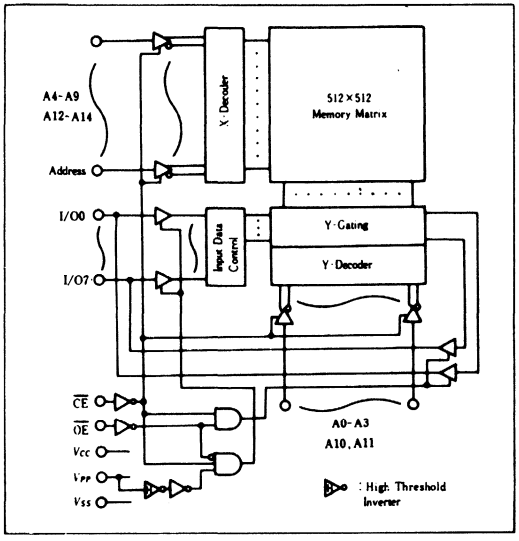


(Top view)

Pin Description

Pin Name	Function
A0 – A14	Address
I/O0–IO7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	x	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	x	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	x	V_{PP}	V_{CC}	Din
Program verify	V_{IH}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Optional verify	V_{IL}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Program inhibit	V_{IH}	V_{IH}	x	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes: 1. x = Don't care.
2. V_H = 12.0V ± 0.5V.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output Voltages*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –1.0V for pulse width ≦ 50ns.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	4	8	pF	Vin = 0V
Output capacitance	$Cout$	–	8	12	pF	Vout = 0V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ±10%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
Output leakage current	I_{LO}	–	–	2	μA	$Vout$ = 0V to V_{CC}
V_{PP} current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
Standby V_{CC} current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = VIH
	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ± 0.3V
Operating V_{CC} current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, $Iout$ = 0 mA
	I_{CC2}	–	–	30	mA	f = 10 MHz, $Iout$ = 0 mA
	I_{CC3}	–	5	15	mA	f = 1 MHz, $Iout$ = 0 mA
Input low voltage*3	V_{IL}	−0.3*1	–	0.8	V	
Input high voltage*3	V_{IH}	2.2	–	V_{CC}+1.0*2	V	
Output low voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH1}	2.4	–	–	V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC}−0.7	–	–	V	I_{OH} = −100 μA

Notes: *1. V_{IL} min = −1.0V for pulse width ≦ 50ns.
*2. V_{IH} max = V_{CC} + 1.5V for pulse width ≦ 20ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
*3. Only defined for DC function test. V_{IL} max = 0.45V, V_{IH} min = 2.4V for AC function test.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5V ±10%, V_{PP} = V_{CC})

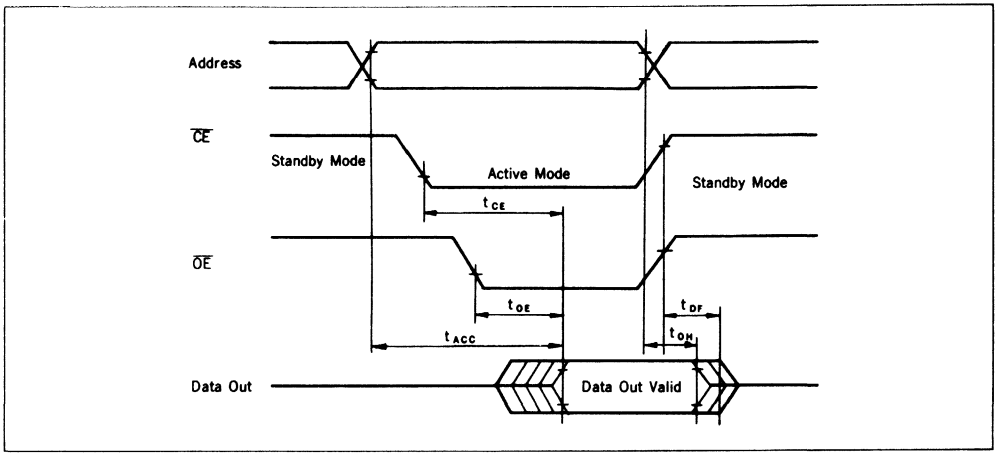
Test condition

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 10ns
- Output load: 1 TTL Gate + 100pF
- Reference lvels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	HN27C256AG-10		HN27C256AG-12		HN27C256AG-15		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	100	–	120	–	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	100	–	120	–	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	–	60	–	60	–	70	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	–	5	–	5	–	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

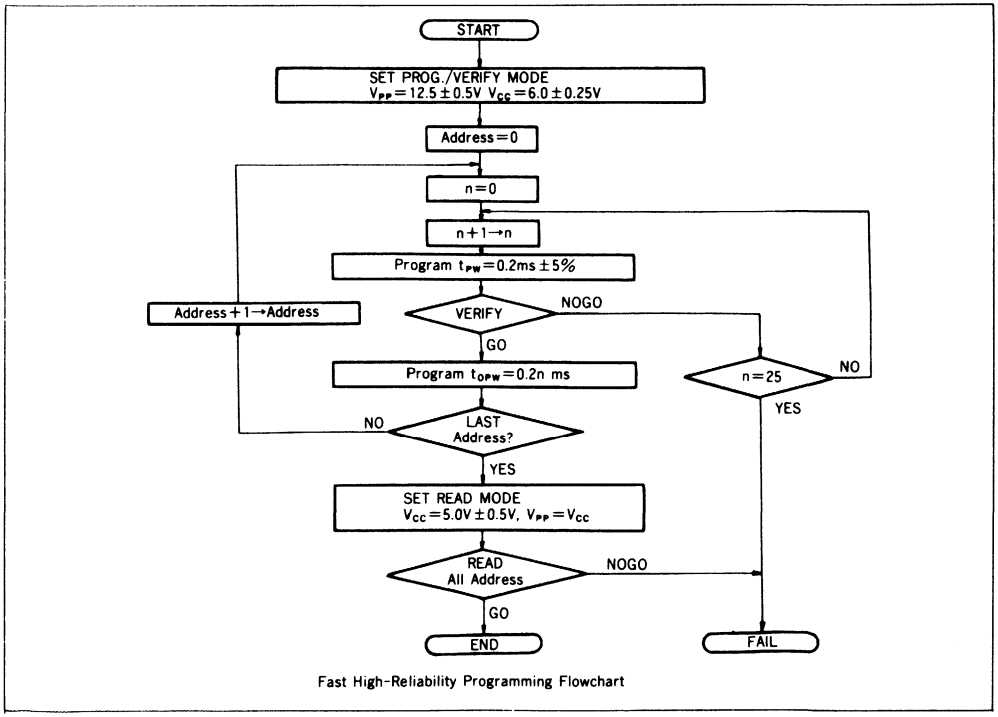
Read Timing Waveform



Programming Operation

Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data retension. A theoretical programming time (except brank checking and verifying time) is one-tenth of conventional high performance programming algorithm's. Regarding the model and software version of the programmers available this algorithm, please contact programmer maker.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	-0.1*5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
Output low voltage during verity	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = -400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V or 12.5V to V_{IL} when CE = Low.
5. V_{IL} min = -0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

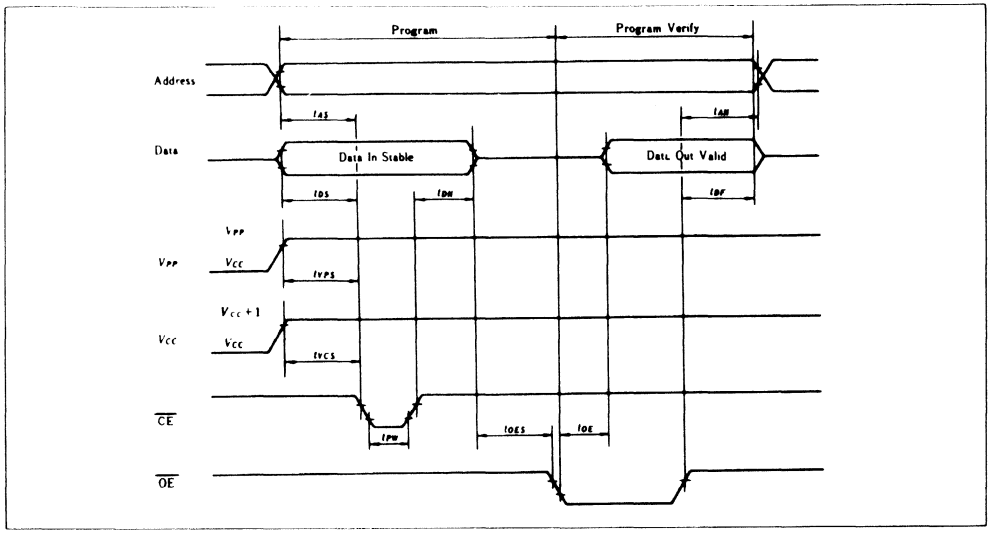
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	μs
$\overline{OE}$ setup time	t_{OES}	2	–	–	μs
Data setup time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
V_{PP} setup time	t_{VPS}	2	–	–	μs
V_{CC} setup time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.19	0.20	0.21	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	0.19	–	5.25	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

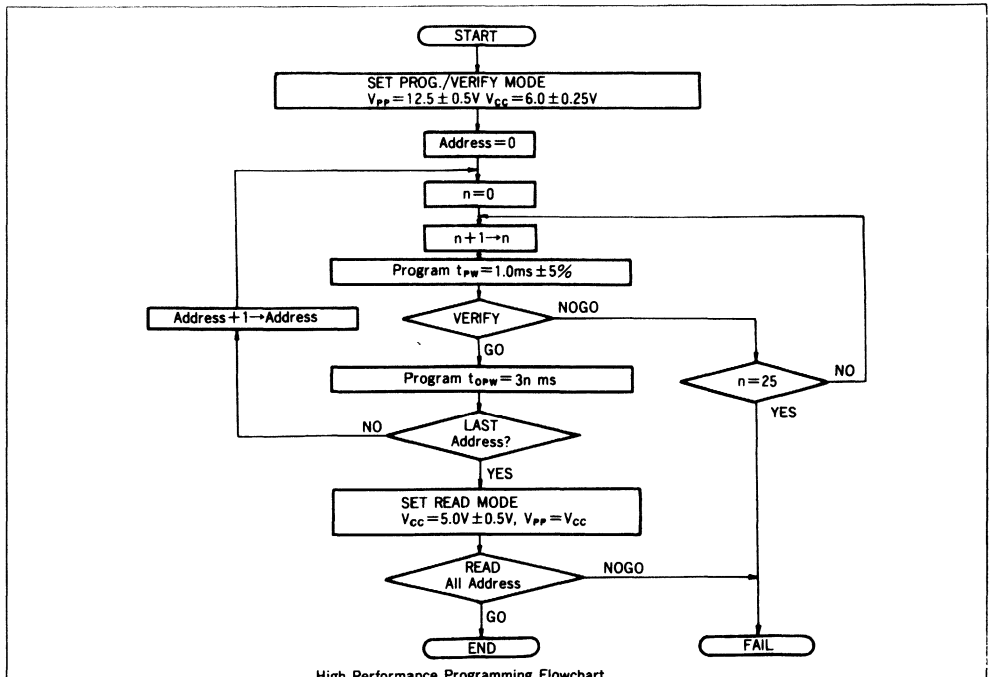
Notes: 1. Refer to the Fast High-Reliability Programming Fowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform



High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-kbit EPROM series so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	−0.1*5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = −400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = −0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation. cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

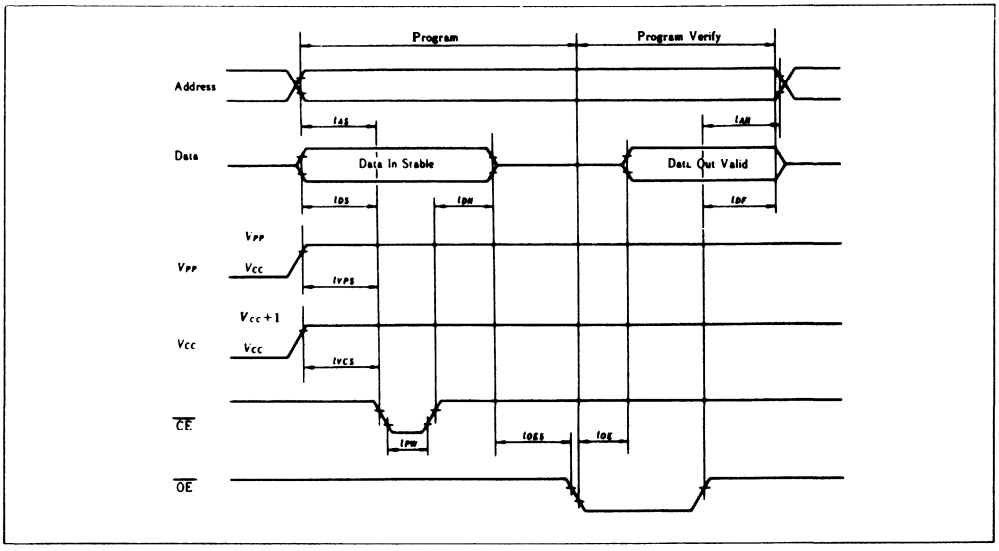
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	μs
$\overline{OE}$ setup time	t_{OES}	2	–	–	μs
Data setup time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
V_{PP} setup time	t_{VPS}	2	–	–	μs
V_{CC} setup time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.95	1.0	1.05	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	2.85	–	78.75	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

Notes: 1. Refer to the high performance programming flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform



Erase

Erasure of HN27C256AG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 $W \cdot sec/cm^2$.

Mode Description

Device Identifier Mode

Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

HN27C256AG Series Identifier Code

Identifier	A0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. A9 = 12.0V ± 0.5V.
2. A1 – A8, A10 – A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

HN27C256HG Series

32768-Word x 8-Bit CMOS UV Erasable and Programmable ROM

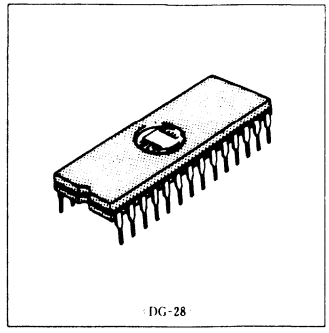
The Hitachi HN27C256HG is a 256-kbit ultraviolet erasable and electrically programmable ROM, featuring sub-100-ns access times.

The HN27C256HG realizes access time of 70ns and 85ns, employing the advanced fine process and high speed circuitry technique.

The timing conditions such as access time or output hold time are designed as same as our byte-wide SRAMs', allowing to use with SRAMs on the same memory board by the same read timings. So its board design in 16-bit microprocessor systems is easy.

Also, the HN27C256HG realizes faster programming time than our conventional 256-kbit EPROM by Hitachi's Fast High-Reliability Programming Algorithm.

Pin arrangement, pin configuration and programming voltage are compatible with our 256-kbit EPROM series, therefore existing programmers can be used with the HN27C256HG.



DG-28

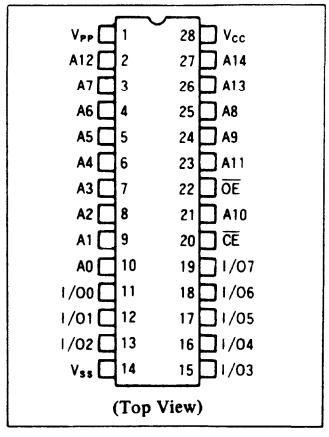
Features

- High speed . . . . . Access time 70/85ns (max.)
- Low power dissipation
  - Active mode . . . . . 30 mW (typ.) (f = 1 MHz)
- High reliability and fast programming
  - Programming voltage: +12.5V DC
  - Fast High-Reliability Programming Algorithm available
- Device identifier mode
  - Manufacturer code and device code

Ordering Information

Type No.	Access Time	Package
HN27C256HG-70	70 ns	600-mil 28-pin cerdip
HN27C256HG-85	85 ns	

Pin Arrangement

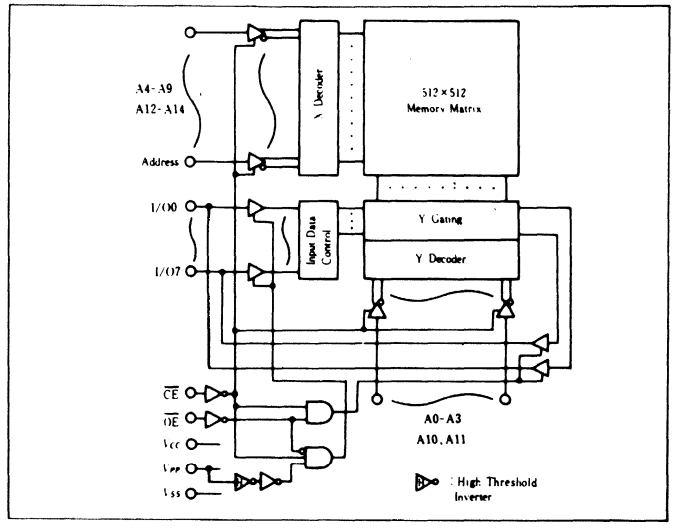


(Top View)

Pin Description

Pin Name	Function
A0 – A14	Address
I/O0–IO7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	x	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	x	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	x	V_{PP}	V_{CC}	Din
Program verify	V_{IH}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Optional verify	V_{IL}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Program inhibit	V_{IH}	V_{IH}	x	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes: 1. x = Don't care
2. V_H = 12.0V ± 0.5V.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –1.0V for pulse width ≦ 50ns.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	4	8	pF	Vin = 0V
Output capacitance	Cout	–	8	12	pF	Vout = 0V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, $V_{PP} = V_{CC}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
Output leakage current	I_{LO}	–	–	2	μA	$Vout$ = 0V to V_{CC}
V_{PP} current	I_{PP1}	–	1	100	μA	V_{PP} = 5.5V
Standby V_{CC} current	I_{SB}	–	–	15	mA	$\overline{CE} = V_{IH}$
Operating V_{CC} current	I_{CC1}	–	–	30	mA	$\overline{CE} = V_{IL}$, $Iout$ = 0 mA
	I_{CC2}	–	–	50	mA	f = 15 MHz, $Iout$ = 0mA
	I_{CC3}	–	5	15	mA	f = 1 MHz, $Iout$ = 0 mA
Input low voltage*3	V_{IL}	−0.3*1	–	0.8	V	
Input high voltage*3	V_{IH}	2.2	–	V_{CC}+1.0*2	V	
Output low voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH1}	2.4	–	–	V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC}−0.7	–	–	V	I_{OH} = −100 μA

Notes: 1. V_{IL} min = −1.0V for pulse width ≦ 50ns.
2. V_{IH} max = V_{CC} + 1.5V for pulse width ≦ 20ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
3. Only defined for DC function test. V_{IL} max = 0.45V, V_{IH} min = 2.4V for AC function test.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, $V_{PP} = V_{CC}$)

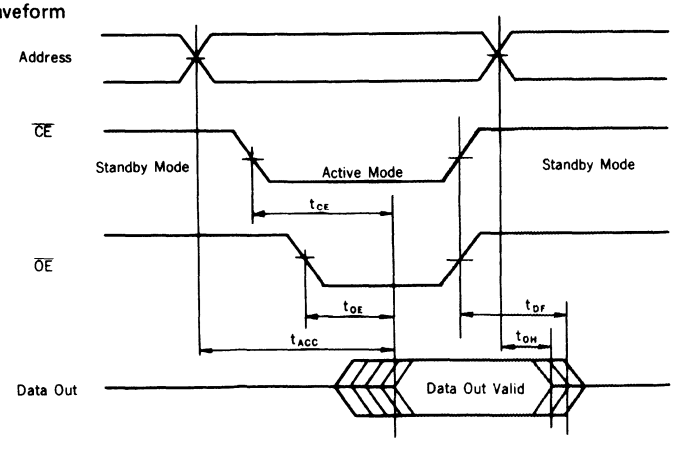
Test conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 10ns
- Output load: 1 TTL Gate + 100 pF
- Reference levels for measuring timing: Input; 1.5V
  Outputs; 1.5V

Parameter	Symbol	HN27C256 HG-70		HN27C256 HG-85		Unit	Test Conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	70	–	85	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to output delay	t_{CE}	–	70	–	85	ns	$\overline{OE} = V_{IL}$
$\overline{OE}$ to output delay	t_{OE}	–	40	–	45	ns	$\overline{CE} = V_{IL}$
$\overline{OE}$ high to output float	t_{DF}	0	30	0	30	ns	$\overline{CE} = V_{IL}$
Address to output hold	t_{OH}	5	–	5	–	ns	$\overline{CE} = \overline{OE} = V_{IL}$

Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

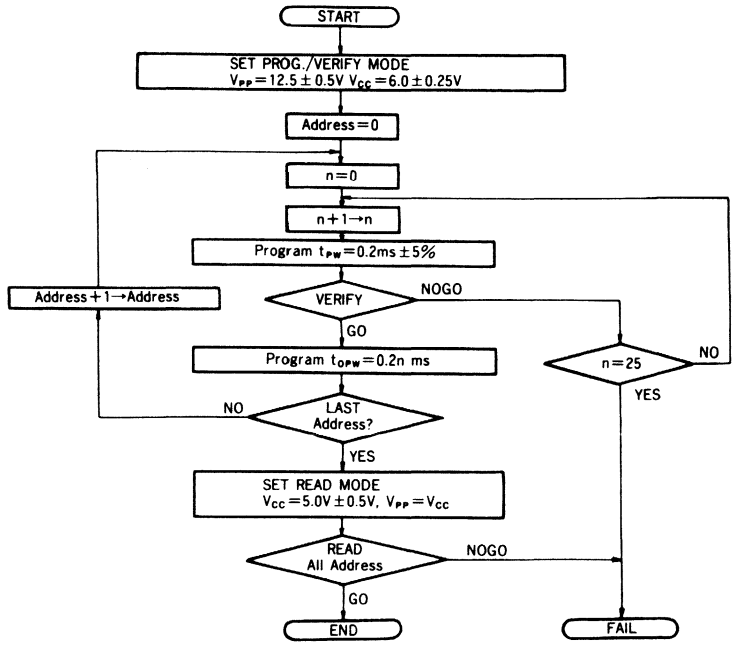
Read Timing Waveform



Programming Operation

Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data retension. A theoretical programming time (except brank checking and verifying time) is one-tenth of conventional high performance programming algorithm's. Regarding the model and software version of the programmers available this algorithm, please contact programmer maker.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	−0.1 *5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5 *6	V	
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = −400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = −0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Test Conditions

Input pulse levels: 0.45V to 2.4V

Input rise and fall times: ≦ 20ns

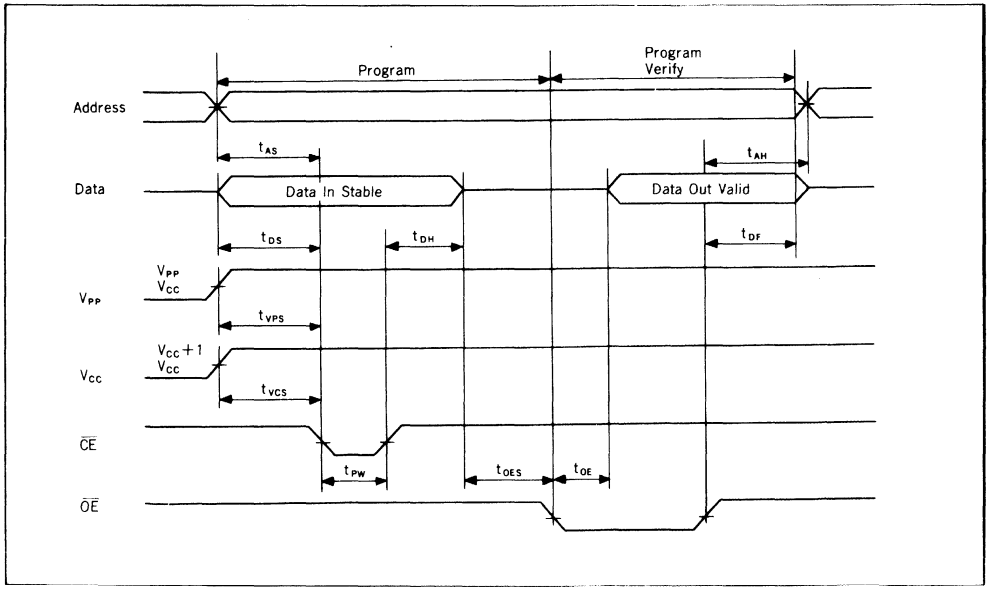
Reference levels for measuring timing: Inputs; 0.8V and 2.0V

Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	µs
$\overline{OE}$ setup time	t_{OES}	2	–	–	µs
Data setup time	t_{DS}	2	–	–	µs
Address hold time	t_{AH}	0	–	–	µs
Data hold time	t_{DH}	2	–	–	µs
V_{PP} setup time	t_{VPS}	2	–	–	µs
V_{CC} setup time	t_{VCS}	2	–	–	µs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.19	0.20	0.21	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	0.19	–	5.25	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

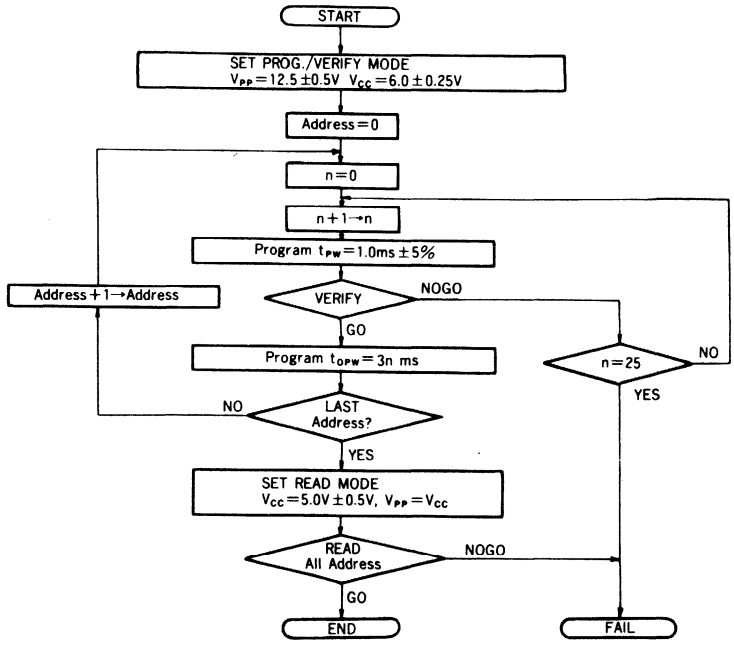
Notes: 1. Refer to the Fast High-Reliability Programming Flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform



High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-kbit EPROM series, so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	µA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	–0.1*5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = –400 µA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

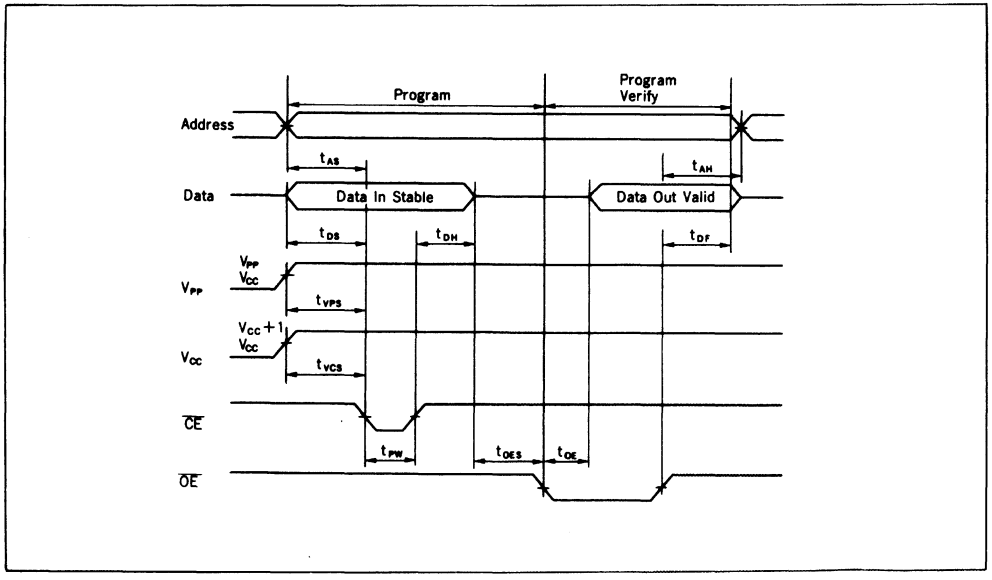
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 1.5V
  Outputs; 1.5V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	µs
$\overline{OE}$ setup time	t_{OES}	2	–	–	µs
Data setup time	t_{DS}	2	–	–	µs
Address hold time	t_{AH}	0	–	–	µs
Data hold time	t_{DH}	2	–	–	µs
V_{PP} setup time	t_{VPS}	2	–	–	µs
V_{CC} setup time	t_{VCS}	2	–	–	µs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.95	1.0	1.05	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW}*1	2.85	–	78.75	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF}*2	–	–	130	ns

Notes: 1. Refer to the high performance programming flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform



Erase

Erasure of HN27C256HG is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 $W \cdot sec/cm^2$.

Mode Description

Device Identifier Mode

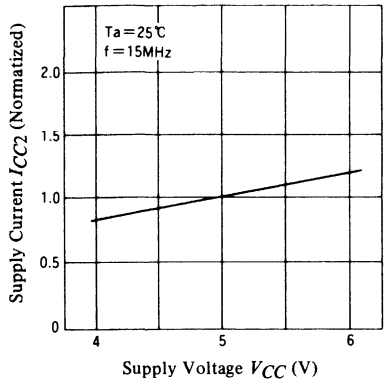
Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. The countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

HN27C256HG Series Identifier Code

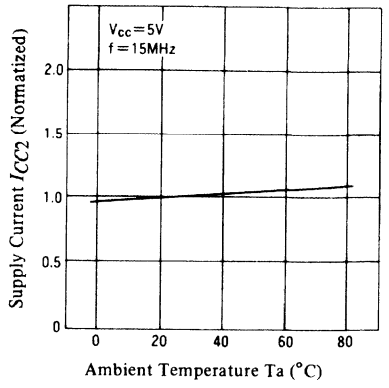
Identifier	A0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. A9 = 12.0V ± 0.5V.
2. A1 – A8, A10 – A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

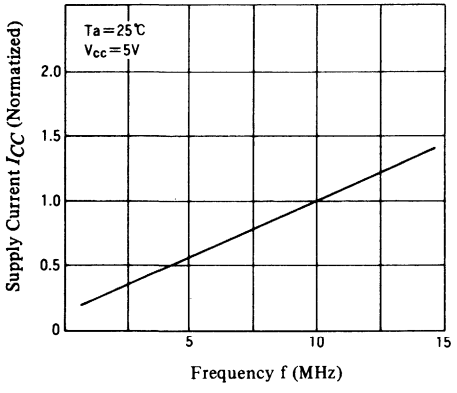
SUPPLY CURRENT vs. SUPPLY VOLTAGE



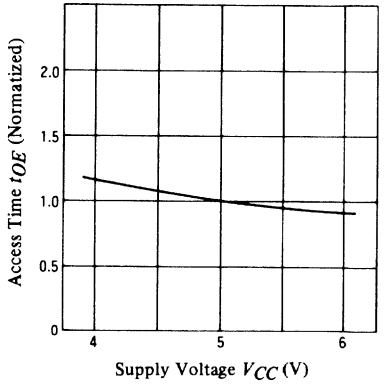
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



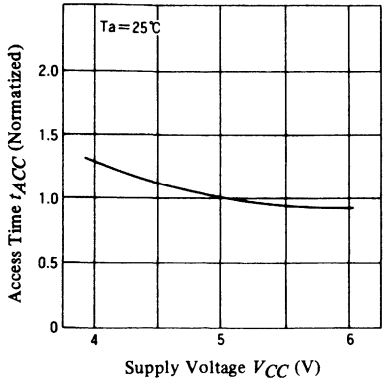
SUPPLY CURRENT-FREQUENCY



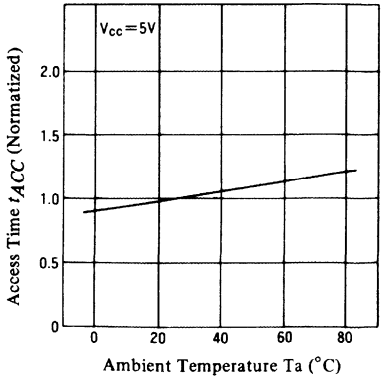
ACCESS TIME – SUPPLY VOLTAGE



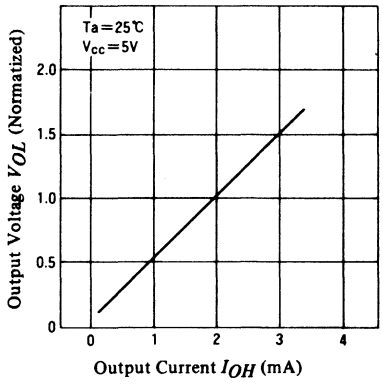
ACCESS TIME – SUPPLY VOLTAGE



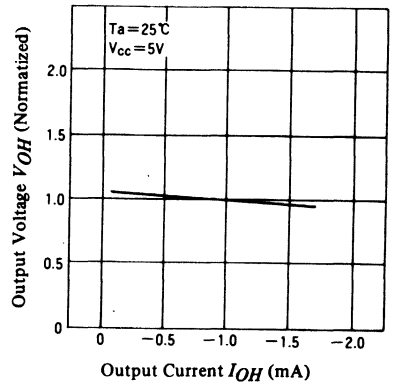
ACCESS TIME – AMBIENT TEMPERATURE



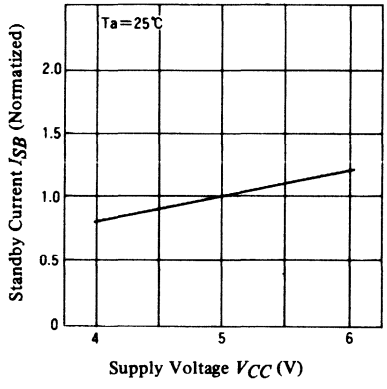
OUTPUT VOLTAGE vs. OUTPUT CURRENT



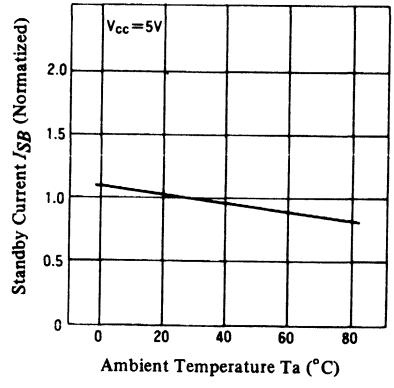
OUTPUT VOLTAGE vs. OUTPUT CURRENT



STANDBY CURRENT vs. SUPPLY VOLTAGE



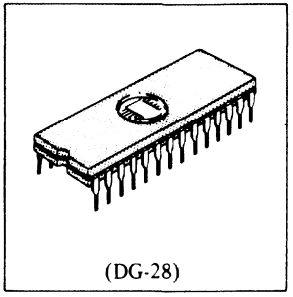
STANDBY CURRENT vs. AMBIENT TEMPERATURE



HN27512G Series

65536-word x 8-bit UV Erasable and Programmable ROM

The HN27512G is a 65536-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin dual in-line package with transparent window. The transparent window allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.


(DG-28)

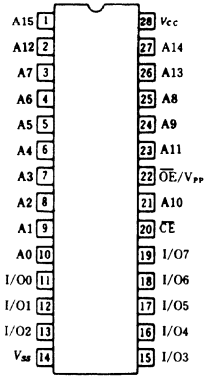
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 250/300ns (max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V (max.)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code

■ ORDERING INFORMATION

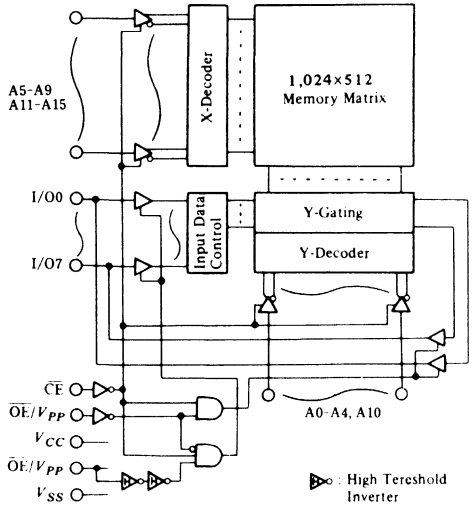
Type No.	Access Time	Package
HN27512G-25	250ns	600 mil 28 pin Cerdip
HN27512G-30	300ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	V_{CC} (28)	I/O (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	Code

Notes) *1. X . . . Don't care
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. with respect to V_{SS}.

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25V/0.45V	−	−	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	−	−	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	−	45	100	mA
Input Low voltage	V_{IL}		−0.1*1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	−	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	−	−	V

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

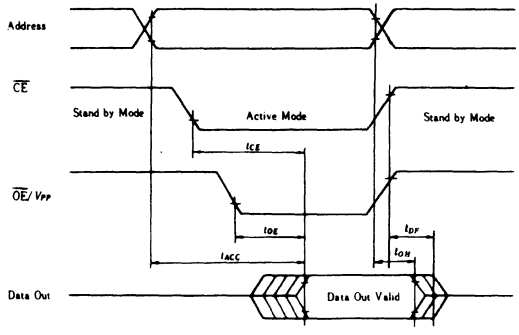
Parameter	Symbol	Test Condition	HN27512G-25		HN27512G-30		Unit
			min.	max.	min.	max.	
Addres to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1 TTL Gate +100pF
Reference Level for Measuring Timing:	0.8V and 2.0V

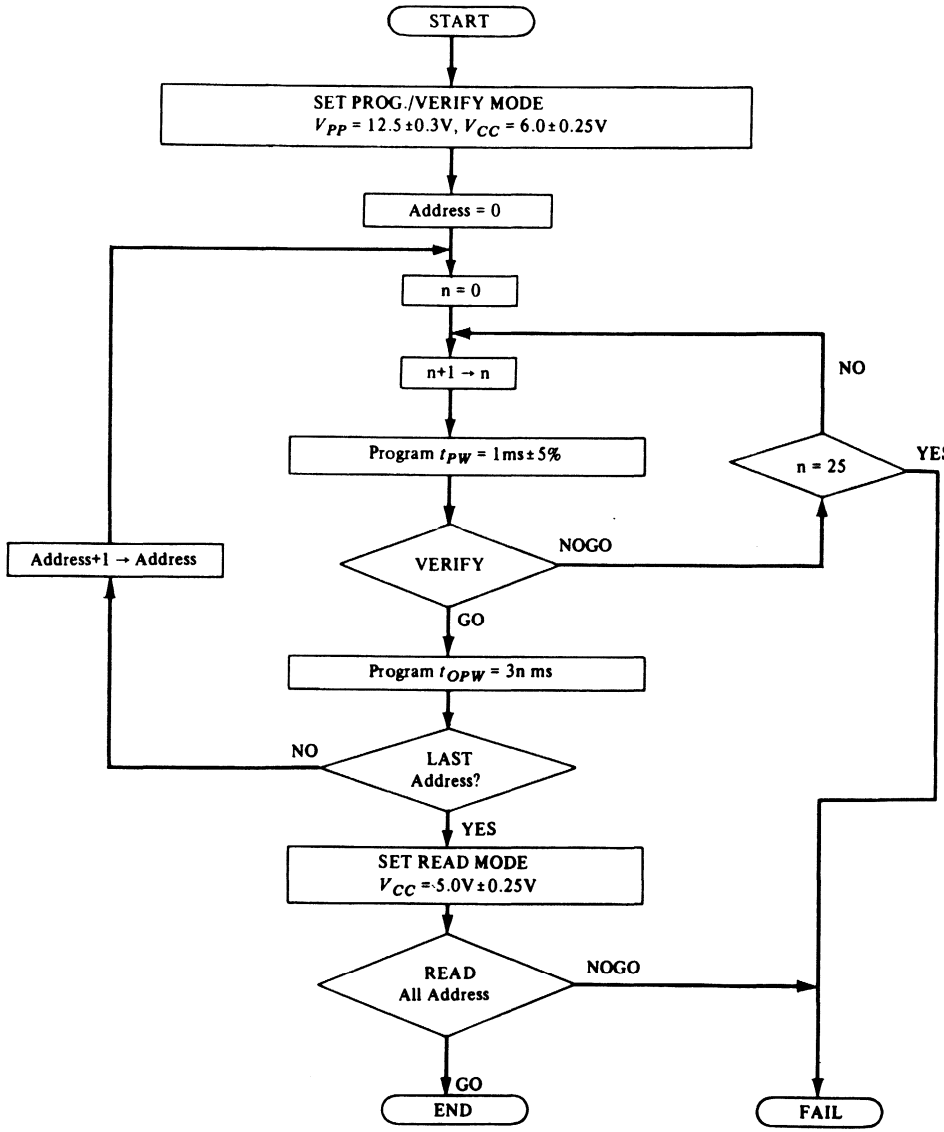


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter		Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	except $\overline{OE}/V_{PP}$	C_{in1}	V_{in} = 0V	–	4	6	pF
	$\overline{OE}/V_{PP}$ Pin	C_{in2}	V_{in} = 0V	–	12	20	pF
Output Capacitance		C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		−0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. −0.6V for pulse width ≦ 20ns.
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

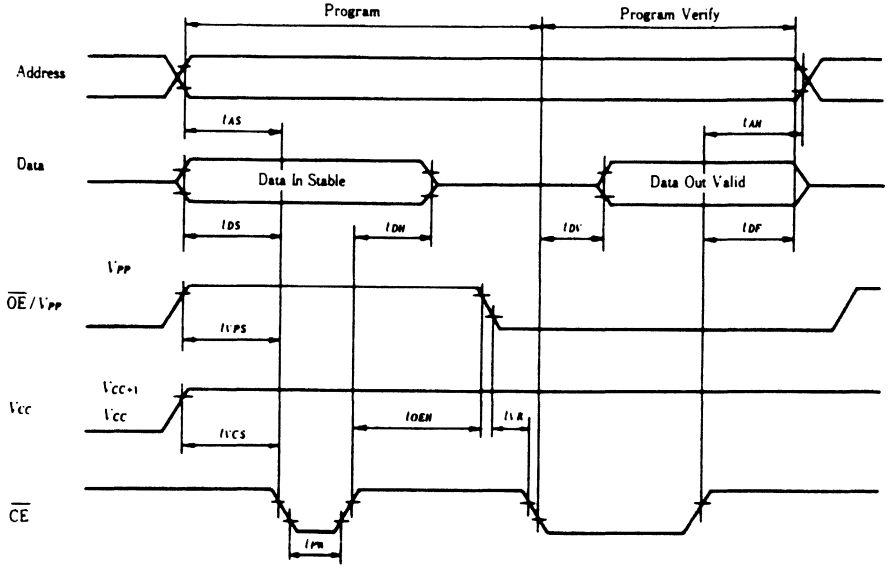
• AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs
$\overline{CE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
V_{PP} Recovery Time	t_{VR}		2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}		–	–	1	μs

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

- **SWITCHING CHARACTERISTICS**

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ ERASE

Erasure of HN27512G is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W · sec/cm^2.

■ DEVICE IDENTIFIER MODE

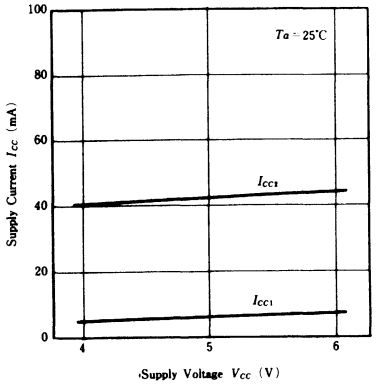
The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

- **HN27512G SERIES IDENTIFIER CODE**

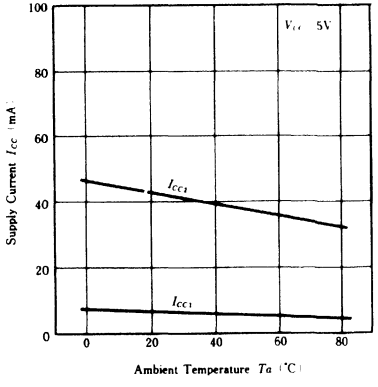
Identifier \ Pins	A_0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	0	1	0	1	0	0	94

Notes: 1. A_0 = 12.0 ± 0.5V.
2. $A_1 - A_8$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$.

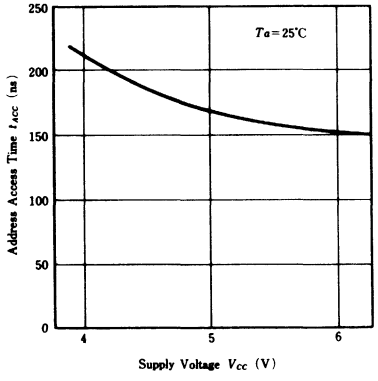
SUPPLY CURRENT vs. SUPPLY VOLTAGE



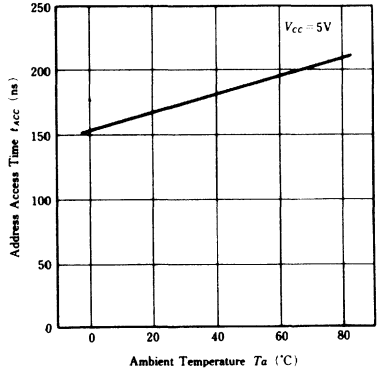
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



HN27C512G Series

65536-Word × 8-Bit CMOS UV Erasable and Programmable ROM

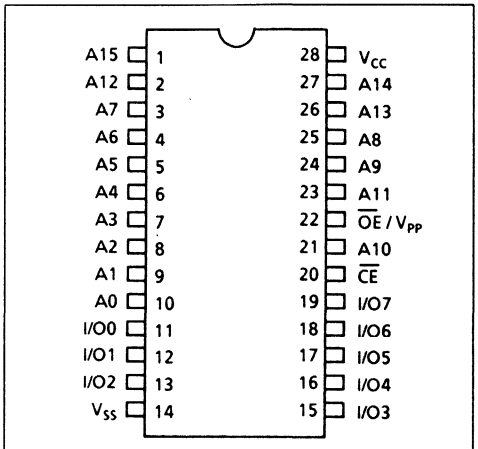
Features

- Single power supply: 5 V ± 5%
- High performance programming
  Programming voltage: +12.5 V DC
  high performance programming operations
- Static: No clocks required
- Inputs and outputs TTL compatible during both read and program modes
- Access time: 170/200 ns (max)
- Absolute maximum rating of V_{PP} pin:
  14.0 V (max)
- Low standby current: 250 µA (max)
- Device identifier mode: Manufacturer code and device code

Ordering Information

Type No.	Access time	Package
HN27C512G-17	170 ns	600-mil 28-pin cerdip
HN27C512G-20	200 ns	

Pin Arrangement

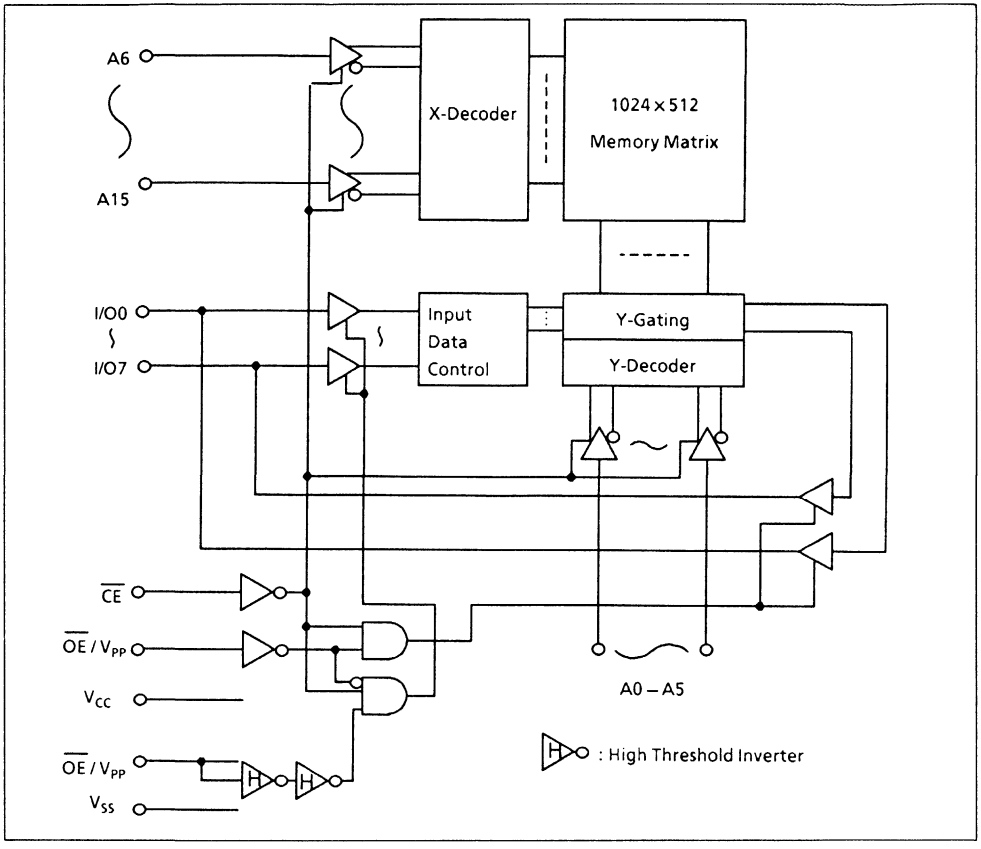


(Top View)

Pin Description

Pin name	Function
A0 – A15	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	V_{CC} (28)	I/O (11–13, 15 – 19)
Read	V_{IL}	V_{IL}	×	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	×	V_{CC}	High-Z
Standby	V_{IH}	×	×	V_{CC}	High-Z
Program	V_{IL}	V_{PP}	×	V_{CC}	Din
Program verify	V_{IL}	V_{IL}	×	V_{CC}	Dout
Program inhibit	V_{IH}	V_{PP}	×	V_{CC}	High-Z
Identifier	V_{IL}	V_{IL}	V_H *2	V_{CC}	Code

Notes: 1. × = Don't care.
2. V_H = 12.0 V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	Vin,Vout	–0.6 to +6.5	V
V_{PP} voltage *1	V_{PP}	–0.6 to +14.0	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6 to +13.5	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Note: 1. Relative to V_{SS}.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	except $\overline{OE}$ / V_{PP}	Cin	—	6	10	pF	Vin = 0 V
	$\overline{OE}$ / V_{PP}		—	20	25		
Output capacitance		Cout	—	8	14	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 5 V ± 5%, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	10	µA	Vin = 0 V to V_{CC}
Output leakage current	I_{LO}	—	—	10	µA	Vout = 0 V to V_{CC}
Standby V_{CC} current	I_{SB1}	—	—	500	µA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	—	250	µA	$\overline{CE}$ = V_{CC}
Operating V_{CC} current	I_{CC}	—	35	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 6 MHz
Input low voltage	V_{IL}	–0.1*1	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	V_{CC}+1.0*2	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (V_{CC} = 5 V ± 5%, Ta = 0 to +70°C)

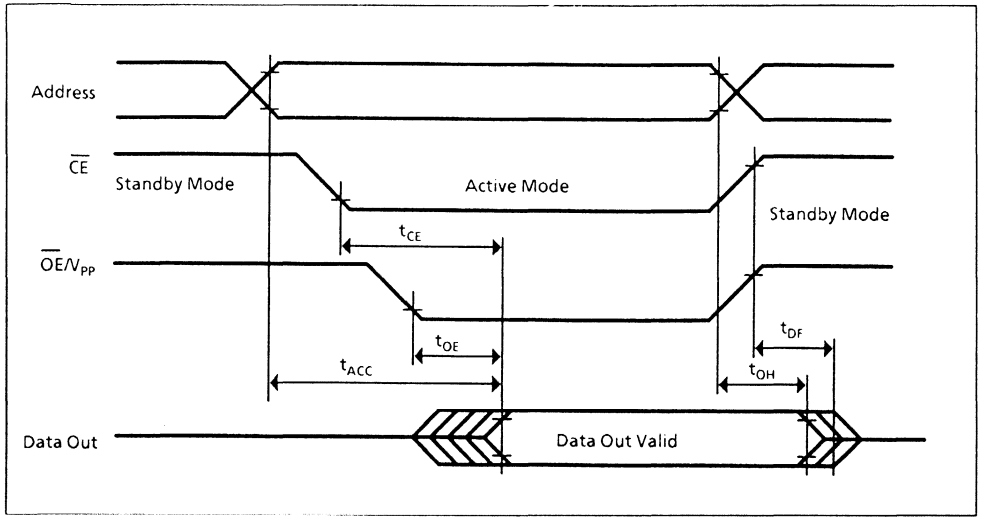
Test condition

- Input pulse levels : 0.4 V to 2.4 V
- Input rise and fall times : ≤ 20 ns
- Output load : 1 TTL gate +100 pF
- Reference levels for measuring timing:
  Inputs ; 0.8 V, 2.0 V
  Outputs ; 0.8V, 2.0 V

		HN27C512G-17		HN27C512G-20			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	170	—	200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	170	—	200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	75	—	75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float*1	t_{DF}	0	60	0	60	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

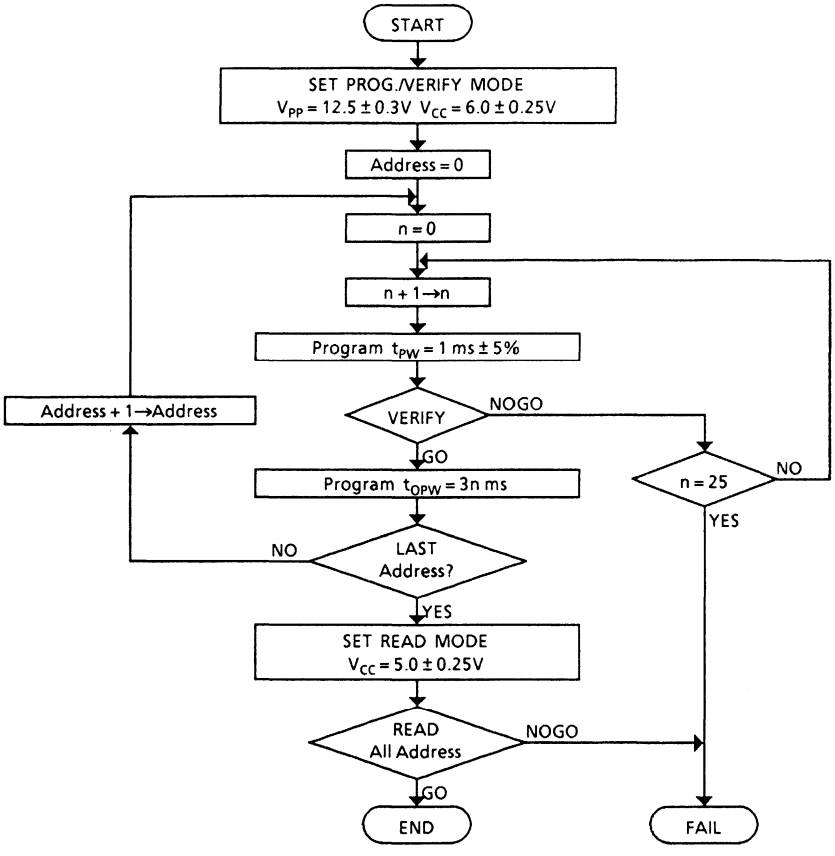
Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



High Performance Programming

This device can be applied the programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High—Peformance Programming Flowchart

DC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	10	µA	Vin = 0 V to V_{CC}
Output low voltage during verify	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = -400 µA

DC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C) (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input low level	V_{IL}	–0.1*1	—	0.8	V	
Input high level	V_{IH}	2.0	—	V_{CC}+0.5*2	V	
V_{PP} supply current	I_{PP}	—	35	50	mA	$\overline{CE}$ = V_{IL}

Notes: 1. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

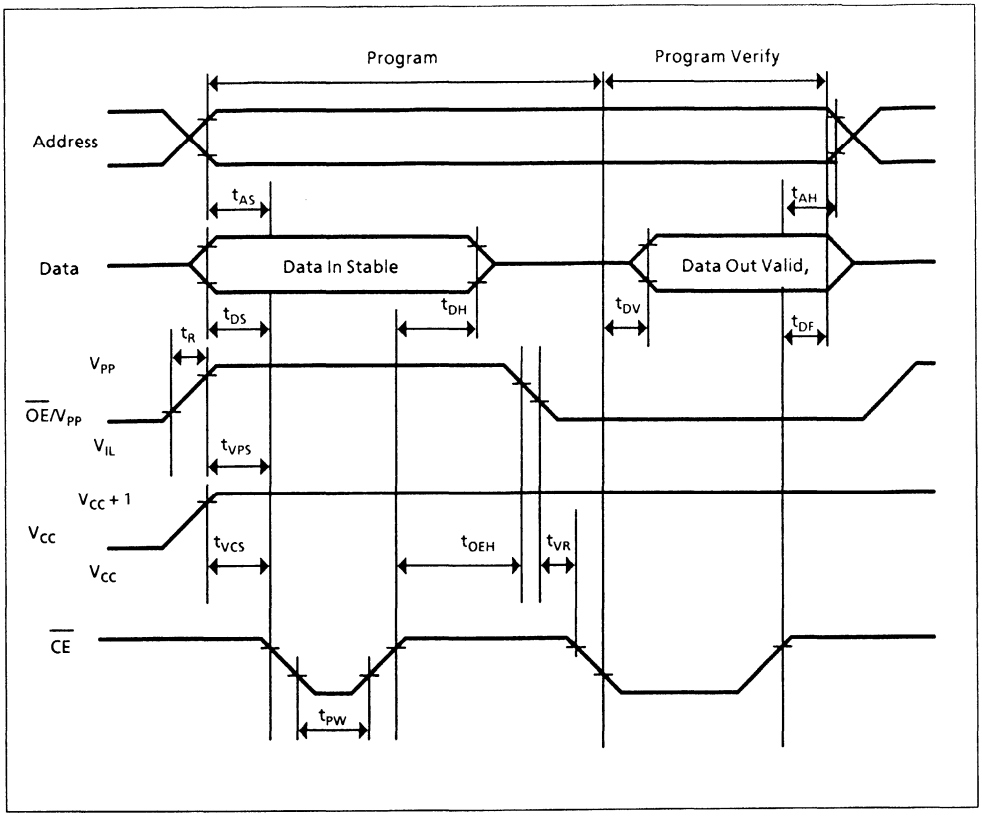
Test condition

- Input pulse levels : 0.4 V to 2.4 V
- Input rise and fall times : ≤ 20 ns
- Reference levels for measuring timing : 0.8 V, 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs	
$\overline{OE}$ to output float delay	t_{DF} *1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{CE}$ initial programming pulth width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ overprogramming pulse width	t_{OPW}*2	2.85	—	78.75	ms	
V_{PP} rising time	t_R	50	—	—	ns	
V_{PP} recovery time	t_{VR}	2	—	—	µs	
Data valid from $\overline{CE}$	t_{DV}	—	—	1	µs	

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

High Performance Programming Timing Waveform



Erase

Erasure of HN27C512G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W. sec/cm^2.

Mode Description

Device Identifier Mode

The identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

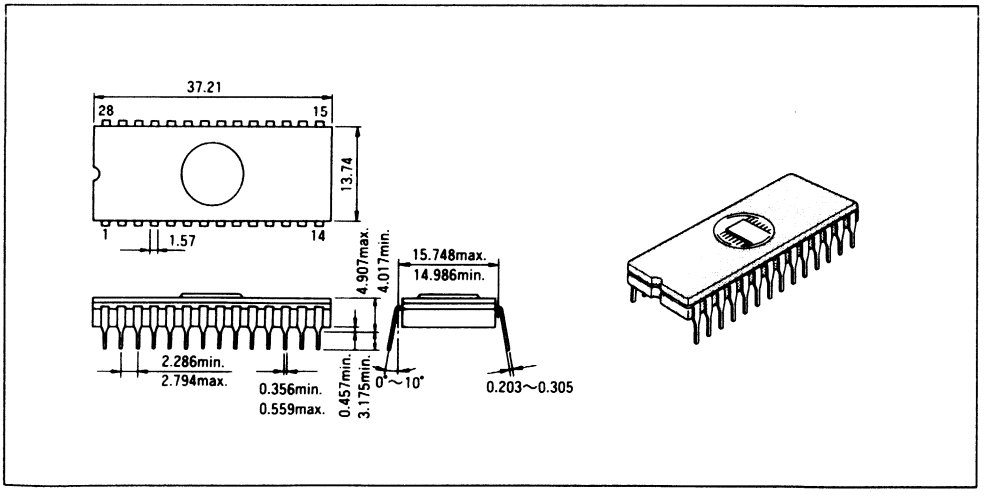
HN27C512G Series Identifier Code

Identifier	A0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex data
Manufacturer code	V_{IL}	1	0	0	1	0	1	1	1	97
Device code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: 1. A9 = 12.0 V ± 0.5 V
2. A1 to A8, A10 to A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

Package Outline

Unit: mm (inch)



HN27C1024H Series

65536-Word × 16-Bit CMOS UV Erasable and Programmable ROM

The Hitachi HN27C1024H series is a 1-Mbit (64-kword × 16-bit) ultraviolet erasable and electrically programmable ROM. Fabricated on new advanced fine process technique, the HN27C1024H makes high speed access time 85/100 ns (max) possible. (HN27C1024H is a fastest 1-Mbit EPROM.) Therefore, it is suitable for 16-bit microcomputer systems using high speed microcomputer such as the 8086 and 68000. The HN27C1024H offers high speed programming using page programming mode. It has the package variation of cerdip-40 pin and JLCC-44 pin.

Features

- Fast high-reliability programming mode and fast high-reliability page programming mode
  Programming voltage: 12.5 V DC
  Fast High-reliability page programming 14 sec (typ)
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 60 mW/MHz (typ)
- Device identifier mode: Manufacturer code and device code
- JEDEC standard

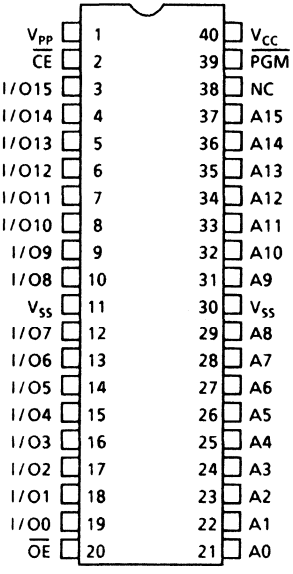
Ordering Information

Type No.	Access time	Package
HN27C1024HG-85	85 ns	600-mil 40-pin cerdip (DG-40A)
HN27C1024HG-10	100 ns	
HN27C1024HG-12	120 ns	
HN27C1024HG-15	150 ns	
HN27C1024HCC-85*1	85 ns	44-pin J-bend leaded chip carrier*1 (CC-44)
HN27C1024HCC-10*1	100 ns	
HN27C1024HCC-12	120 ns	
HN27C1024HCC-15	150 ns	

Note: 1. Preliminary

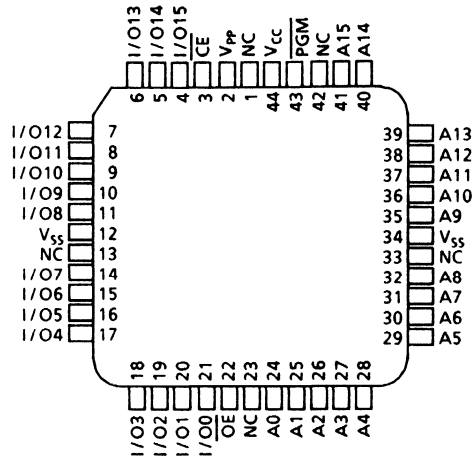
Pin Arrangement

HN27C1024HG series



(Top View)

HN27C1024HCC series

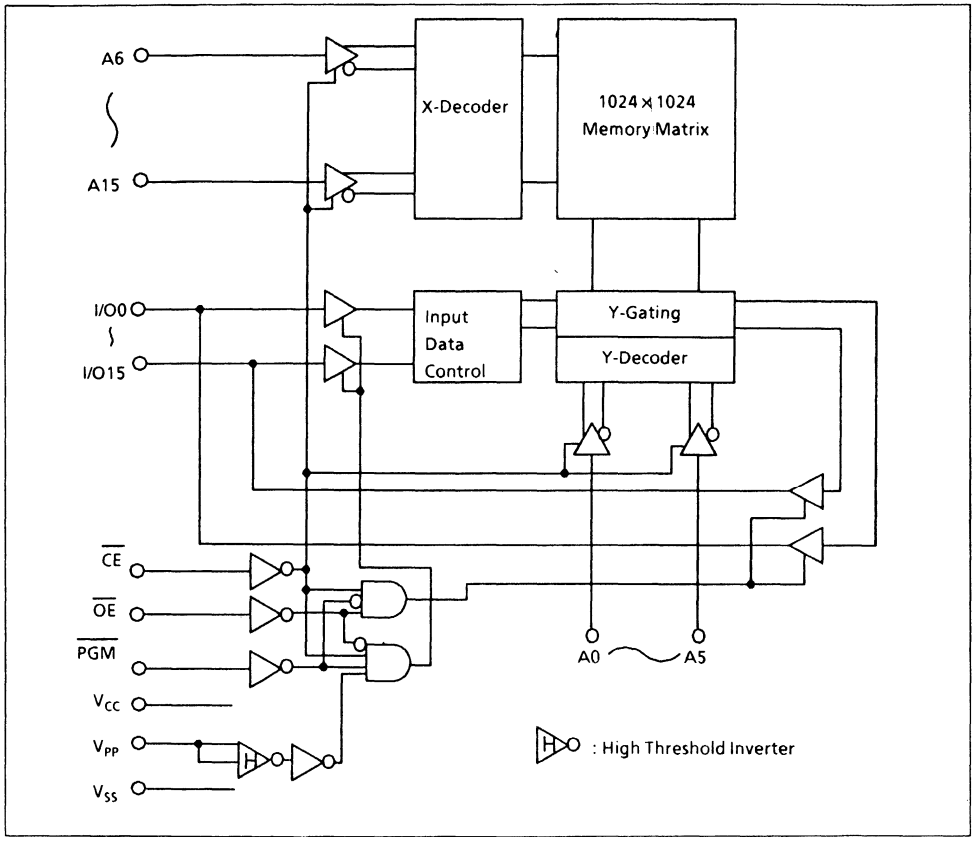


(Top View)

Pin Description

Pin name	Function
A0 – A15	Address
I/O0 – I/O15	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

	Pin	CE	OE	PGM	V_{PP}	V_{CC}	A9	I/O
	DG – 40A	(2)	(20)	(39)	(1)	(40)	(31)	(3 – 10, 12 – 19)
Mode	CC – 44	(3)	(22)	(43)	(2)	(44)	(35)	(4 – 11, 14 – 21)
Read		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	×	Dout
Output disable		V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	×	High-Z
Standby		V_{IH}	×	×	V_{CC}	V_{CC}	×	High-Z
Program		V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	×	Din
Program verify		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	×	Dout
Page data latch		V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	×	Din

Mode Selection (cont)

	Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	A9	I/O
	DG – 40A	(2)	(20)	(39)	(1)	(40)	(31)	(3 – 10, 12 – 19)
Mode	CC – 44	(3)	(22)	(43)	(2)	(44)	(35)	(4 – 11, 14 – 21)
Page program		V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	×	High-Z
Program inhibit		V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	×	High-Z
		V_{IL}	V_{IH}	V_{IH}				
		V_{IH}	V_{IL}	V_{IL}				
		V_{IH}	V_{IH}	V_{IH}				
Identifier		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_H	Code

Note: ×; Don't care, V_H: 12.0 V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages *1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage *1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage *1	V_{PP}	–0.6 to +13.0	V
V_{CC} voltage *1	V_{CC}	–0.6 to 7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –1.0 V for pulse width ± 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	12	pF	Vin = 0 V
Output capacitance	Cout	—	—	15	pF	Vout = 0 V

Read Operation

DC Characteristics (Ta = 0 to +70°C, VCC = 5 V ± 5%, VPP = VCC)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 5.25 V
Output leakage current	I_{LO}	—	—	2	µA	Vout = 5.25 V/0.45 V
V_{PP} current	I_{PP1}	—	1	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB}	—	—	25	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC1}	—	—	50	mA	$\overline{CE}$ = V_{IL}, Iout = 0 mA
	I_{CC2}	—	—	110	mA	f = 12 MHz, Iout = 0 mA
	I_{CC3}	—	—	25	mA	f = 1 MHz, Iout = 0 mA,
Input low voltage	V_{IL}	−0.3*1	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} +1.0*2	V	
Output low voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = −400 µA

Notes: 1. V_{IL} min = −1.0 V for pulse width ≤ 50 ns
2. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 5%, V_{PP} = V_{CC})

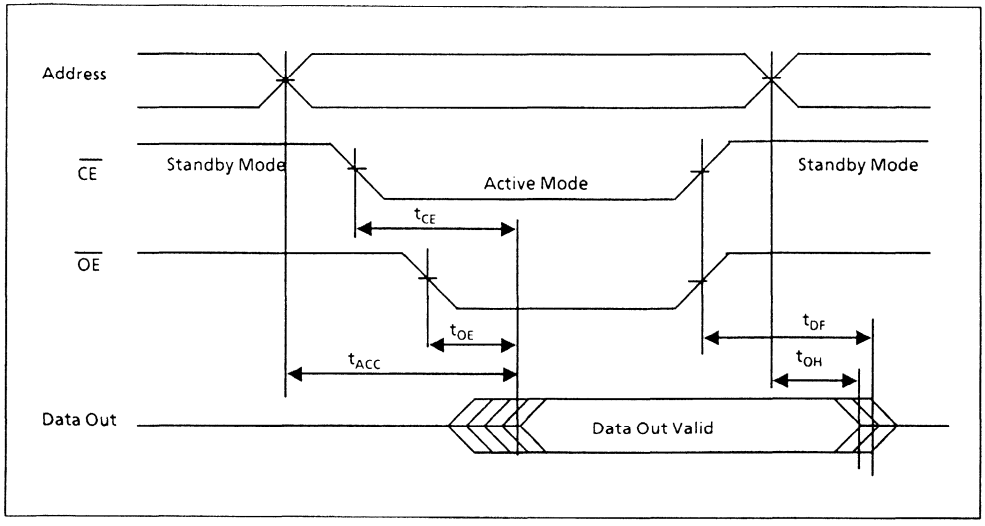
Test Conditions

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL gate + 100 pF
- Reference levels for measuring timing:
  Inputs; 1.5 V
  Outputs; 1.5 V

		HN27C1024H -85		HN27C1024H -10		HN27C1024H -12		HN27C1024H -15			
Item	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	85	—	100	—	120	—	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	85	—	100	—	120	—	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	45	—	50	—	60	—	60	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	30	0	50	0	50	0	50	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0	—	0	—	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

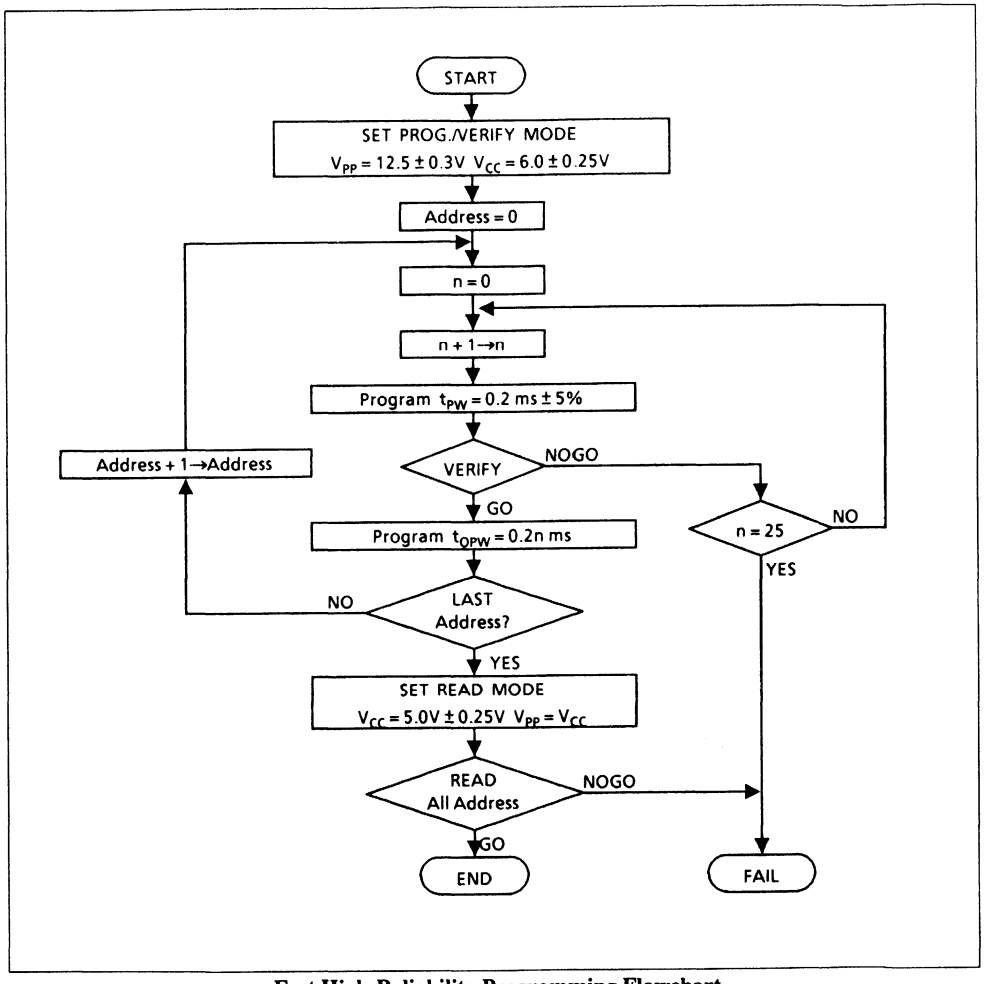
Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Item	Symbol	Min	Typ	Max	Unit	Test condition
Input leakage current	I_{LI}	—	—	2	µA	Vin = 6.25 V/0.45 V
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA
Operating Vcc current	I_{CC}	—	—	50	mA	
Input low level	V_{IL}	–0.1[*5]	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC}+0.5[*6]	V	
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta=25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

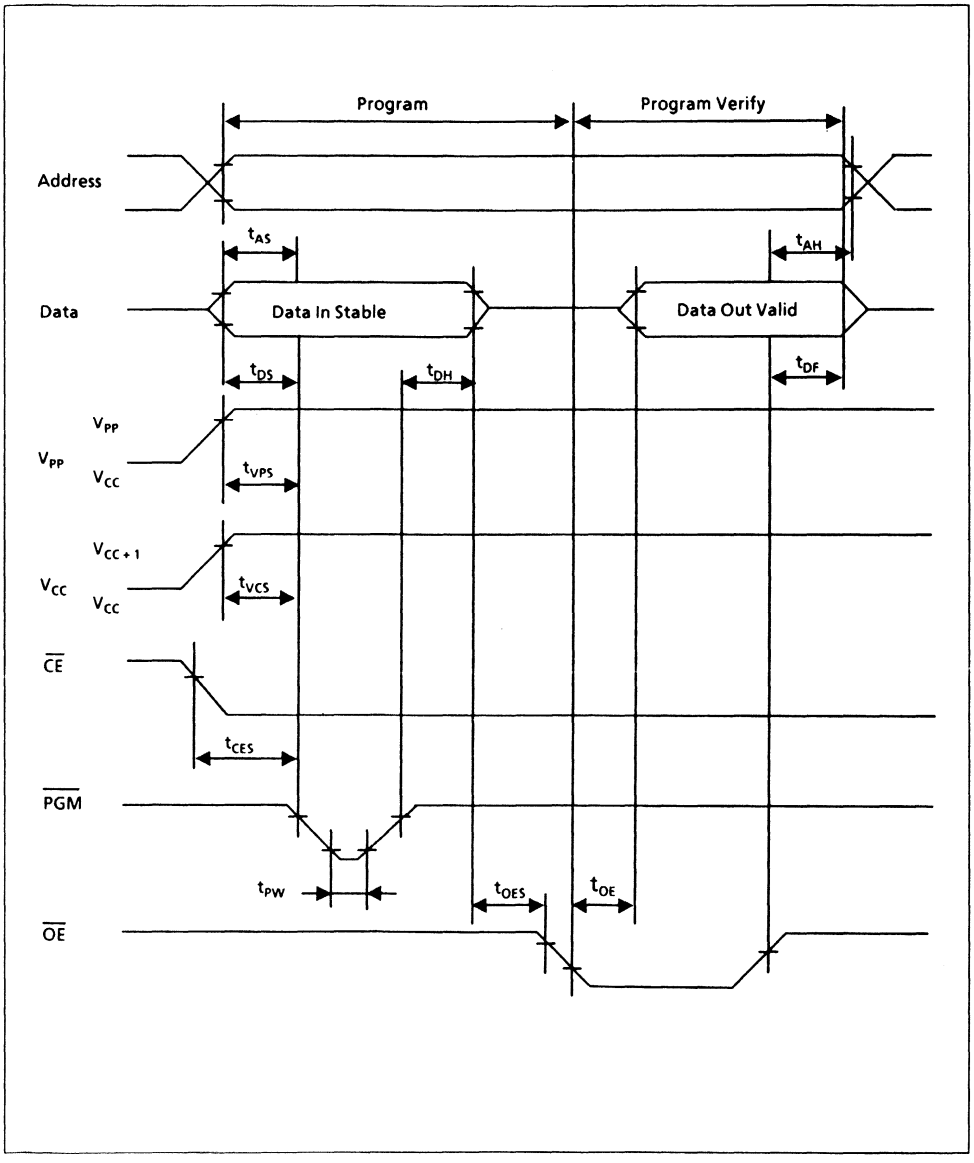
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing:
  Inputs: 0.8 V, 2.0 V
  Outputs: 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	µs
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs
Data setup time	t_{DS}	2	—	—	µs
Address hold time	t_{AH}	0	—	—	µs
Data hold time	t_{DH}	2	—	—	µs
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	µs
V_{CC} setup time	t_{VCS}	2	—	—	µs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns

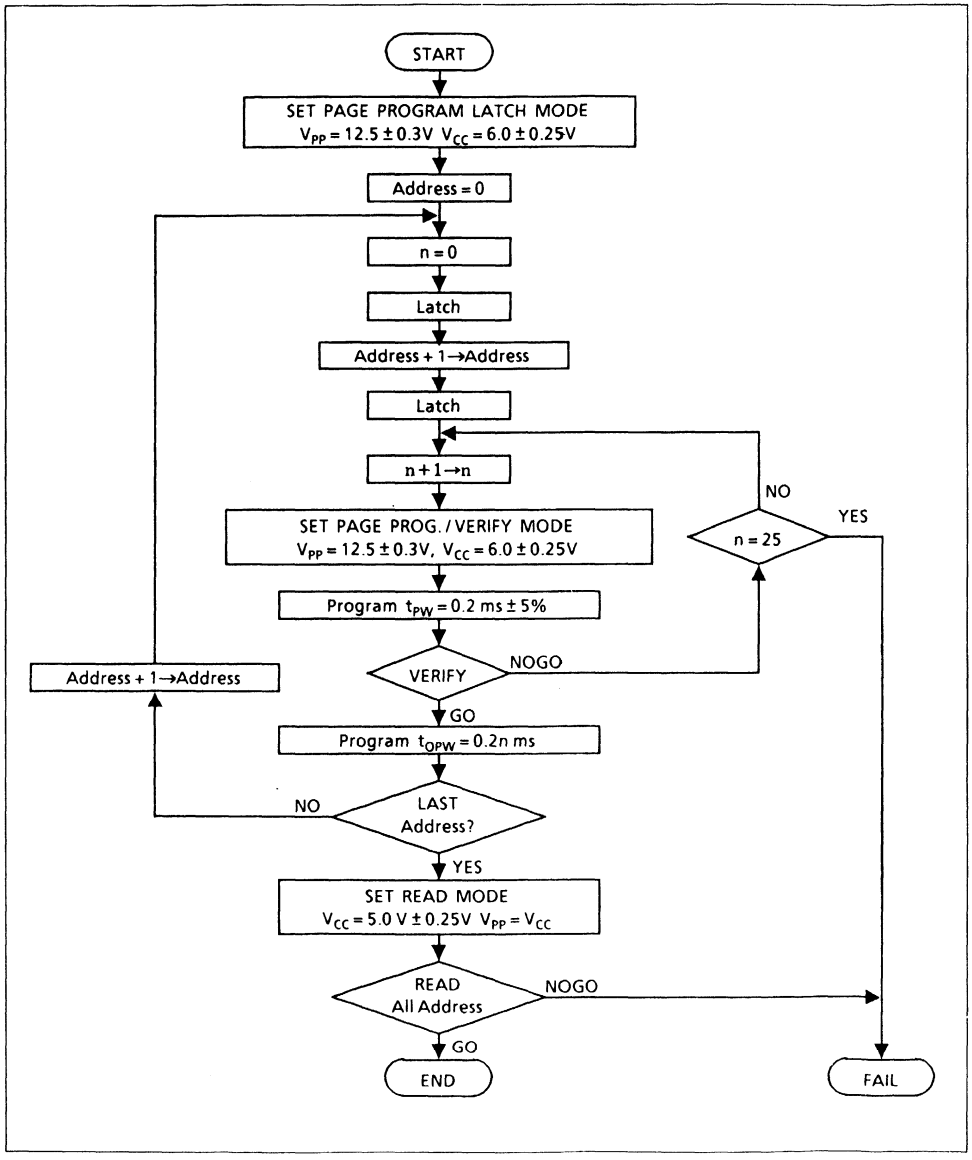
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Programming Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 6.25 V/0.45 V
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA
Operating Vcc current	I_{CC}	—	—	50	mA	
Input low level	V_{IL}	–0.1*5	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC}+0.5*6	V	
V_{PP} supply current	I_{PP}	—	—	50	mA	$\overline{PGM}$ = V_{IL}

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta=25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

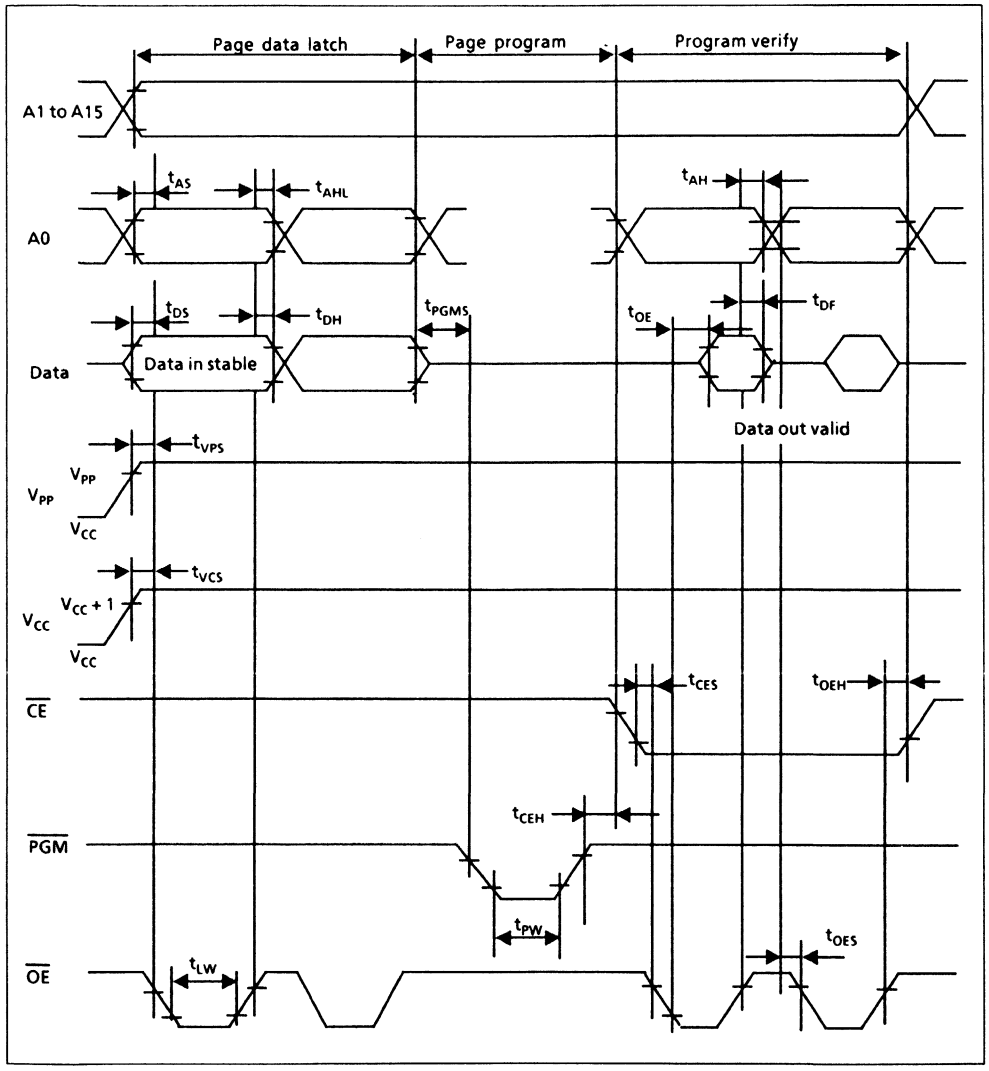
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall rimes: ≤ 20 ns
- Reference levels for measuring timing:
  Inputs; 0.8 V, 2.0 V
  Outputs; 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	µs
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs
Data setup time	t_{DS}	2	—	—	µs
Address hold time	t_{AH}	0	—	—	µs
	t_{AHL}	2	—	—	µs
Data hold time	t_{DH}	2	—	—	µs
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	µs
V_{CC} setup time	t_{VCS}	2	—	—	µs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns
$\overline{OE}$ pulse width during data latch	t_{LW}	1	—	—	µs
$\overline{PGM}$ setup time	t_{PGMS}	2	—	—	µs
$\overline{CE}$ hold time	t_{CEH}	2	—	—	µs
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Page Programming Timing Waveform



Erase

Erasure of HN27C1024H is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W. sec/cm^2.

Mode Description

Device Identifier Mode

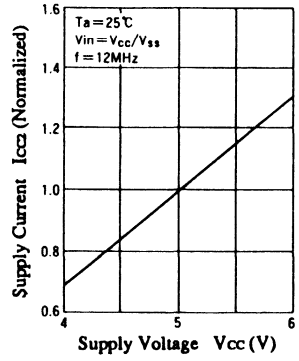
The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C1024H Identifier Code

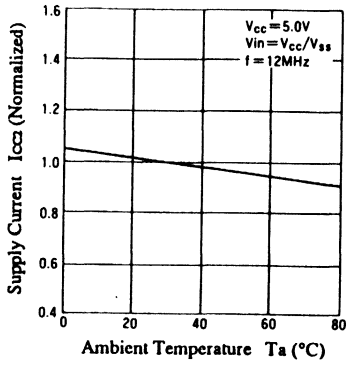
	Pin	A0	I/O8 to I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	
	DG – 40A	(21)	(10) to (3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	
Identifier	CC – 44	(24)	(11) to (4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	Data Hex
Manufacturer code		V_{IL}	×	0	0	0	0	0	1	1	1	07
Device code		V_{IH}	×	1	0	1	1	1	0	1	0	BA

Note: ×; Don't care, A9 = 12.0 V ± 0.5 V, A1 – A8, A10 – A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}

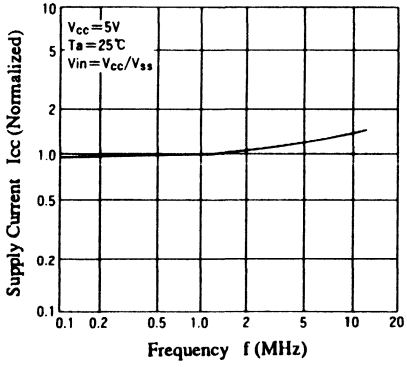
Supply Current vs. Supply Voltage



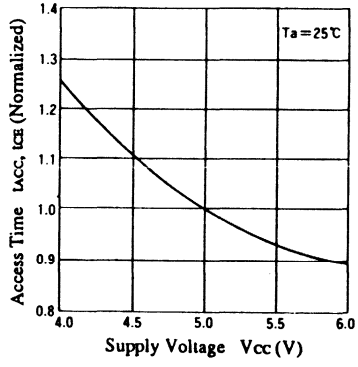
Supply Current vs. Ambient Temperature



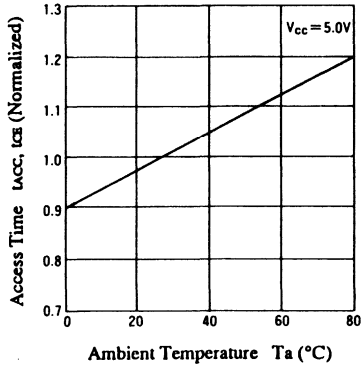
Supply Current vs. Frequency



Access Time vs. Supply Voltage



Access Time vs. Ambient Temperature

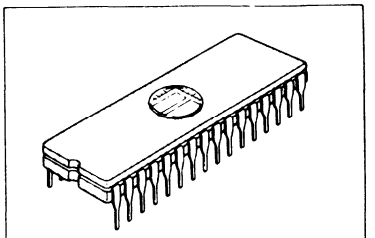


HN27C101G Series

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Fast High-Reliability Program Mode and Fast High-Reliability Page Program Mode . . . . . Program Voltage: +12.5V DC . . . . . Fast High-Reliability Programming Available
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible during Both Read and Program Modes
- Access Time . . . . . 170/200/250ns (max.)
- Low power Dissipation . . 50mW/MHz typ. (Active Mode) 5μW typ. (Standby Mode)
- Pin Arrangement . . . . . 32-Pin JEDEC Standard

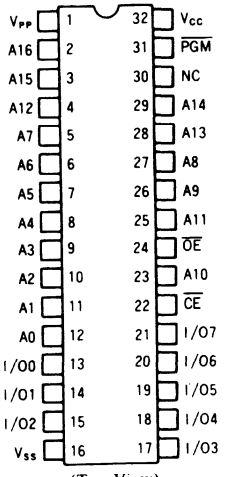


(DG-32)

■ ORDERING INFORMATION

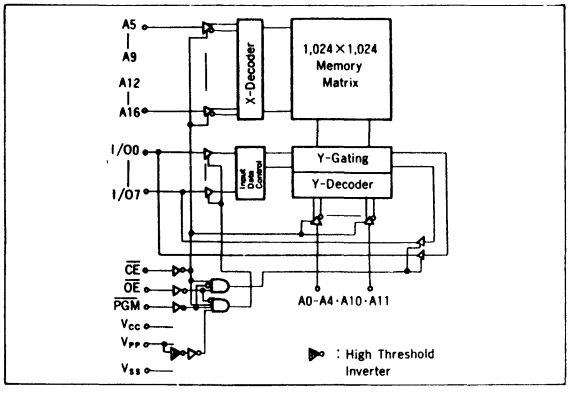
Type No.	Access Time	Package
HN27C101G-17	170ns	600-mil 32-pin Cerdip
HN27C101G-20	200ns	
HN27C101G-25	250ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13~15, 17~21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) 1. X: Don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0V for pulse width ≦ 50ns.

■ READ OPERATION

• DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC}=5V ±5%, V_{PP}=V_{CC})

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}=5.25V	–	–	2	μA
Output Leakage Current	I_{LO}	V_{out}=5.25V/0.45V	–	–	2	μA
V_{PP} Current	I_{PP1}	V_{PP}=5.5V	–	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE}$=V_{IH}	–	–	1	mA
	I_{SB2}	$\overline{CE}$=V_{CC} ±0.3V	–	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE}$=V_{IL}, I_{out}=0mA	–	–	30	mA
	I_{CC2}	f=5MHz, I_{out}=0mA	–	–	30	mA
	I_{CC3}	f=1MHz, I_{out}=0mA	–	–	15	mA
Input Low Voltage	V_{IL}		−0.3*1	–	0.8	V
Input High Voltage	V_{IH}		2.2	–	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.45	V
Output High Voltage	V_{OH}	I_{OH}=−400μA	2.4	–	–	V

Notes) *1. −1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

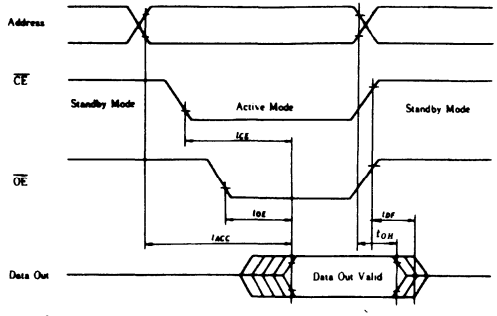
Parameter	Symbol	Test Conditions	HN27C101G-17		HN27C101G-20		HN27C101G-25		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	–	200	–	250	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	70	–	70	–	100	ns
$\overline{OE}$ High to Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	0	–	ns

Note) t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

• Test Condition

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≦ 20ns
Output Load:	1 TTL Gate + 100pF
Reference Levels for Measuring Timing:	Inputs; 0.8V and 2.0V
	Outputs; 0.8V and 2.0V

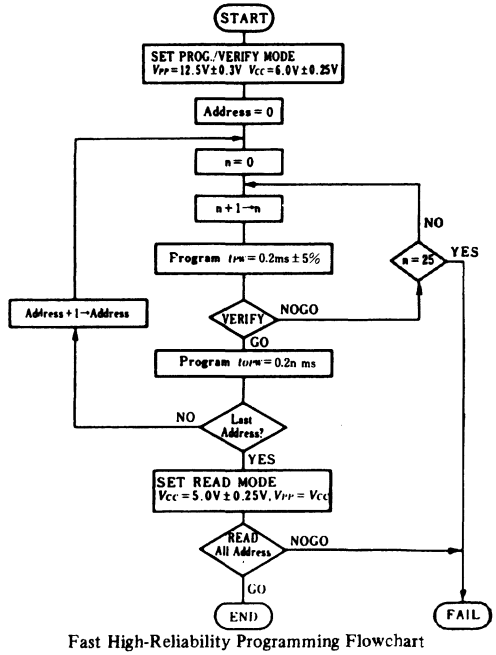


- **CAPACITANCE** (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	10	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	15	pF

■ FAST HIGH-RELIABILITY PROGRAMMING

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = −400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		−0.1*5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5*6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$=V_{IL}	–	–	40	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. −0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS

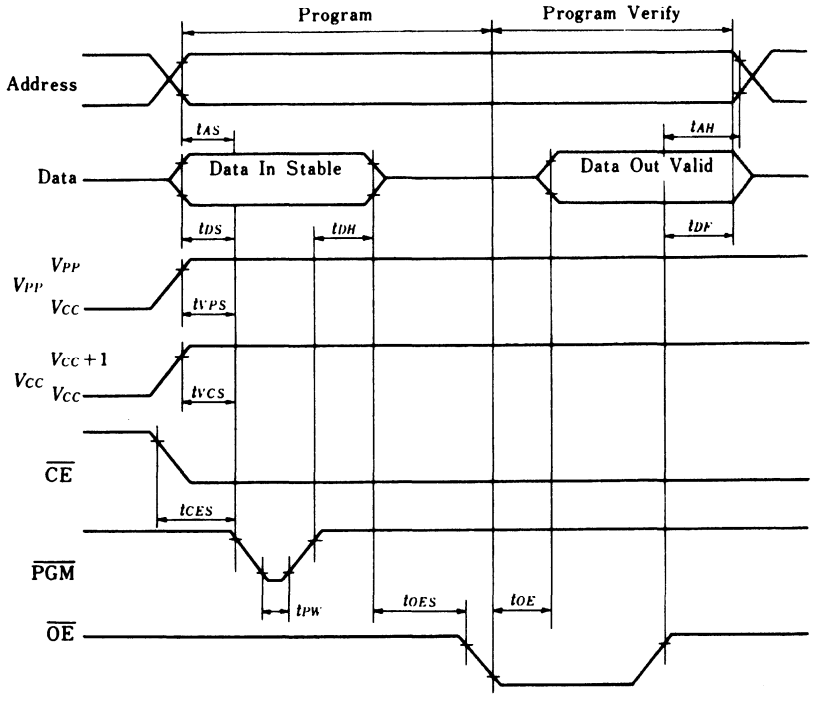
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

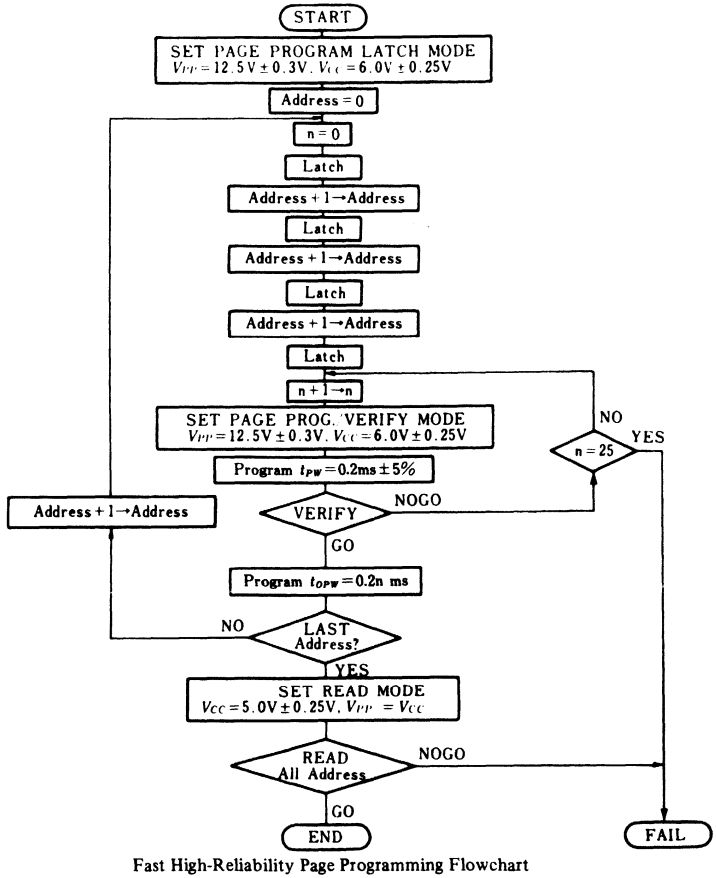
• SWITCHING CHARACTERISTICS

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



■ FAST HIGH-RELIABILITY PAGE PROGRAMMING

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

● DC PROGRAMMING CHARACTERISTICS (T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{in}= 6.25V/0.45V	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH}= –400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		–0.1 *5	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}+0.5 *6	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$=$\overline{OE}$=V_{IH}, $\overline{PGM}$=V_{IL}	–	–	50	mA

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

• AC PROGRAMMING CHARACTERISTICS

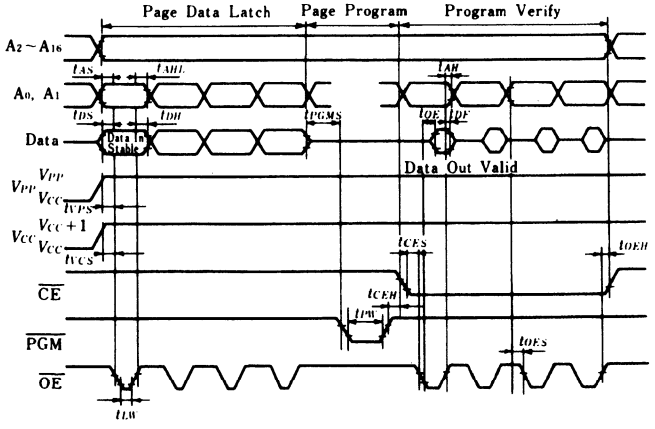
(T_a=25°C ±5°C, V_{CC}=6V ±0.25V, V_{PP}=12.5V ±0.3V)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{OE}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
	t_{AHL}		2	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}		0.19	0.2	0.21	ms
$\overline{PGM}$ Pulse Width during Overprogramming	t_{OPW}*2		0.19	–	5.25	ms
$\overline{CE}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}		0	–	150	ns
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}		1	–	–	μs
$\overline{PGM}$ Setup Time	t_{PGMS}		2	–	–	μs
$\overline{CE}$ Hold Time	t_{CEH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs

Notes: *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

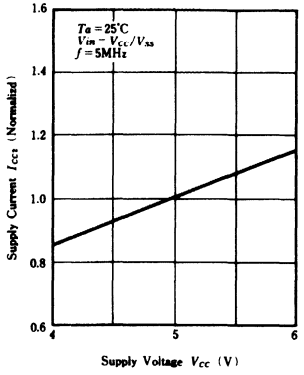
• **Test Condition**
Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



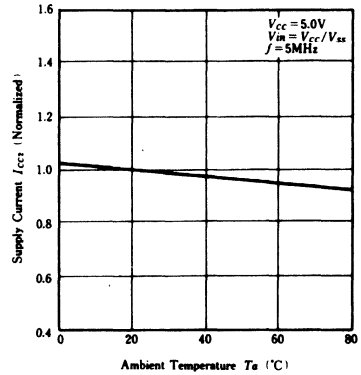
■ ERASE

Erasure of HN27C101G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W•sec/cm^2

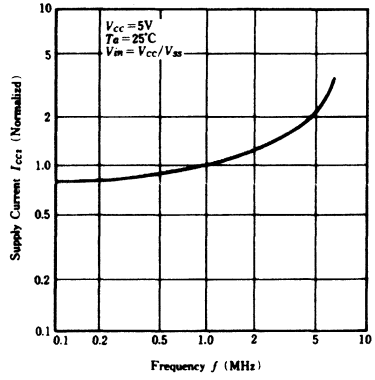
SUPPLY CURRENT vs. SUPPLY VOLTAGE



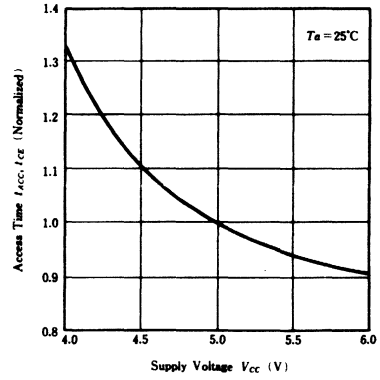
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



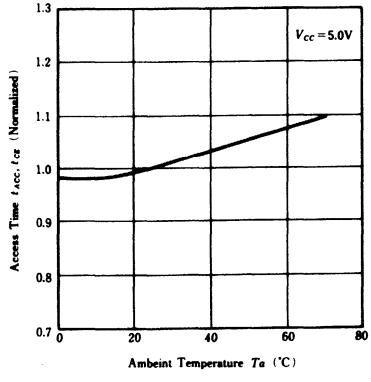
SUPPLY CURRENT vs. FREQUENCY



ACCESS TIME vs. SUPPLY VOLTAGE



ACCESS TIME vs. AMBIENT TEMPERATURE



HN27C101AG Series

131072-Word × 8-Bit CMOS UV Erasable and Programmable ROM

The Hitachi HN27C101AG is a 1-Mbit ultraviolet erasable and electrically programmable ROM. This device is packaged in a 32-pin dual-in-line package with transparent lid. The transparent lid allows the memory content to be erased with ultraviolet light, whereby a new pattern can then be written into the device.

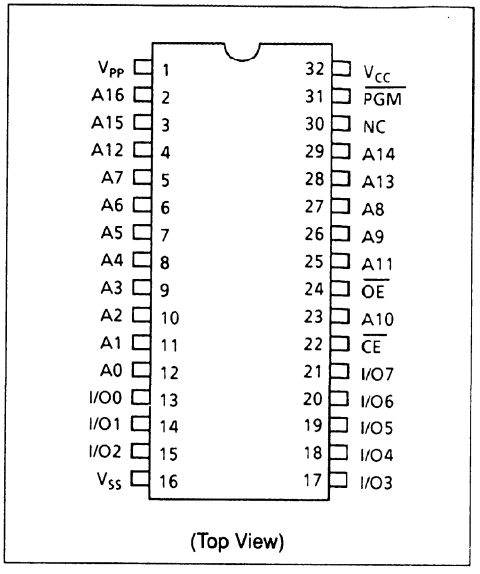
Features

- Single power supply: +5 V ± 5%
  (HN27C101AG-10)
  +5 V ± 10%
  (HN27C101AG-12/15)
- Fast high-reliability programming mode and fast high-reliability page programming mode
  – Programming voltage: +12.5 V DC
  – Fast high-reliability page programming:
  14 sec typ
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 50 mW/MHz typ (active)
  5 µW typ (standby)
- Pin arrangement: 32-pin JEDEC standard
- Device identifier mode: manufacturer code and device code
- Fully compatible with HN27C101G series

Ordering Information

Type No.	Access time	Package
HN27C101AG-10	100 ns	600-mil 32-pin cerdip (DG-32)
HN27C101AG-12	120 ns	
HN27C101AG-15	150 ns	
HN27C101AG-17	170 ns	
HN27C101AG-20	200 ns	
HN27C101AG-25	250 ns	

Pin Arrangement

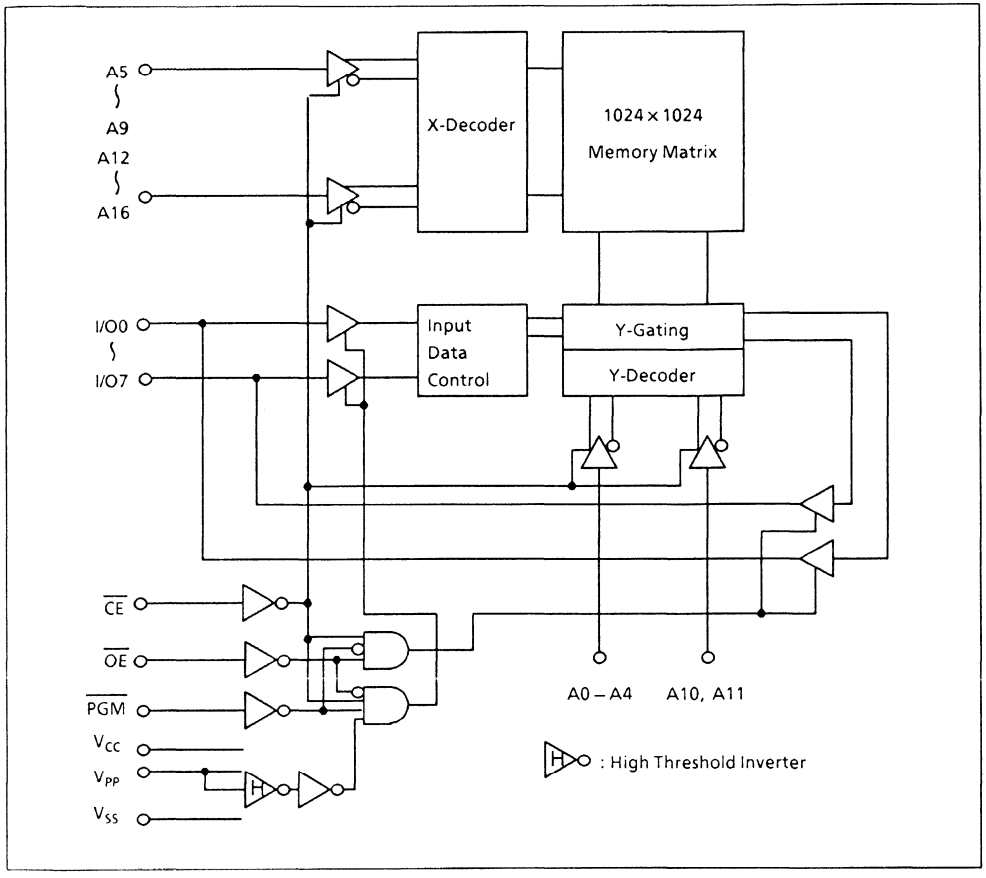


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	CE (22)	OE (24)	PGM (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	×	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	V_{IH}	×	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	×	×	×	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Din
Program verify	V_{IL}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Dout
Page data latch	V_{IH}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din

Mode Selection (cont)

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13-15, 17-21)
Page program	V_{IH}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
Program inhibit	V_{IL}	V_{IL}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
	V_{IL}	V_{IH}	V_{IH}				
	V_{IH}	V_{IL}	V_{IL}				
	V_{IH}	V_{IH}	V_{IH}				
Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code

Notes: 1. × = Don't care
2. V_H = 12.0 V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–65 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}
2. Vin, Vout and V_{ID} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	10	pF	Vin = 0 V
Output capacitance	Cout	—	—	15	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 5 V ± 5% (HN27C101AG-10), V_{CC} = 5 V ± 10% (HN27C101AG-12/15/17/20/25), V_{PP} = V_{CC}, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = 0 V to V_{CC}
V_{PP} current	I_{PP1}	—	1	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
Operating V_{CC} current	I_{CC1}	—	—	30	mA	$\overline{CE}$ = V_{IL}, Iout = 0 mA
	I_{CC2}	—	—	30	mA	f = 5 MHz, Iout = 0 mA
		—	—	50	mA	f = 10 MHz, Iout = 0 mA
Input low voltage	V_{IL}	–0.3*1	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} +1.0*2	V	
Output low voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
		V_{CC} –0.7	—	—	V	I_{OH} = –0.1 mA

Notes: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns
2. V_{IH} max = V_{CC} +1.5 V for pulse width ≤ 20 ns
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (V_{CC} = 5 V ± 5% (HN27C101AG-10), V_{CC} = 5 V ± 10% (HN27C101AG-12/15/17/20/25), V_{PP} = V_{CC}, Ta = 0 to +70°C)

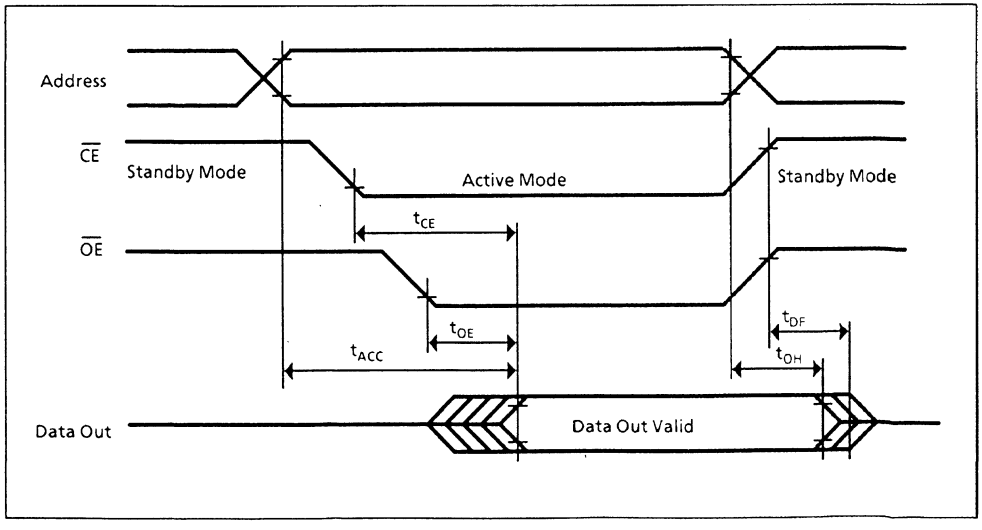
Test Condition

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V Outputs; 0.8 V and 2.0 V

		HN27C101AG													
		-10		-12		-15		-17		-20		-25			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	100	—	120	—	150	—	170	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	100	—	120	—	150	—	170	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	60	—	60	—	70	—	70	—	70	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	50	0	60	0	50	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0	—	0	—	0	—	0	—	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

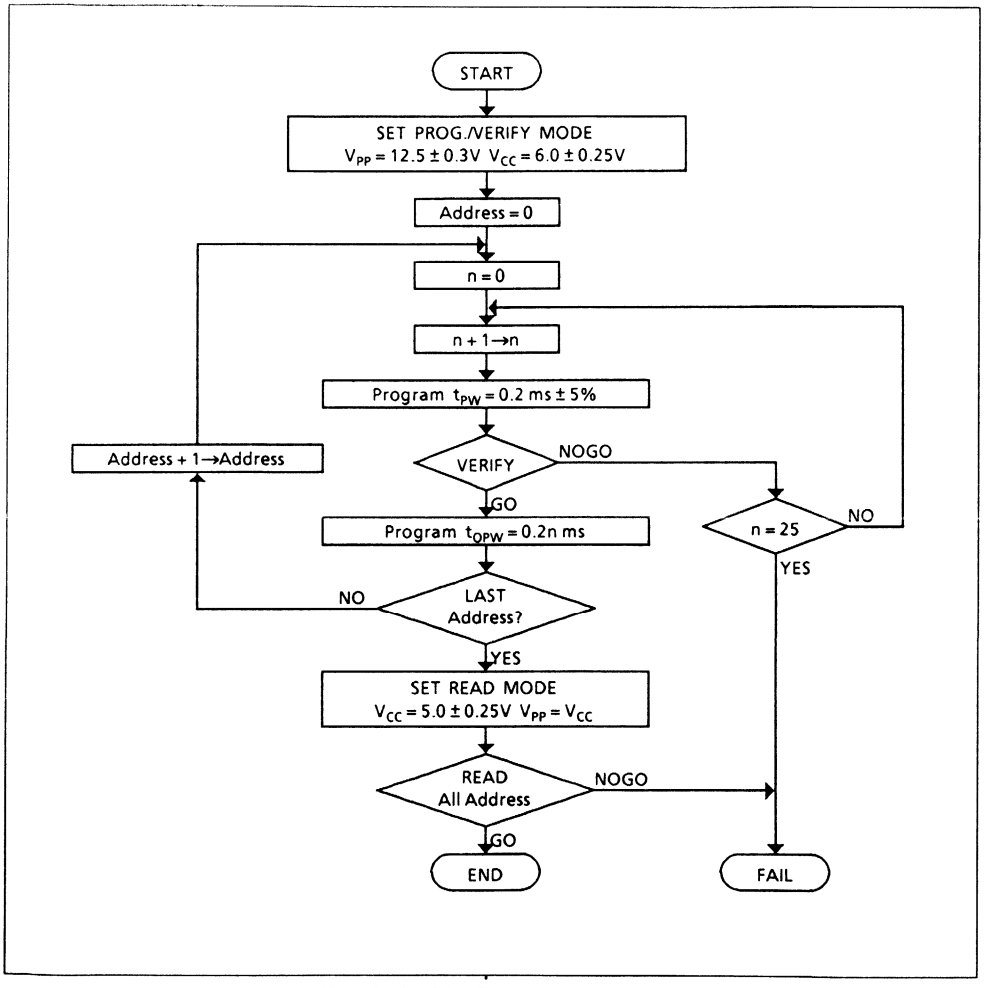
Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25 °C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1*5	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5*6	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

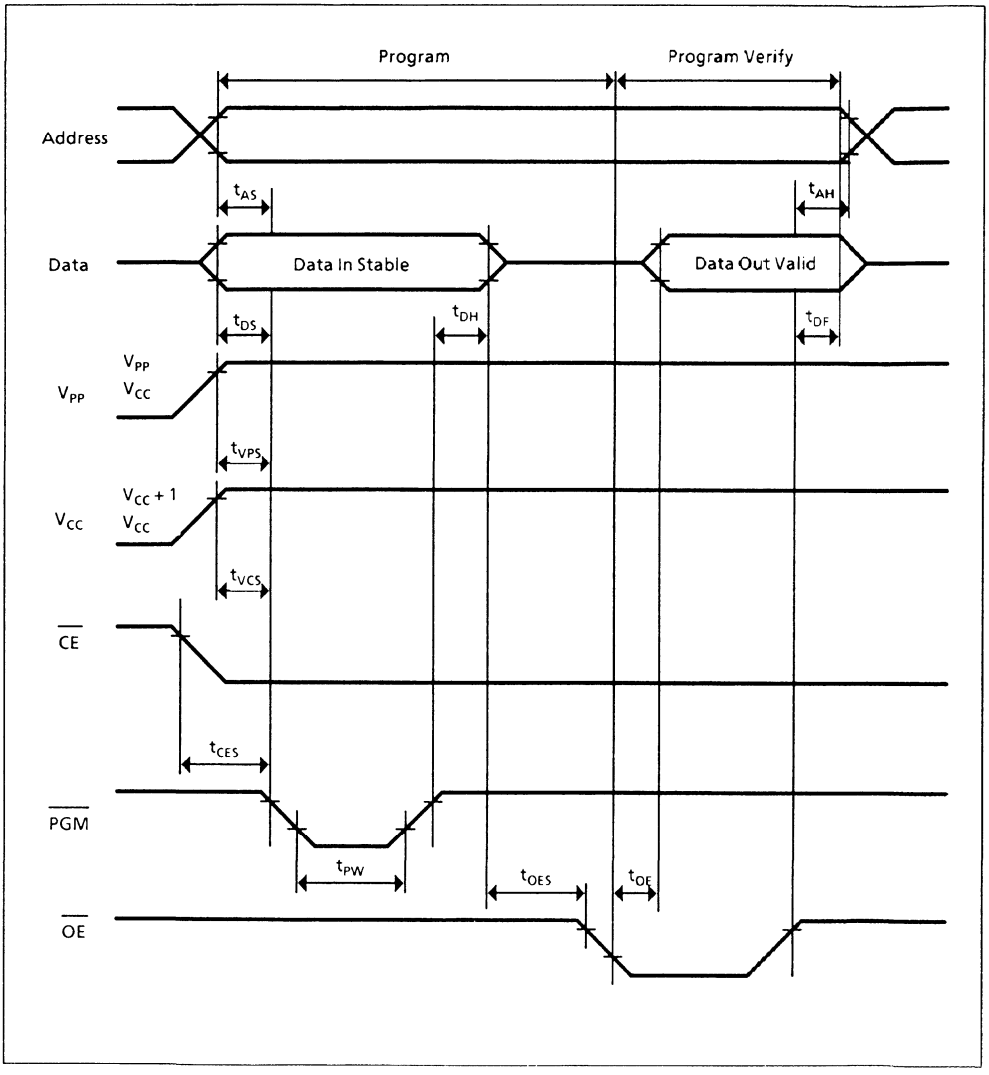
Test Condition

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing:
  Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	

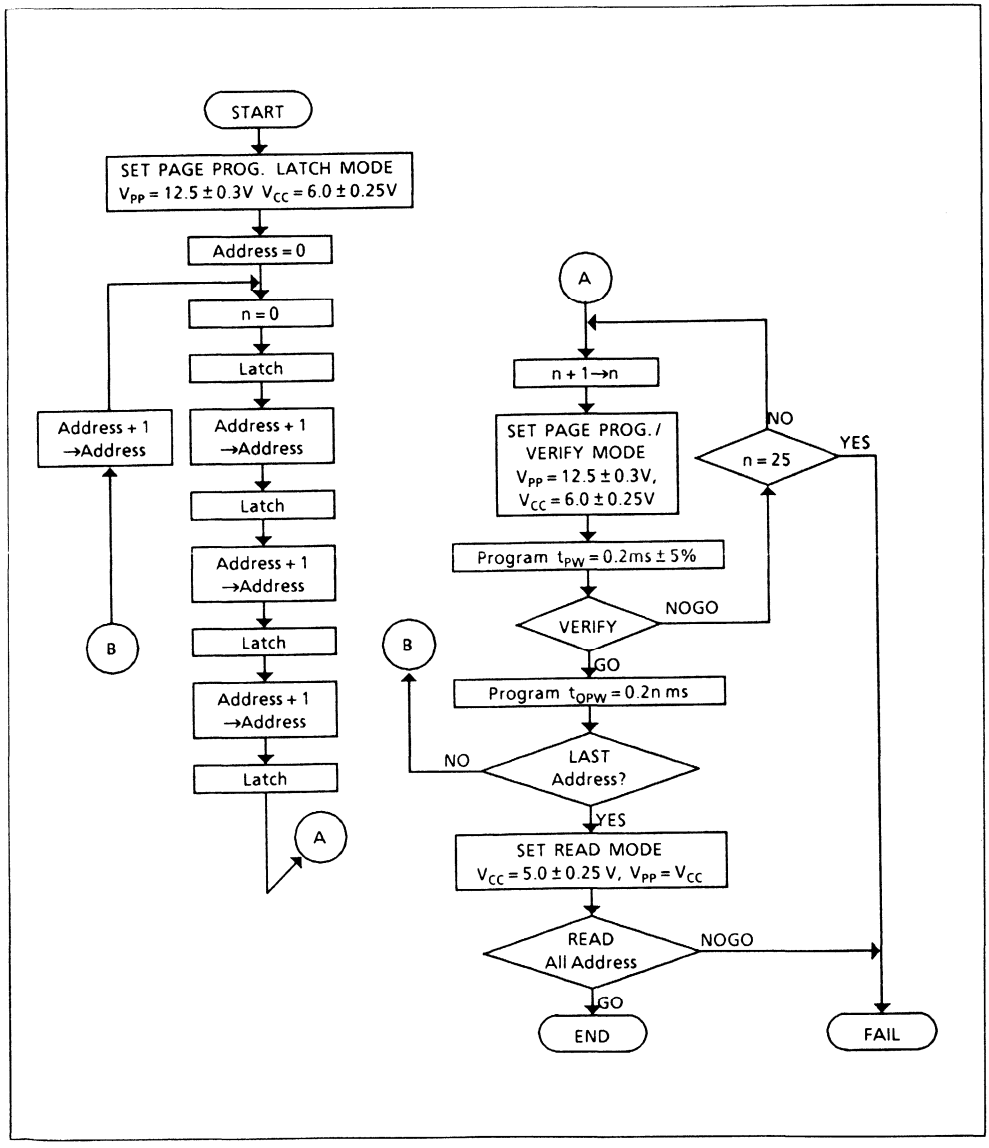
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Programming Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Characteristics (Ta = 25 °C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	50	mA	$\overline{CE}$ = $\overline{OE}$= V_{IH}, $\overline{PGM}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1*5	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5*6	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

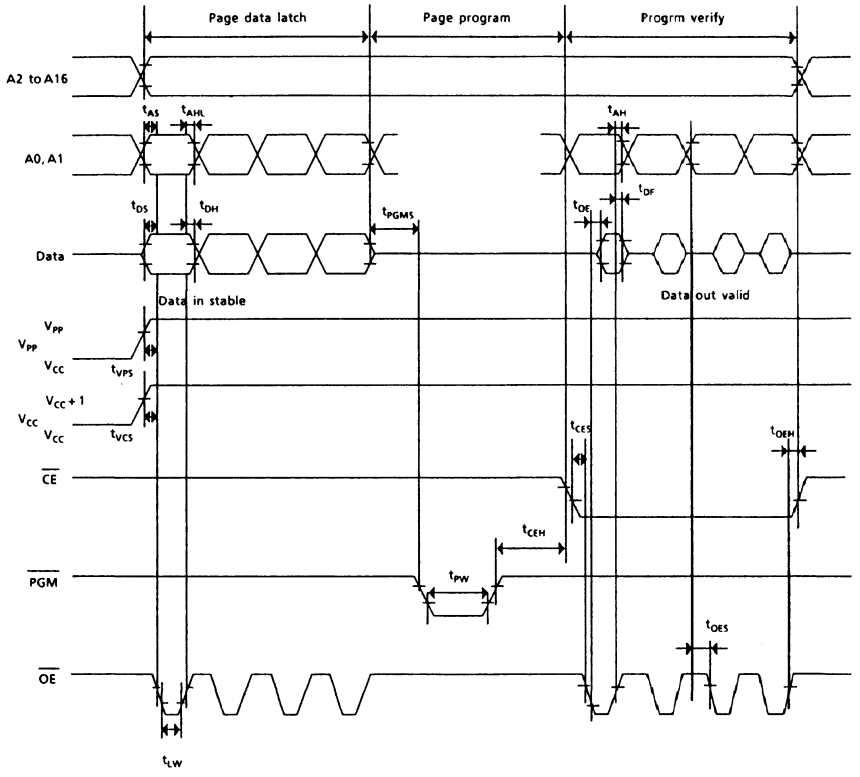
Test condition

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing:
  Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	µs
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs
Data setup time	t_{DS}	2	—	—	µs
Address hold time	t_{AH}	0	—	—	µs
	t_{AHL}	2	—	—	µs
Data hold time	t_{DH}	2	—	—	µs
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	µs
V_{CC} setup time	t_{VCS}	2	—	—	µs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns
$\overline{OE}$ pulse width during data latch	t_{LW}	1	—	—	µs
$\overline{PGM}$ setup time	t_{PGMS}	2	—	—	µs
$\overline{CE}$ hold time	t_{CEH}	2	—	—	µs
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Page Programming Timing Waveform



Erase

Erasure of this device is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W. sec/cm^2.

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C101AG Identifier Code

Identifier	A0 (12)	A9 (26)	I/O7 (21)	I/O6 (20)	I/O5 (19)	I/O4 (18)	I/O3 (17)	I/O2 (15)	I/O1 (14)	I/O0 (13)	Hex Data
Manufacturer code	V_{IL}	V_H	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	V_H	0	0	1	1	1	0	0	0	38

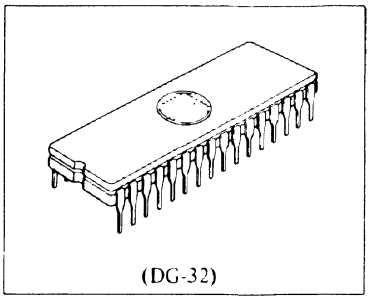
Notes: 1. $V_H = 12.0\ V \pm 0.5\ V$
2. A1–A8, A10–A16, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

HN27C301G Series

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- Fast High-Reliability Program Mode and Fast High-Reliability Page Program Mode
  . . . . . Program Voltage: +12.5V DC
  . . . . . Fast High-Reliability Programming Available
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 170/200/250ns (max.)
- Low power Dissipation . . 50mW/MHz typ. (Active Mode)
  5μW typ. (Standby Mode)
- Pin Arrangement : Replaceable 1-Mbit Mask ROM (28-Pin type)

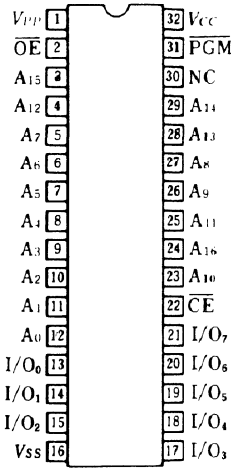


(DG-32)

■ ORDERING INFORMATION

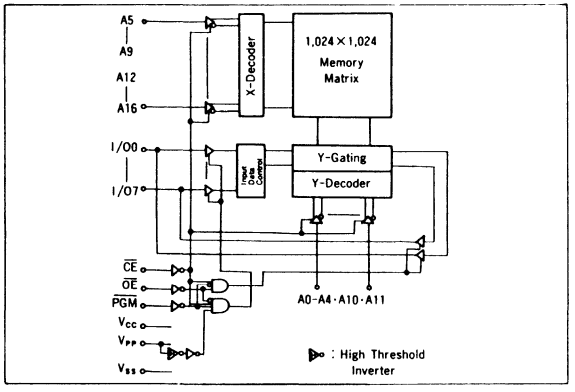
Type No.	Access Time	Package
HN27C301G-17	170ns	600 mil 32 pin Cerdip
HN27C301G-20	200ns	
HN27C301G-25	250ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (2)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13~15, 17~21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) *1. X: Don't care

■ ELECTRICAL CHARACTERISTICS

Refer to the HN27C101G data sheet.

HN27C301AG Series

131072-Word × 8-Bit CMOS UV Erasable and Programmable ROM

The Hitachi HN27C301AG is a 1-Mbit ultraviolet erasable and electrically programmable ROM. This device is packaged in a 32-pin dual-in-line package with transparent lid. The transparent lid allows the memory content to be erased with ultraviolet light, whereby a new pattern can then be written into the device.

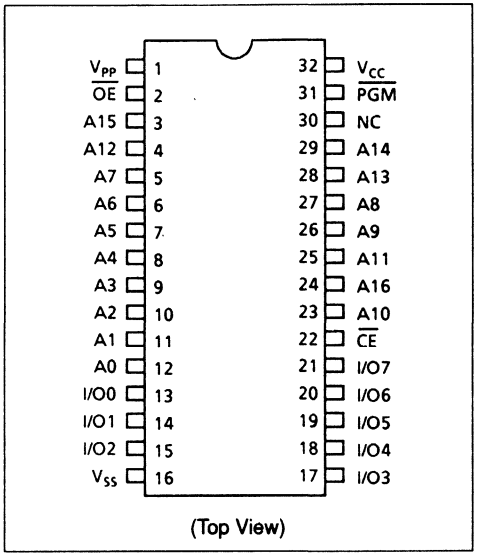
Features

- Single power supply: +5 V ± 5%
  (HN27C301AG-10)
  +5 V ± 10%
  (HN27C301AG-12/15)
- Fast high-reliability programming mode and Fast high-reliability page programming mode
  Programming voltage: +12.5 V DC
  Fast high-reliability page programming:
  14 sec typical
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 50 mW/MHz typ
  (active)
  5 µW typ (standby)
- Pin Arrangement: replaceable Mask ROM
  (32-pin)
- Device identifier mode: manufacturer code and device code
- Fully compatible with HN27C301G Series

Ordering Information

Type No.	Access time	Package
HN27C301AG-10	100 ns	600-mil 32-pin cerdip (DG-32)
HN27C301AG-12	120 ns	
HN27C301AG-15	150 ns	
HN27C301AG-17	170 ns	
HN27C301AG-20	200 ns	
HN27C301AG-25	250 ns	

Pin Arrangement

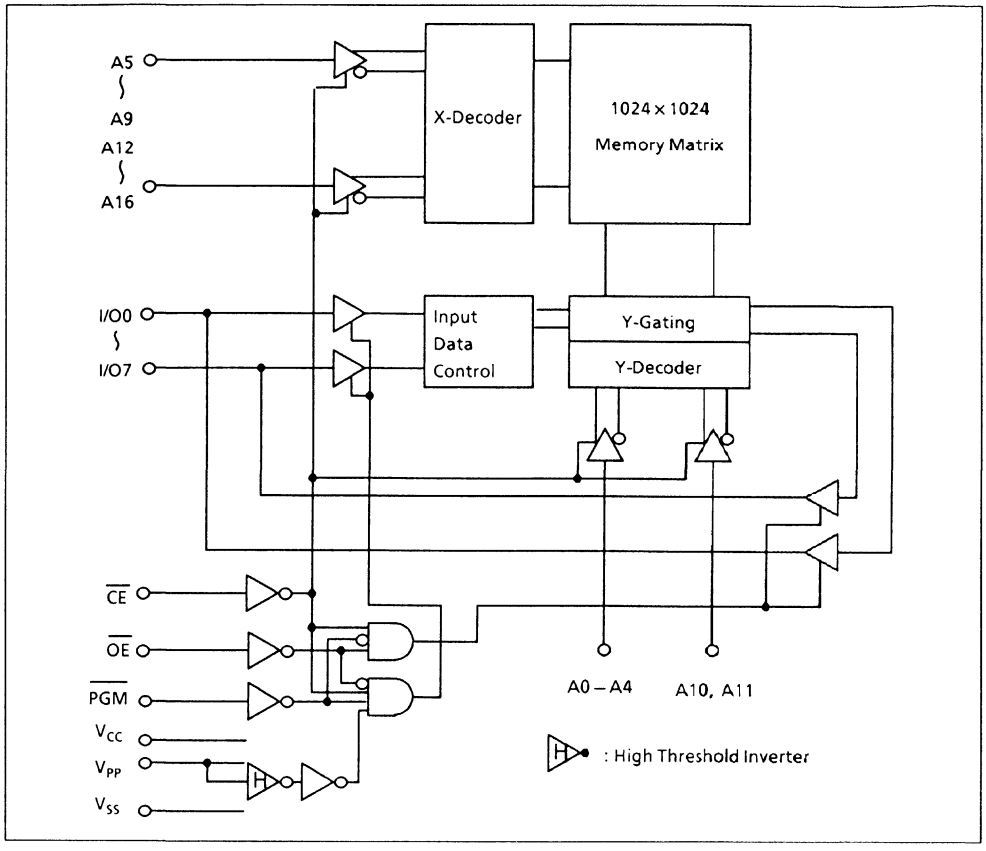


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (2)	$\overline{PGM}$ (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13-15, 17-21)
Read	V_{IL}	V_{IL}	V_{IH}	×	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	V_{IH}	×	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	×	×	×	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Din
Program verify	V_{IL}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Dout
Page data latch	V_{IH}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din

Mode Selection (cont)

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (2)	$\overline{PGM}$ (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13-15, 17-21)
Page program	V_{IH}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
Program inhibit	V_{IL}	V_{IL}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
	V_{IL}	V_{IH}	V_{IH}				
	V_{IH}	V_{IL}	V_{IL}				
	V_{IH}	V_{IH}	V_{IH}				
Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code

Notes: 1. × = Don't care
2. $V_H = 12.0\ V \pm 0.5\ V$

Electrical Characteristics

Refer to the HN27C101AG data sheet.

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C301AG Identifier Code

Identifier	A0 (12)	A9 (26)	I/07 (21)	I/06 (20)	I/05 (19)	I/04 (18)	I/03 (17)	I/02 (15)	I/01 (14)	I/00 (13)	Hex data
Manufacturer code	V_{IL}	V_H	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	V_H	1	0	1	1	1	0	0	1	B9

Notes: 1. $V_H = 12.0\ V \pm 0.5\ V$
2. A1 – A8, A10 – A16, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

HN27C4096 Series — Preliminary

262144-Word×16-Bit CMOS UV Erasable and Programmable ROM

The Hitachi HN27C4096G/CC is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation. Fabricated on advanced fine process and high speed circuitry technique, the HN27C4096 makes high speed access time possible. Therefore, it is suitable for 16/32-bit microcomputer systems using high speed microcomputer such as the 80286 and 68020. The HN27C4096 offers high speed programming using page programming mode. This device has the package variation of cerdip-40pin and JLCC-44 pin.

Features

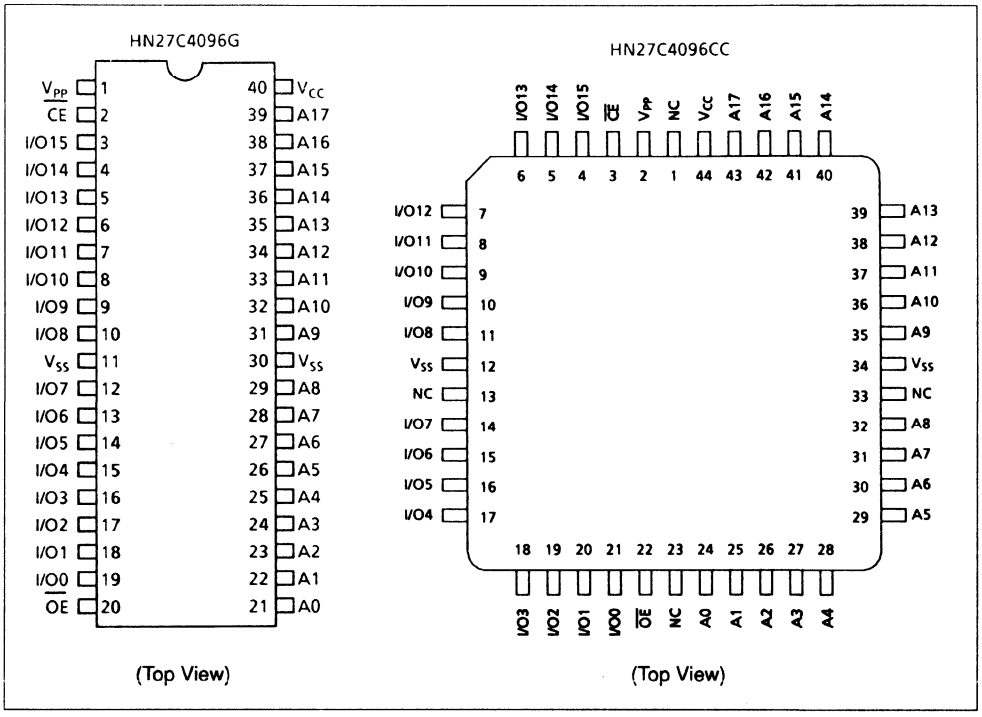
- High speed: Access time 100 ns/120 ns/150 ns (max)
- Low power dissipation:
  Standby mode; 5 μW (typ),
  Active mode; 35 mW/MHz (typ)
- Fast high reliability page programming and fast high-reliability programming:
  Program voltage; +12.5 V DC
  Program time; 3.5 sec (min)
  (Theoretical in Page programming)
- Inputs and outputs TTL compatible during both read and program modes
- Pin arrangement: 40-pin JEDEC standard,
  44-pin JLCC JEDEC standard
- Device identifier mode: Manufacturer code and device code

Ordering Information

Type No.	Access time	Package
HN27C4096G-10	100 ns	600-mil 40-pin cerdip (DG-40A)
HN27C4096G-12	120 ns	
HN27C4096G-15	150 ns	
HN27C4096CC-10	100 ns	44-pin JLCC (CC-44)
HN27C4096CC-12	120 ns	
HN27C4096CC-15	150 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

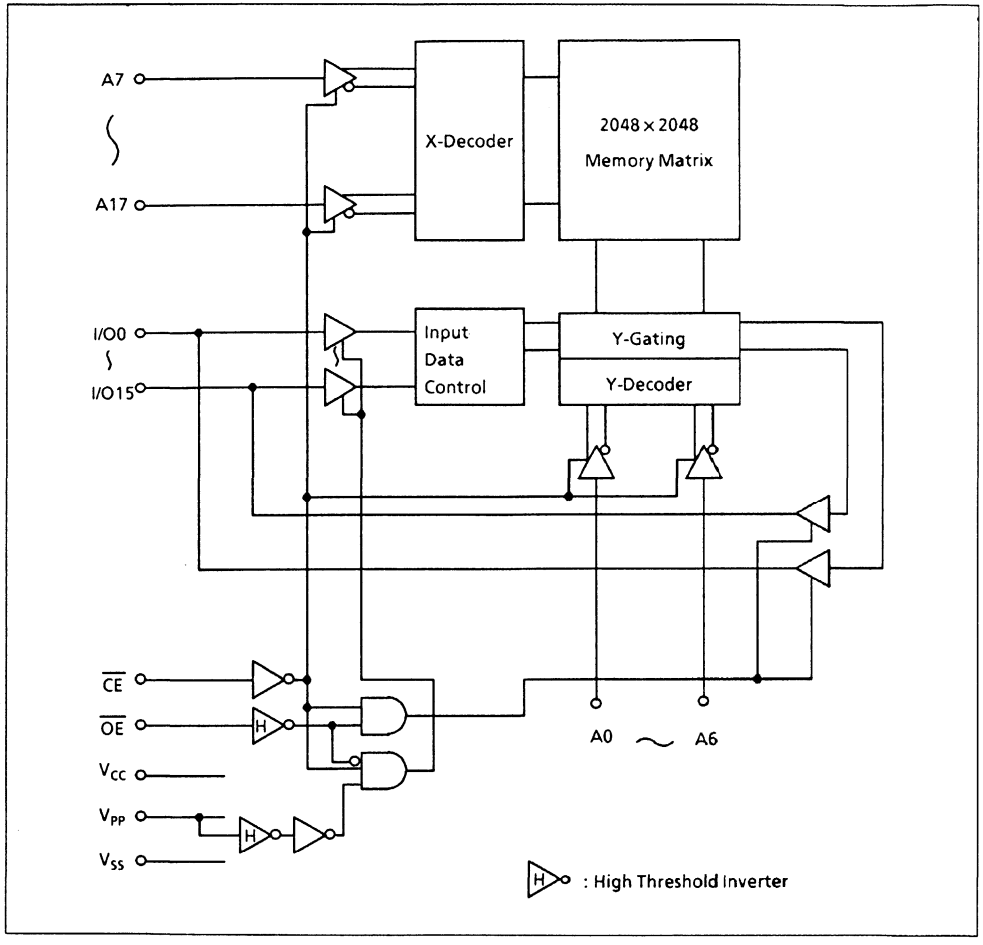
Pin Arrangement



Pin Description

Pin name	Function
A0 – A17	Address
I/O0 – I/O15	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Block Diagram



Mode Selection

	Pin	CE	OE	A9	V_{PP}	V_{CC}	I/O
	CC – 44	(3)	(22)	(35)	(2)	(44)	(4 – 11, 14 – 21)
Mode	DG – 40A	(2)	(20)	(31)	(1)	(40)	(3 – 10, 12 – 19)
Read		V_{IL}	V_{IL}	×	V_{SS} – V_{CC}	V_{CC}	Dout
Output disable		V_{IL}	V_{IH}	×	V_{SS} – V_{CC}	V_{CC}	High-Z
Standby		V_{IH}	×	×	V_{SS} – V_{CC}	V_{CC}	High-Z

Mode Selection (cont)

Mode	Pin	$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	V_{CC}	I/O
	CC – 44	**(3)**	**(22)**	**(35)**	**(2)**	**(44)**	**(4 – 11, 14 – 21)**
	DG – 40A	**(2)**	**(20)**	**(31)**	**(1)**	**(40)**	**(3 – 10, 12 – 19)**
Page prog.	Page program set	V_{IH}	V_H*2	×	V_{PP}	V_{CC}	High-Z
	Page data latch	V_{IL}	V_H*2	×	V_{PP}	V_{CC}	Din
	Page program	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	High-Z
	Page program verify	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Dout
	Page program reset	V_{IH}	V_{IH}	×	V_{CC}	V_{CC}	High-Z
Word prog.	Program	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din
	Program verify	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Dout
	Optional verify	V_{IL}	V_{IL}	×	V_{PP}	V_{CC}	Dout
	Program inhibit	V_{IH}	V_{IH}	×	V_{PP}	V_{CC}	High-Z
Identifier		V_{IL}	V_{IL}	V_H*2	$V_{SS} - V_{CC}$	V_{CC}	Code

Notes: 1. ×: Don't care.
2. V_H: 12.0 V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	Vin, Vout	–0.6*2 to +7.0	V
Voltage on pin A9 and $\overline{OE}$	V_{ID}	–0.6*2 to +13.0	V
V_{PP} voltage *1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage *1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range *3	Tstg	–65 to +125	°C
Storage temperature under bias	Tbias	–20 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = –2.0 V for pulse width ≤ 20 ns
3. Storage temperature range of device before programming.

Capacitance (Ta = 25°C, f = 1 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	12	pF	Vin = 0 V
Output capacitance	Cout	—	—	20	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{SS} to V_{CC}, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	Vout = 5.5 V/0.45 V
V_{PP} current	I_{PP1}	—	1	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	1	20	µA	$\overline{CE}$ = V_{CC} ± 0.3 V
Operating V_{CC} current	I_{CC1}	—	—	30	mA	Iout = 0 mA, f = 1 MHz
	I_{CC2}	—	—	100	mA	Iout = 0 mA, f = 10 MHz
Input voltage	V_{IL}	–0.3*1	—	0.8	V	
	V_{IH}	2.2	—	V_{CC}+1*2	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns
V_{IL} min = –2.0 V for pulse width ≤ 20 ns
2. V_{IH} max = V_{CC} +1.5 V for pulse width ≤ 20 ns
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{SS} to V_{CC}, Ta = 0 to +70°C)

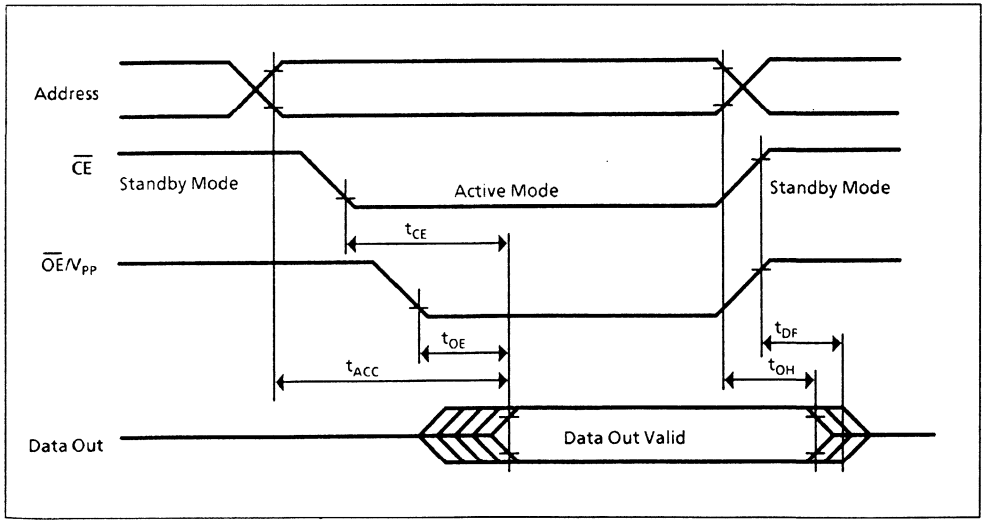
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤ 10 ns
- Output load: 1 TTL gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

Item	Symbol	HN27C4096 -10 Min	HN27C4096 -10 Max	HN27C4096 -12 Min	HN27C4096 -12 Max	HN27C4096 -15 Min	HN27C4096 -15 Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	100	—	120	—	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	100	—	120	—	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	60	—	60	—	70	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float *1	t_{DF}	0	35	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	—	5	—	5	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Page Programming

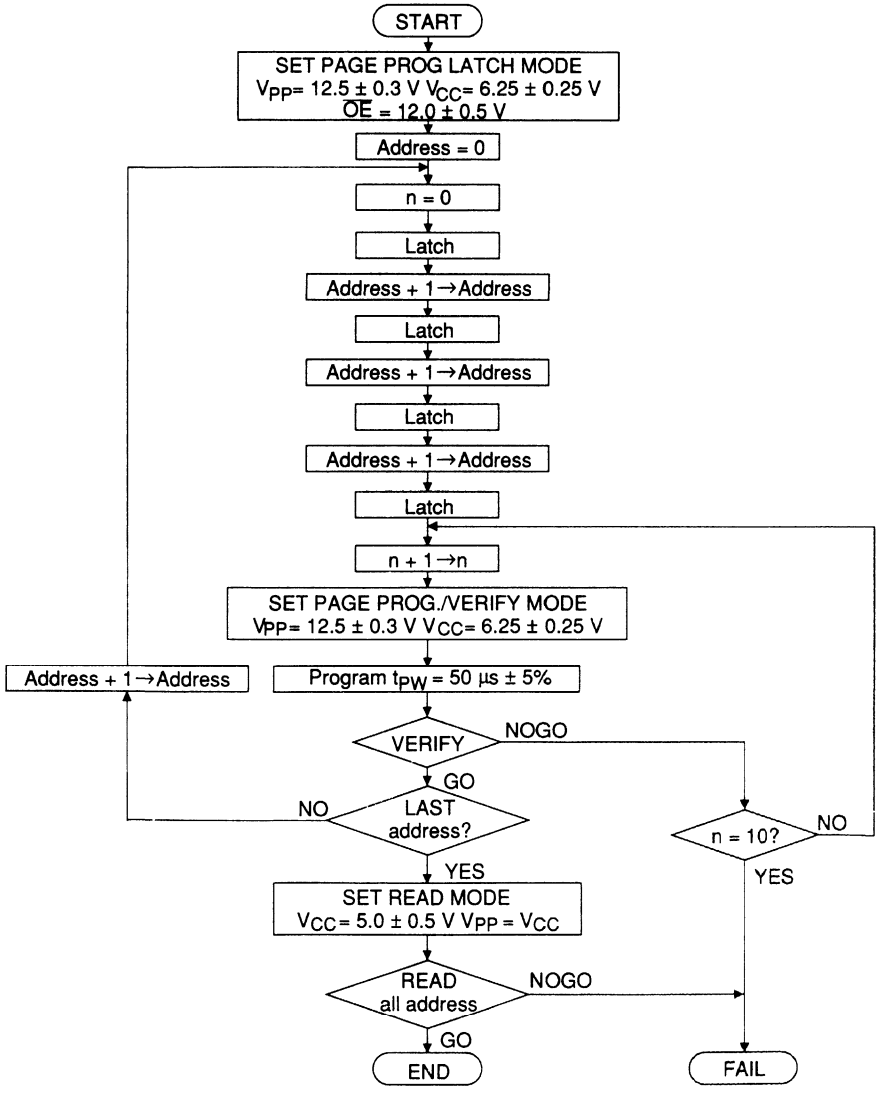
This device can be applied the high performance page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

Page Program Set

Apply 12 V to $\overline{OE}$ pin after applying 12.5 V to V_{PP} to set a page program mode.
The device operates in a page program mode until reset.

Page Program Reset

Set V_{PP} to V_{CC} level or less to reset a page program mode.



Fast High-Reliability Page Programming Flowchart

DC Characteristics (V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 6.5 V/0.45 V
Output voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	–0.1*5	—	0.8	V	
	V_{IH}	2.2	—	V_{CC}+0.5*6	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE}$=V_{IL}

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta=25°C ± 5°C)

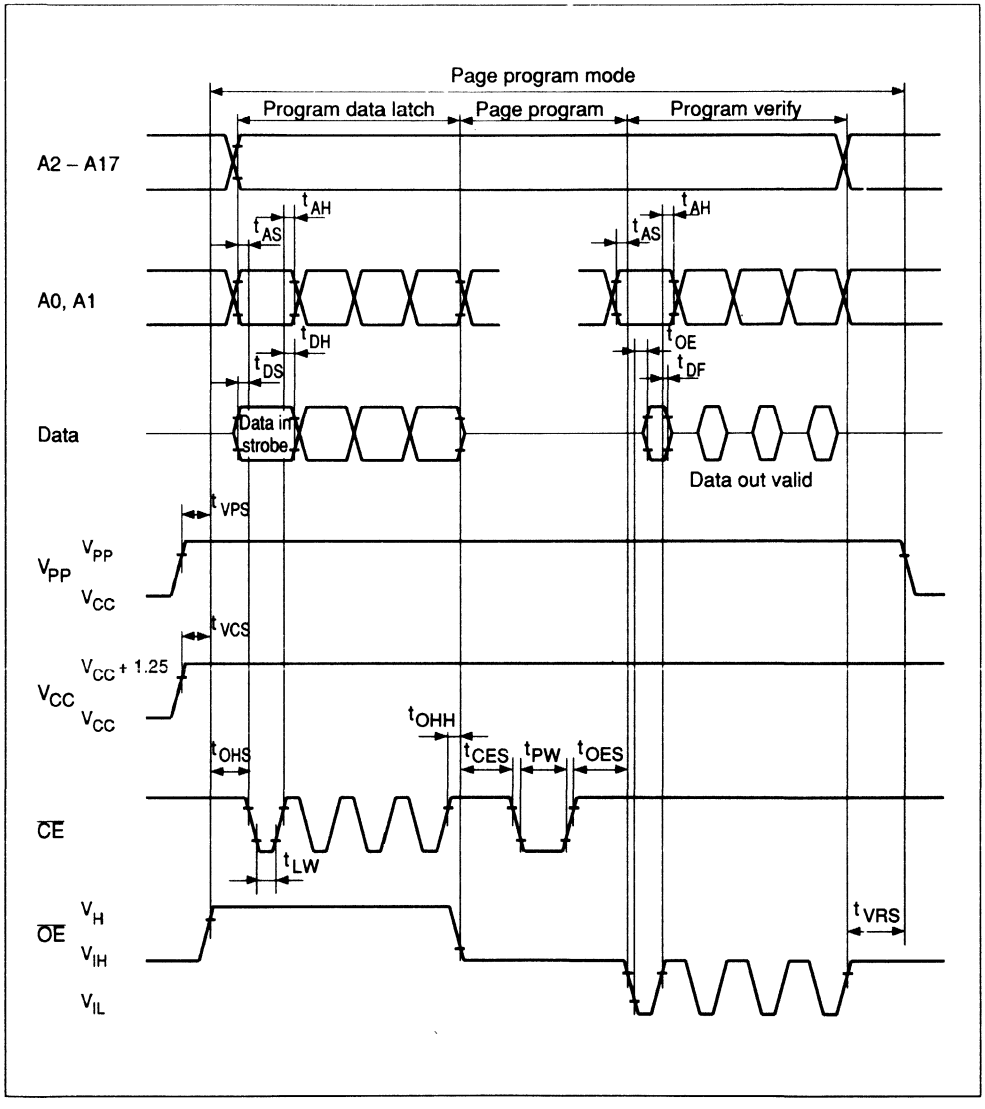
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤20 ns
- Reference levels for measuring timing: Inputs; 0.8 V, 2.0 V, Outputs; 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ high to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{CE}$ initial programming pulse width	t_{PW}	47.5	50.0	52.5	µs	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	t_{LW}	1	—	—	µs	
$\overline{OE}$=V_H setup time	t_{OHS}	2	—	—	µs	
$\overline{OE}$=V_H hold time	t_{OHH}	2	—	—	µs	
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs	
V_{PP} hold time*2	t_{VRS}	1	—	—	µs	

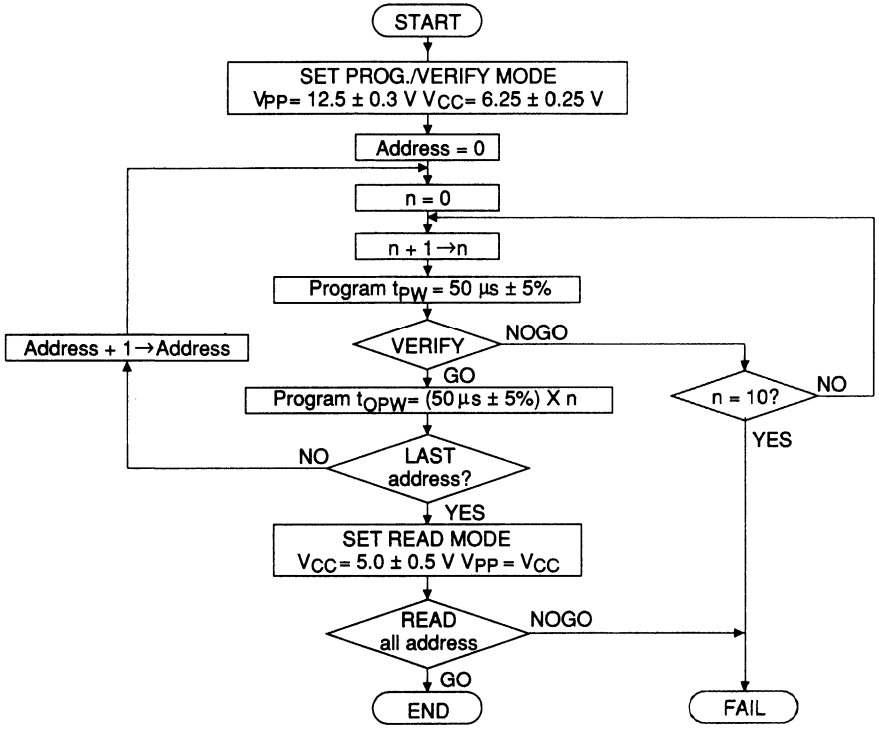
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

Fast High-Reliability Page Programming Timing Waveform



Fast High-Reliability Programming

This device can be applied the fast high-reliability programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (V_{CC} = 6.25 V ± 0.25 V, V_{PP} =12.5 V ± 0.3 V, Ta=25°C ± 5°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 6.5 V/0.45 V
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	–0.1*5	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} +0.5*6	V	
Output voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

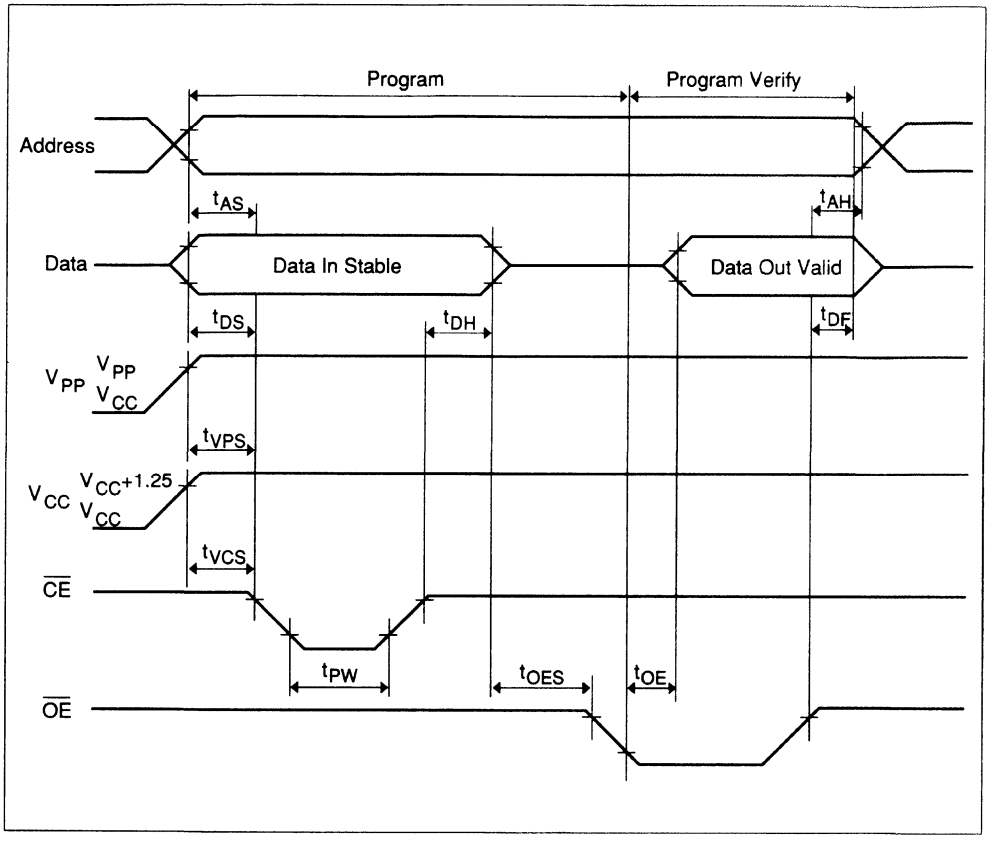
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤20 ns
- Reference levels for measuring timings: 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{CE}$ initial programming pulse width	t_{PW}	47.5	50.0	52.5	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	

Note: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform

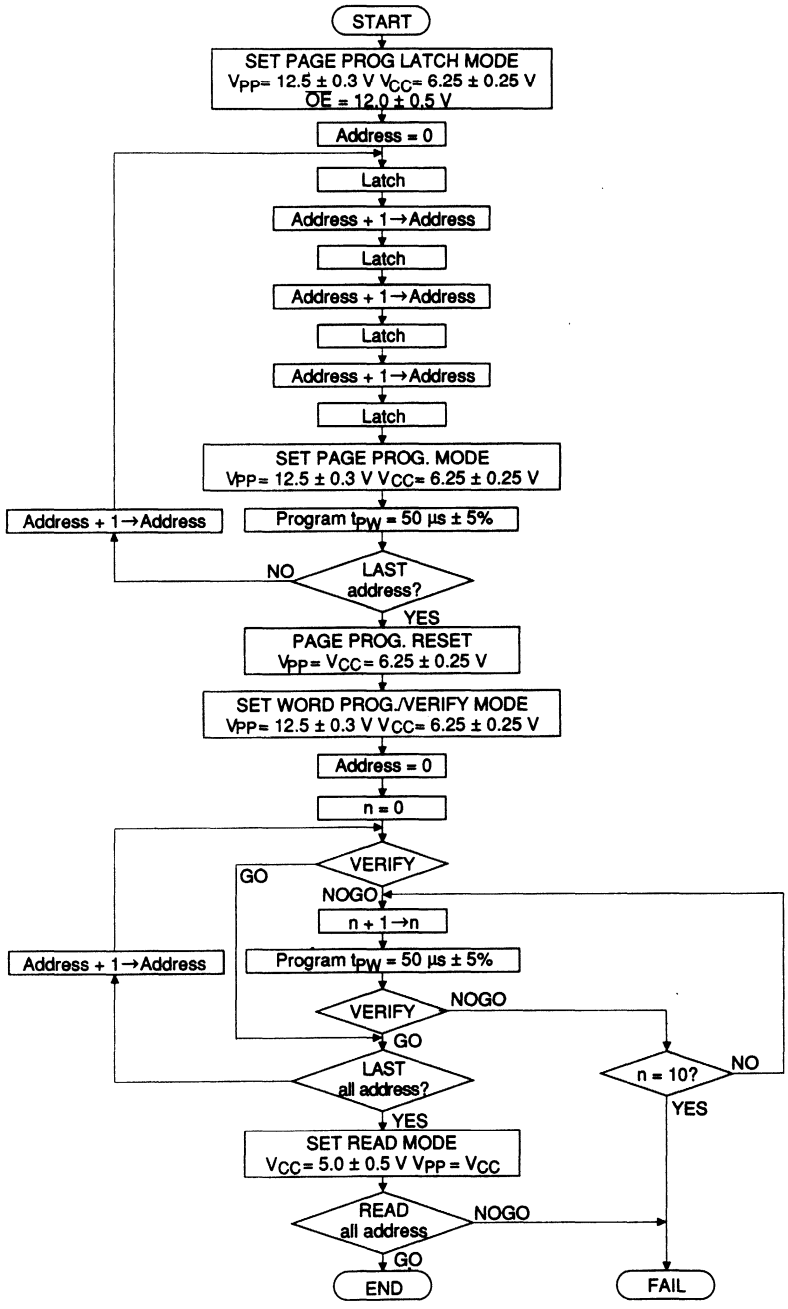


Optional Page Programming

This device can be applied the optional page programming algorithm shown in the following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

This programming algorithm is the combination of page programming and word verify. It can avoid the increase of programming verify time when a programmer with slow machine cycle is used, and shorten the total programming time.

Regarding the timing specifications for page programming and word verify, please refer to the specifications for fast high-reliability page programming and fast high-reliability programming.



Optional Page Programming Flowchart

DC Characteristics (V_{CC} = 6.25 V ± 0.25 V, V_{PP} =12.5 V ± 0.3 V, Ta=25°C ± 5°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 6.5 V/0.45 V
Output voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA
Operating V_{CC} current	I_{CC}	—	—	50	mA	
Input voltage	V_{IL}	–0.1*5	—	0.8	V	
	V_{IH}	2.2	—	V_{CC} +0.5*6	V	
	V_H	11.5	12.0	12.5	V	
V_{PP} supply current	I_{PP}	—	—	70	mA	$\overline{CE}$ = V_{IL}

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, Ta = 25°C ± 5°C)

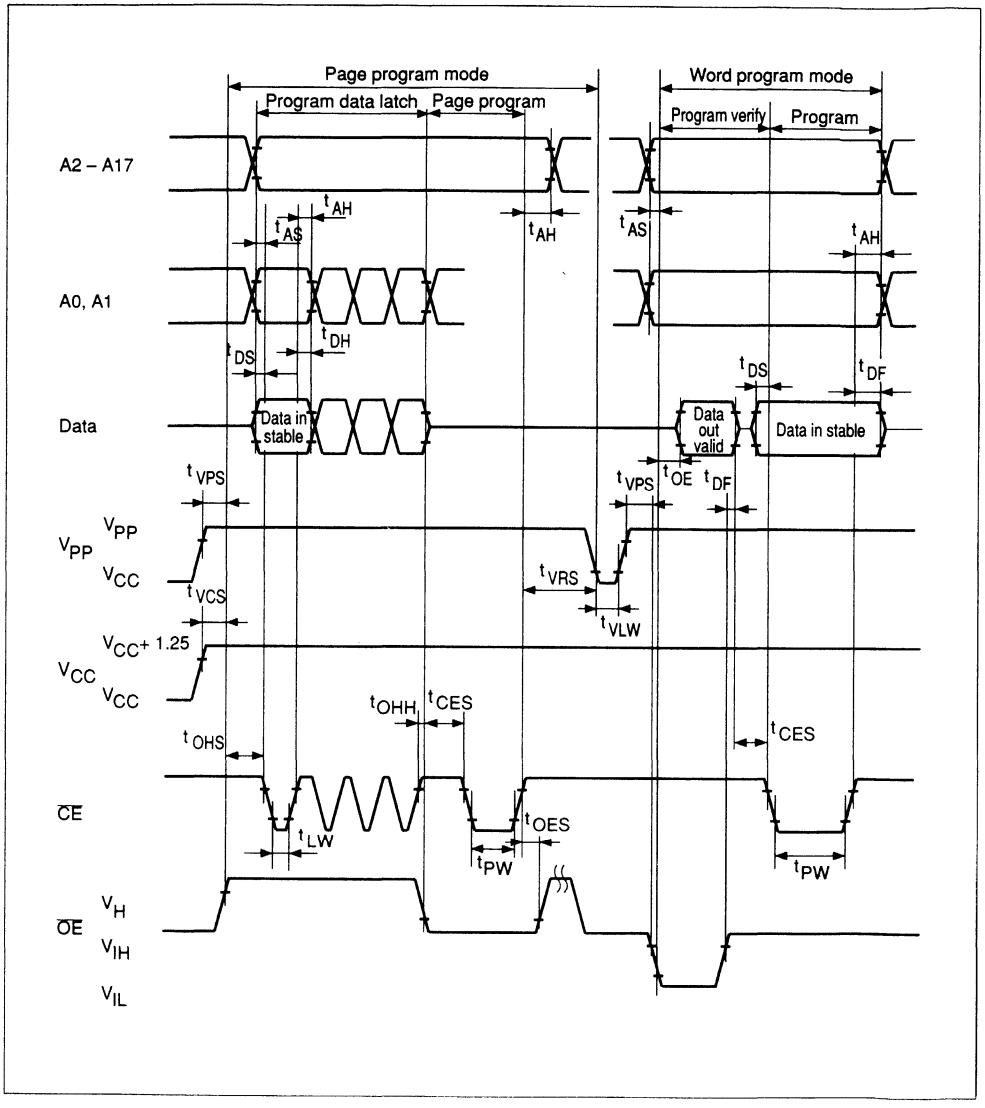
Test Conditions

- Input pulse levels: 0.45 to 2.4 V
- Input rise and fall times: ≤20 ns
- Reference levels for measuring timings:
  Inputs; 0.8 V, 2.0 V
  Outputs; 0.8 V, 2.0 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ high to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{CE}$ initial programming pulse width	t_{PW}	47.5	50.0	52.5	µs	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	
$\overline{CE}$ pulse width during data latch	t_{LW}	1	—	—	µs	
$\overline{OE}$ = V_H setup time	t_{OHS}	2	—	—	µs	
$\overline{OE}$ = V_H hold time	t_{OHH}	2	—	—	µs	
Page programming reset time *2	t_{VLW}	1	—	—	µs	
V_{PP} hold time *2	t_{VRS}	1	—	—	µs	

Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Page program mode will be reset when V_{PP} is set to V_{CC} or less.

Option Page Programming Timing Waveform



Erase

Erasure of HN27C4096G/CC is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity × exposure time) for erasure is 15 W•sec/cm^2.

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C4096 Identifier Code

		A0	I/O8 – I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	
	CC – 44	(24)	(11) – (4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	
Identifier	DG – 40A	(21)	(10) – (3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	Hex Data
Manufacturer code		V_{IL}	×	0	0	0	0	0	1	1	1	07
Device code		V_{IH}	×	1	0	1	0	0	0	1	0	A2

Notes: 1. V_{CC} = 5.0 V ± 10%
2. A9 = 12.0 V ± 0.5 V
3. A1 – A8, A10 – A17, $\overline{CE}$, $\overline{OE}$=V_{IL}
4. ×: Don't care.

HN27C4001G Series — Under Development

524288-Word × 8-Bit CMOS UV Erasable and Programmable ROM

The Hitachi HN27C4001G is a 4-Mbit ultraviolet erasable and electrically programmable ROM, featuring high speed and low power dissipation. Fabricated on advanced fine process and high speed circuitry technique, the HN27C4001G makes high speed access time possible. Therefore, it is suitable for high-speed microcomputer systems. The HN27C4001G offers high speed programming using short pulse programming.

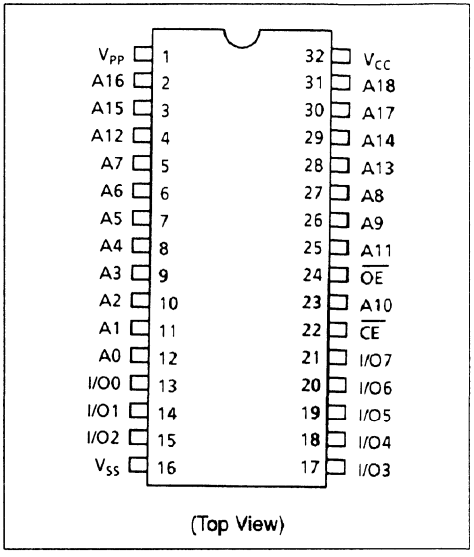
Features

- High speed: Access time 100 ns/120 ns/150 ns (max)
- Low power dissipation:
  - Standby mode: 5 µW (typ)
  - Active mode: 35 mW/MHz (typ)
- Fast high reliability programming
  - Program voltage: + 12.5 V DC
  - Program time: 11 sec (min) (Theoretical)
- Inputs and outputs TTL compatible during both read and program modes
- Pin arrangement: 32 pin JEDEC standard
- Device identifier mode: Manufacture code and device code

Ordering Information

Type No.	Access time	Package
HN27C4001G-10	100 ns	600-mil 32-pin cerdip (DG-32)
HN27C4001G-12	120 ns	
HN27C4001G-15	150 ns	

Pin Arrangement



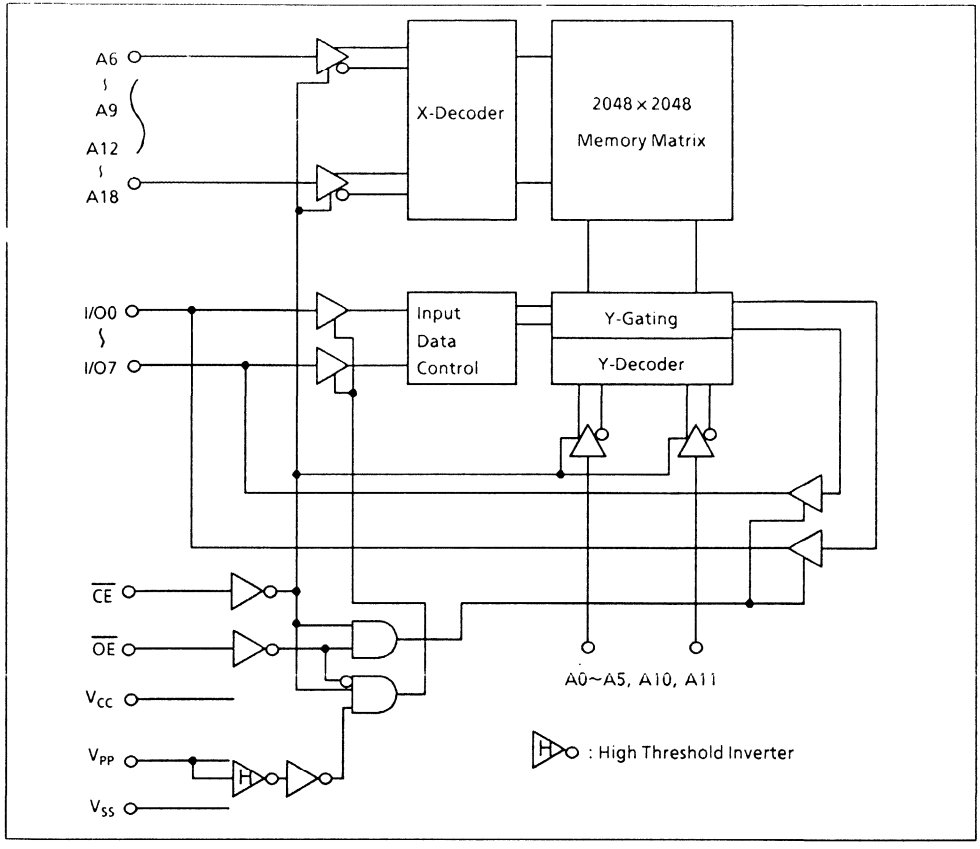
(Top View)

Pin Description

Pin Name	Function
A0 – A18	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Mode Selection

Mode	Pin	$\overline{CE}$ (22)	$\overline{OE}$ (24)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13 to 15, 17 to 21)
Read		V_{IL}	V_{IL}	×	V_{SS}–V_{CC}	V_{CC}	Dout
Output disable		V_{IL}	V_{IH}	×	V_{SS}–V_{CC}	V_{CC}	High-Z
Standby		V_{IH}	×	×	V_{SS}–V_{CC}	V_{CC}	High-Z
Prog	Program	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din
	Program verify	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Dout
	Optional verify	V_{IL}	V_{IL}	×	V_{PP}	V_{CC}	Dout
	Program inhibit	V_{IH}	V_{IH}	×	V_{PP}	V_{CC}	High-Z
Identifier		V_{IL}	V_{IL}	V_H*2	V_{SS}–V_{CC}	V_{CC}	Code

Notes: 1. ×: Don't care
2. V_H: 12.0 V ± 0.5 V

HN27C256AFP Series — Preliminary

32768-word x 8-bit CMOS OneTime Electrically Programmable ROM

The HN27C256AFP is a 32768-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C256AFP are in the "1" State (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28-pin plastic flat package (SOP). Therefore, this device cannot be re-written.

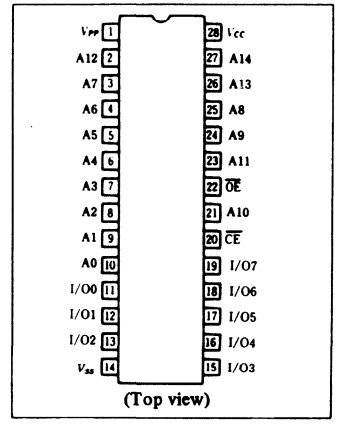
Features

- High speed
  - Access time . . . . . 120 / 150ns (max.)
- Low power dissipation
  - Active mode . . . . . 25 mW (typ.) (f = 1 MHz)
  - Standby mode . . . . . 5 μW (typ.)
- High reliability and fast programming
  - Programming voltage: +12.5V DC
  - Fast High-Reliability Programming Algorithm available
- Device identifier mode
  - Manufacturer code and device code

Ordering Information

Type No.	Access Time	Package
HN27C256AFP-12	120 ns	28-pin Plastic SOP (FP-28DA)
HN27C256AFP-15	150 ns	

Pin Arrangement



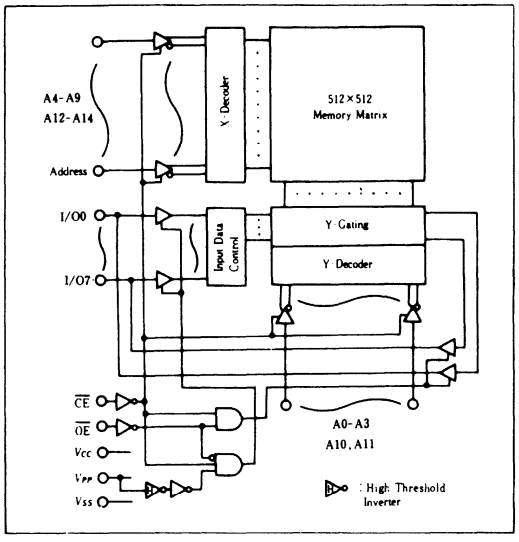
(Top view)

Pin Description

Pin Name	Function
A0 – A14	Address
I/O0–IO7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground

Note) The specifications of this device are subject to change without notice. Please contact Hitachi's Sales Dept. regarding specifications.

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	I/O (11 – 13, 15 – 19)
Read	V_{IL}	V_{IL}	x	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	x	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	x	V_{PP}	V_{CC}	Din
Program verify	V_{IH}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Optional verify	V_{IL}	V_{IL}	x	V_{PP}	V_{CC}	Dout
Program inhibit	V_{IH}	V_{IH}	x	V_{PP}	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	V_{CC}	Code

Notes: 1. x = Don't care.
2. V_H = 12.0V ± 0.5V.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output Voltages*1	Vin, Vout	−0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	−0.6*2 to +13.5	V
V_{PP} voltage*1	Vpp	−0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	−0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−65 to +125	°C
Storage temperature range under bias	Tbias	−10 to +80	°C

Notes: 1. Relative to V_{SS}.
2. Vin, Vout, V_{ID} min = −1.0V for pulse width ≦ 50ns.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	4	8	pF	Vin = 0V
Output capacitance	$Cout$	–	8	12	pF	Vout = 0V

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ±10%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
Output leakage current	I_{LO}	–	–	2	μA	$Vout$ = 0V to V_{CC}
V_{PP} current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
Standby V_{CC} current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = VIH
	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ± 0.3V
Operating V_{CC} current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, $Iout$ = 0 mA
	I_{CC2}	–	–	30	mA	f = 10 MHz, $Iout$ = 0 mA
	I_{CC3}	–	5	15	mA	f = 1 MHz, $Iout$ = 0 mA
Input low voltage*3	V_{IL}	−0.3*1	–	0.8	V	
Input high voltage*3	V_{IH}	2.2	–	V_{CC}+1.0*2	V	
Output low voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH1}	2.4	–	–	V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC}−0.7	–	–	V	I_{OH} = −100 μA

Notes: *1. V_{IL} min = −1.0V for pulse width ≦ 50ns.
*2. V_{IH} max = V_{CC} + 1.5V for pulse width ≦ 20ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.
*3. Only defined for DC function test. V_{IL} max = 0.45V, V_{IH} min = 2.4V for AC function test.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 5V ±10%, V_{PP} = V_{CC})

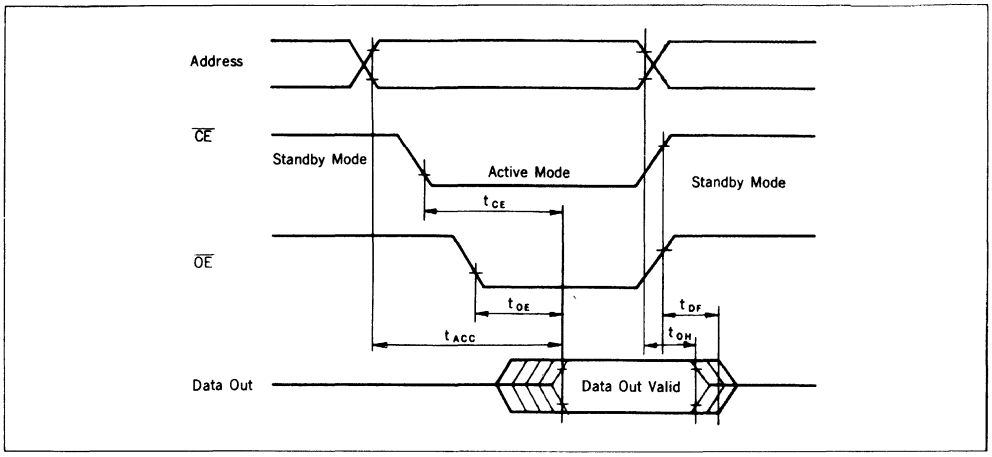
Test condition

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 10ns
- Output load: 1 TTL Gate + 100pF
- Reference Ivels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	HN27C256AFP-12		HN27C256AFP-15		Unit	Test Conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	120	–	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	120	–	150	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	–	60	–	70	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	40	0	50	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	5	–	5	–	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

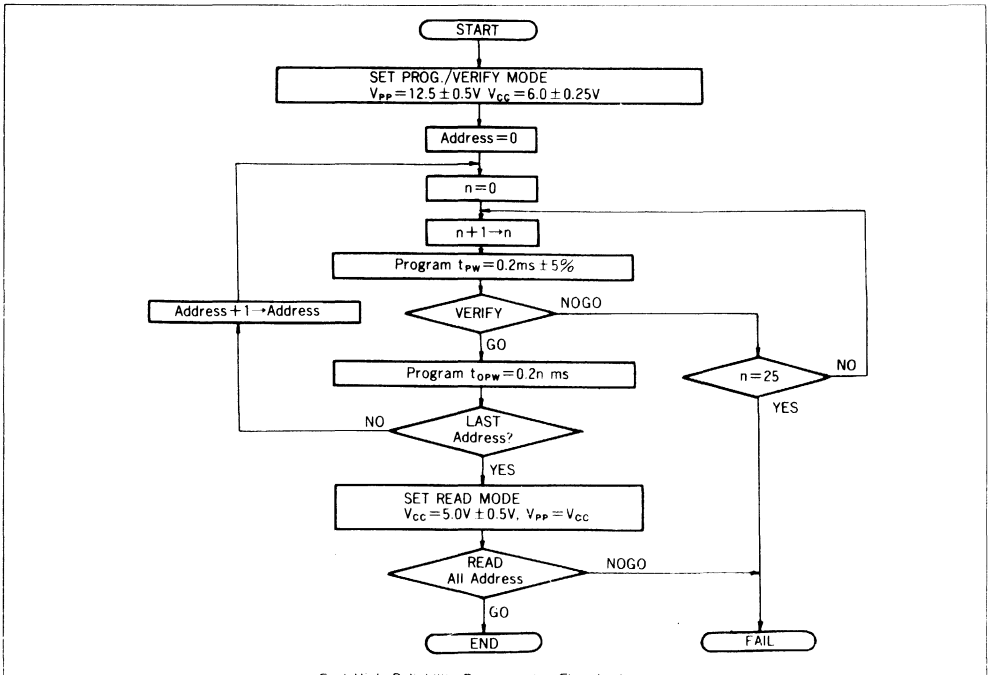
Read Timing Waveform



Programming Operation

Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming Algorithm shown in following flowchart. This algorithm offers both faster programming time and high reliability data retension. A theoretical programming time (except brank checking and verifying time) is one-tenth of conventional high performance programming algorithm's. Regarding the model and software version of the programmers available this algorithm, please contact programmer maker.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	−0.1 *5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5 *6	V	
Output low voltage during verity	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = −400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = −0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

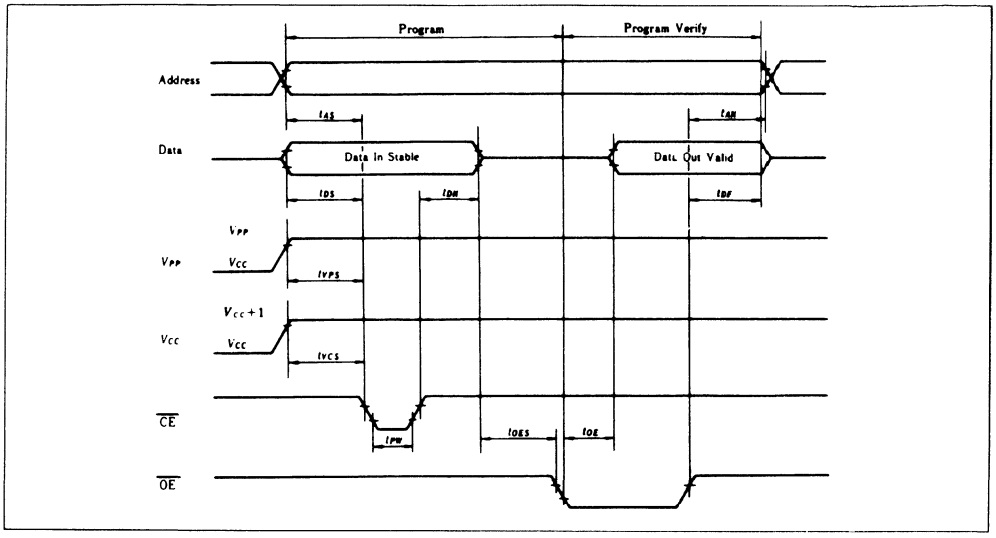
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	μs
$\overline{OE}$ setup time	t_{OES}	2	–	–	μs
Data setup time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
V_{PP} setup time	t_{VPS}	2	–	–	μs
V_{CC} setup time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.19	0.20	0.21	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW} *1	0.19	–	5.25	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF} *2	–	–	130	ns

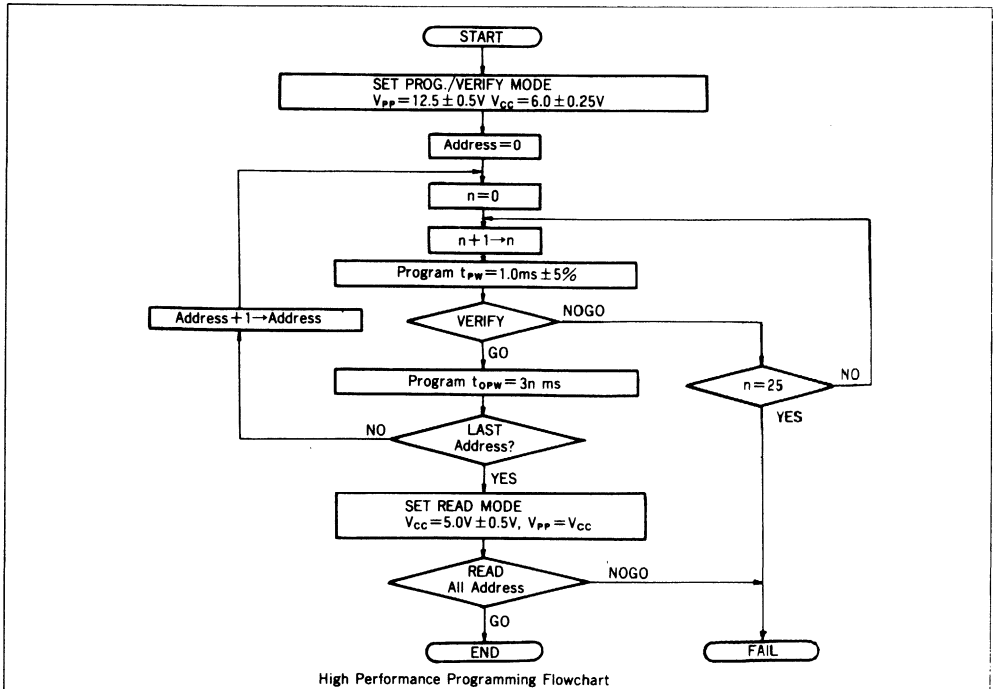
Notes: 1. Refer to the Fast High-Reliability Programming Fowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Fast High-Reliability Programming Timing Waveform



High Performance Programming

This device can be applied the high performance programming algorithm shown in following flowchart. This algorithm is as same as our 256-kbit EPROM series so existing programmers can be used with this device. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	–	–	2	μA	Vin = 0V to V_{CC}
V_{PP} supply current	I_{PP}	–	–	30	mA	$\overline{CE}$ = V_{IL}
Operating V_{CC} current	I_{CC}	–	–	30	mA	
Input low level	V_{IL}	−0.1 *5	–	0.8	V	
Input high level	V_{IH}	2.2	–	V_{CC}+0.5 *6	V	
Output low voltage during verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	–	–	V	I_{OH} = −400 μA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5V.
4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = −0.6V for pulse width ≦ 20ns.
6. If V_{IH} is over the specified maximum value, programming operation. cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

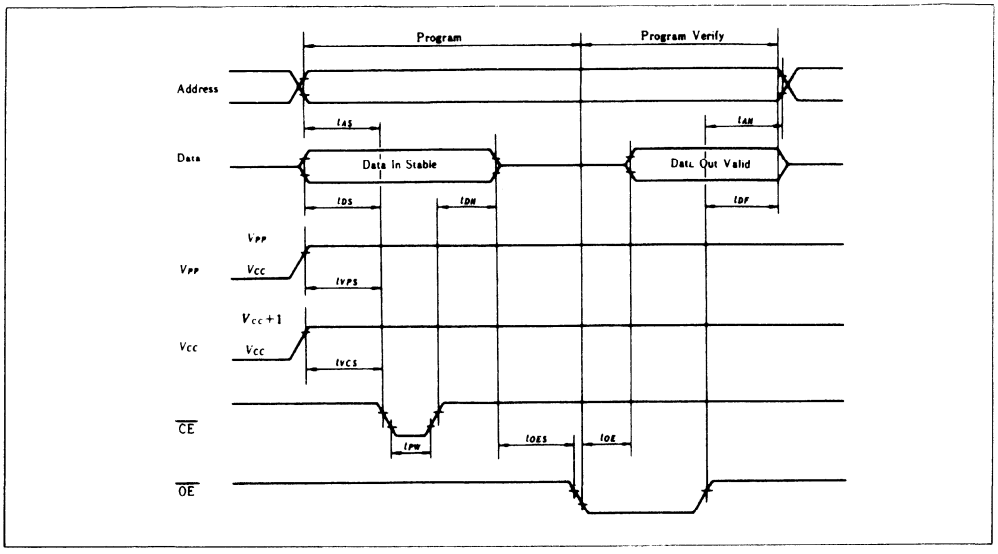
Test Conditions

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall times: ≦ 20ns
- Reference levels for measuring timing: Inputs; 0.8V and 2.0V
  Outputs; 0.8V and 2.0V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	–	–	μs
$\overline{OE}$ setup time	t_{OES}	2	–	–	μs
Data setup time	t_{DS}	2	–	–	μs
Address hold time	t_{AH}	0	–	–	μs
Data hold time	t_{DH}	2	–	–	μs
V_{PP} setup time	t_{VPS}	2	–	–	μs
V_{CC} setup time	t_{VCS}	2	–	–	μs
$\overline{CE}$ initial programming pulth width	t_{PW}	0.95	1.0	1.05	ms
$\overline{CE}$ overprogramming pulse width	t_{OPW} *1	2.85	–	78.75	ms
Data valid from $\overline{OE}$	t_{OE}	0	–	150	ns
$\overline{OE}$ to output float delay	t_{DF} *2	–	–	130	ns

Notes: 1. Refer to the high performance programming flowchart for t_{OPW}.
2. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

High Performance Programming Timing Waveform



Mode Description

Device Identifier Mode

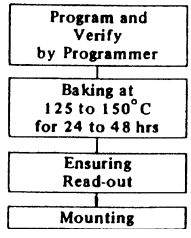
Programming condition of OTPROM is various according to OTPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some OTPROMs provide maker identifier code. Users can write OTPROM by reading out write condition coded before shipped. Some commercial programmers can set write condition by recognizing this code. This function enables effective program. Regarding commercial programmers that can recognize this device's identifier code, please contact programmer maker.

Identifier	A0 (10)	I/O7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer code	V_{IL}	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	0	0	1	1	0	0	0	1	31

Notes: 1. A9 = 12.0V ± 0.5V.
2. A1 – A8, A10 – A14, $\overline{CE}$, $\overline{OE}$ = V_{IL}.

Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.

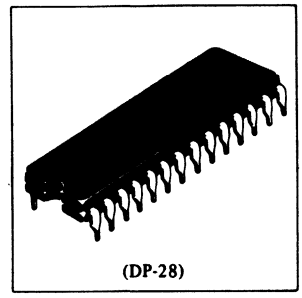


Recommended Screening conditions

HN27512P Series

65536-word x 8-bit One Time Electrically Programmable Read Only Memory

The HN27512P is a 65536-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27512P are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic dual in-line package. Therefore, this device can not be re-written.



(DP-28)

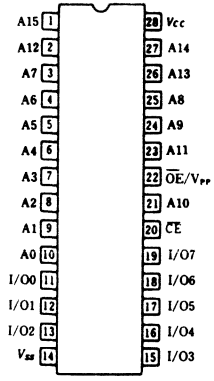
■ FEATURES

- Single Power Supply . . . . . +5V ±5%
- High Performance Programming . . . . . Program Voltage: +12.5V D.C. High Performance Programming Operations
- Static . . . . . No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time . . . . . 250/300ns (max.)
- Absolute Max. Rating of Vpp pin . . . . . 14.0V (max.)
- Device Identifier Mode . . . . . Manufacturer Code and Device Code.

Ordering Information

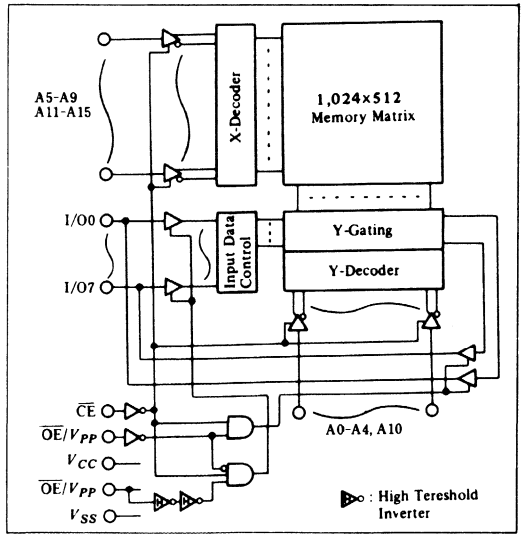
Part No.	Access	Package
HN27512P-25	250ns	600 mil 28-pin Plastic DIP
HN27512P-30	300ns	

Pin Arrangement



(Top View)

Block Diagram



Pin Description

Pin Name	Function
A0 – A15	Address
I/O0 – I/O7	Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{PP}	Programming Power Supply
V_{SS}	Ground

■ MODE SELECTION

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	A9 (24)	V_{CC} (28)	I/O (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H*2	V_{CC}	Code

Notes) *1. X . . . Don't care
*2. V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +80	°C
All Input and Output Voltages*1	V_{IN}, V_{out}	−0.6 to +7	V
Voltage on Pin 24 (A9)*1	V_{ID}	−0.6 to +13.5	V
V_{PP} Voltage*1	V_{PP}	−0.6 to +14.0	V
V_{CC} Voltage*1	V_{CC}	−0.6 to +7	V

Note) *1. With respect to V_{SS}

■ READ OPERATION

• DC AND OPERATING CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	−	−	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.25/0.45V	−	−	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}	−	−	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	−	45	100	mA
Input Low voltage	V_{IL}		−0.1*1	−	0.8	V
Input High Voltage	V_{IH}		2.0	−	V_{CC}+1*2	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	−	0.45	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	−	−	V

Notes) *1. −0.6V for pulse width ≦ 20ns
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

• AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±5%)

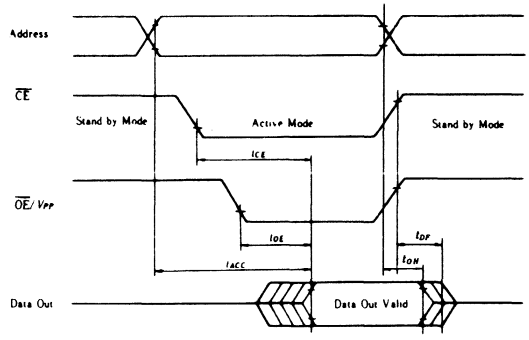
Parameter	Symbol	Test Condition	HN27512P-25		HN27512P-30		Unit
			min.	max.	min.	max.	
Addres to Output Delay	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	$\overline{OE}$ = V_{IL}	–	250	–	300	ns
$\overline{OE}$ to Output Delay	t_{OE}	$\overline{CE}$ = V_{IL}	–	100	–	120	ns
$\overline{OE}$ High Output Float	t_{DF}	$\overline{CE}$ = V_{IL}	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	0	–	ns

Note: t_{DF} is defined as the time at which the Output achieves the open circuit condition and Data is no longer driven.

• SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Output Load:	1 TTL Gate +100pF
Reference Level for Measuring Timing:	0.8V and 2.0V

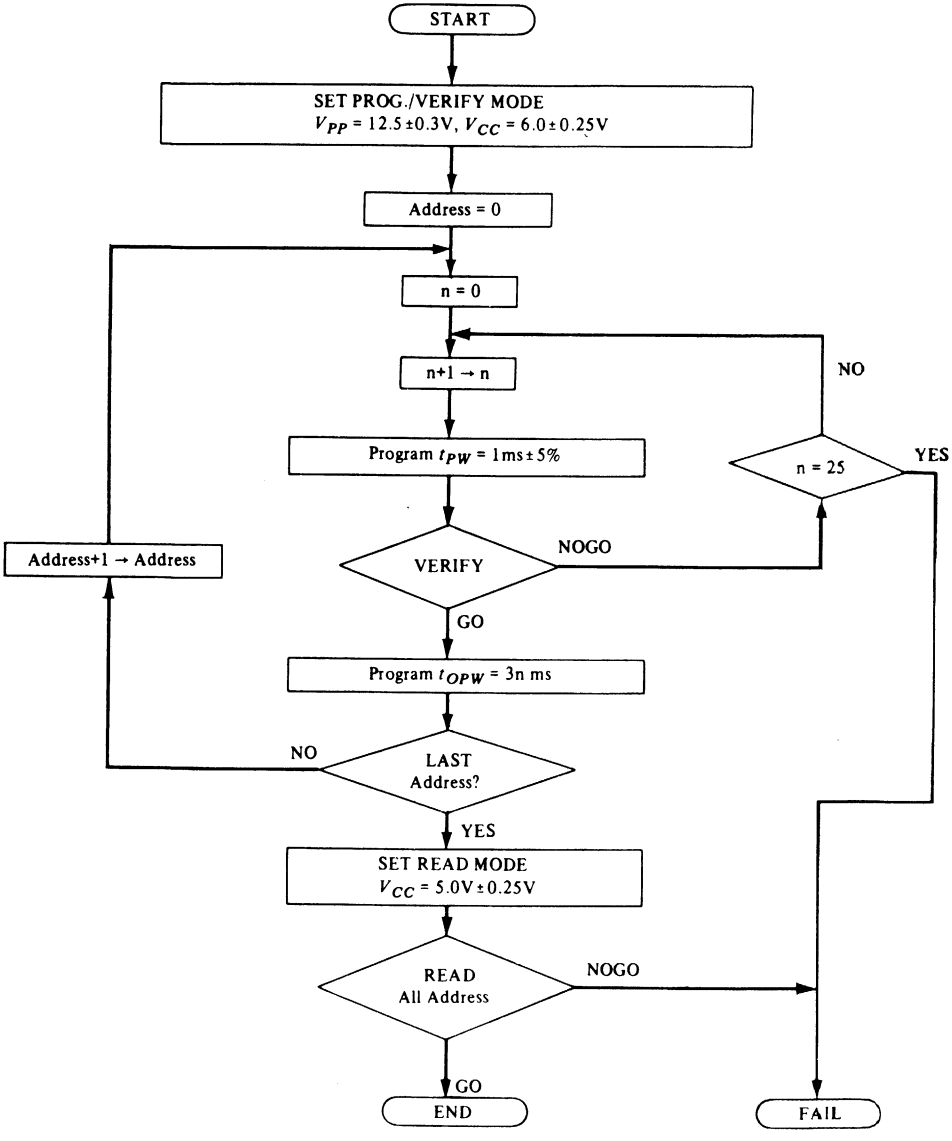


• CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter		Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	except $\overline{OE}/V_{PP}$	C_{in1}	V_{in} = 0V	–	4	6	pF
	$\overline{OE}/V_{PP}$ Pin	C_{in2}	V_{in} = 0V	–	12	20	pF
Output Capacitance		C_{out}	V_{out} = 0V	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

• DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V_{OL}	I_{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	I_{OH} = -400μA	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	100	mA
Input Low Level	V_{IL}		-0.1*1	–	0.8	V
Input High Level	V_{IH}		2.0	–	V_{CC}+0.5*2	V
V_{PP} Supply Current	I_{PP}	$\overline{CE}$ = V_{IL}	–	–	50	mA

Notes) *1. -0.6V for pulse width ≦ 20ns
*2. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

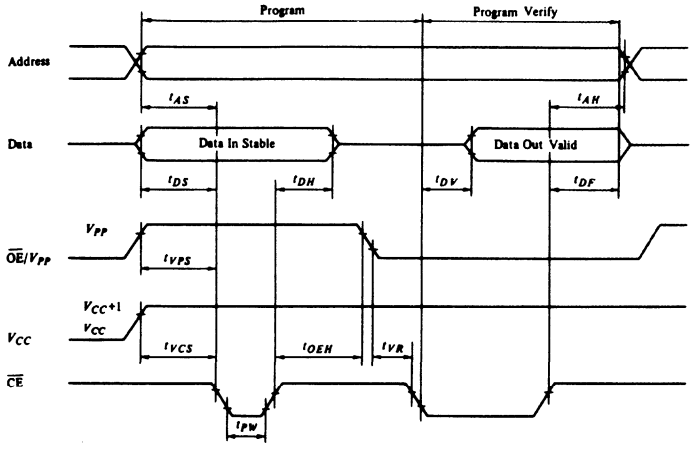
• AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ±5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{OE}$ Hold Time	t_{OEH}		2	–	–	μs
$\overline{CE}$ to Output Float Delay	t_{DF}*1		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{CE}$ Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{CE}$ Pulse Width During Overprogramming	t_{OPW}*2		2.85	–	78.75	ms
V_{PP} Recovery Time	t_{VR}		2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}		–	–	1	μs

Notes: *1. t_{DF} is de fined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

• SWITCHING CHARACTERISTICS

Test Condition
Input Pulse Level: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Level for Measuring Timing: 0.8V and 2.0V



■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of OTPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

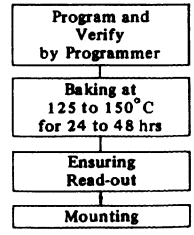
• HN27512P SERIES IDENTIFIER CODE

Pins / Identifier	A_0 (10)	O_7 (19)	I/O6 (18)	I/O5 (17)	I/O4 (16)	I/O3 (15)	I/O2 (13)	I/O1 (12)	I/O0 (11)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IL}	1	0	0	1	0	1	0	0	94

Notes: 1. $A_9 = 12.0V \pm 0.5V$.
2. $A_1 - A_8$, $A_{10} - A_{15}$, $\overline{CE}$, $\overline{OE}/V_{PP} = V_{IL}$.

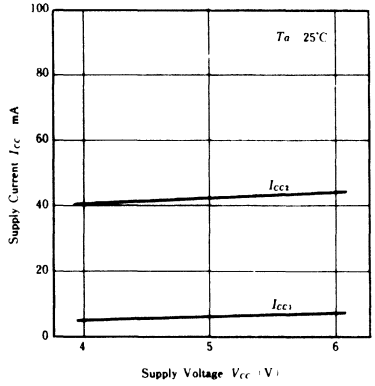
■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.

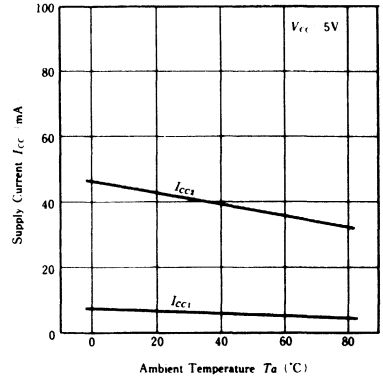


Recommended Screening conditions

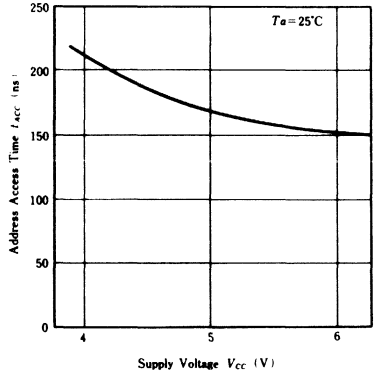
SUPPLY CURRENT vs. SUPPLY VOLTAGE



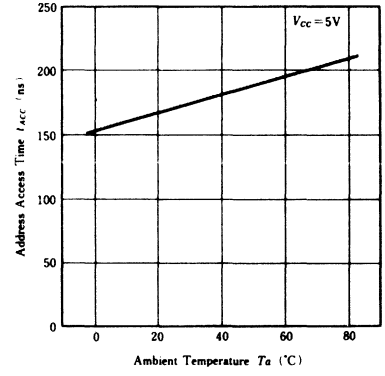
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



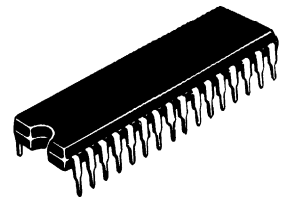
HN27C101P Series
HN27C101FP Series

131072-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C101P Series are 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C101P/FP series are in the "1" state (output high).

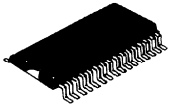
Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in 32 pin plastic package, therefore, this device cannot be rewritten and erased.

HN27C101 Series



(DP-32)

HN27C101FP Series



(FP-32D)

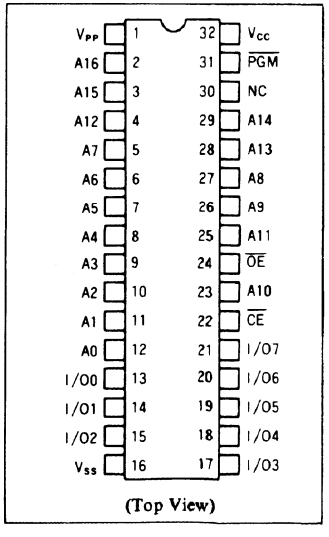
Features

- High speed
  - Access time . . . . . 200/250 ns (max.)
- Low power dissipation
  - Active mode 50 mW/MHz (typ.)
  - Standby mode 5 μW (typ.)
- Single power supply . . . . . +5 V ± 5%
- Fast High-Reliability program mode and Fast High-Reliability page program mode
  - Program voltage: +12.5V DC
  - Fast High-Reliability programming available
- Static . . . . . No clocks required
- Inputs and outputs TTL compatible during both read and program modes

Ordering Information

Type No.	Access time	Package
HN27C101P-20	200ns	600 mil 32 pin
HN27C101P-25	250ns	Plastic DIP
HN27C101FP-20	200ns	32 pin
HN27C101FP-25	250ns	Plastic SOP

Pin Arrangement

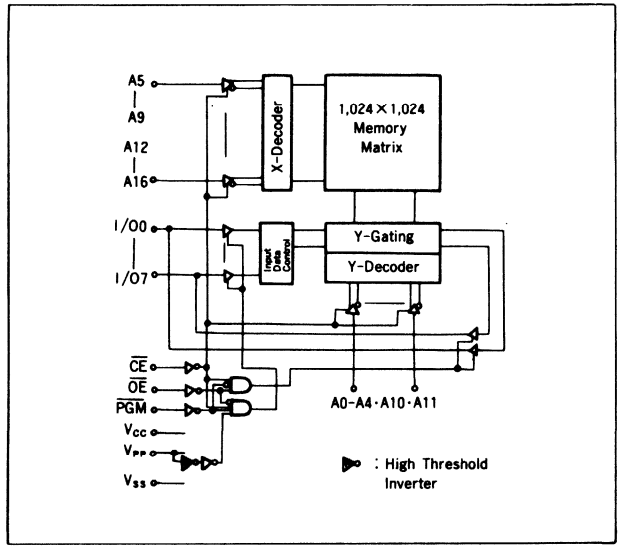


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



■ Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) 1. X: Don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
All input and output voltages*1	V_{in}, V_{out}	−0.6*2 to +7.0	V
V_{PP} voltage*1	V_{PP}	−0.6 to +13.0	V
V_{CC} voltage*1	V_{CC}	−0.6 to +7.0	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	−55 to +125	°C
Storage temperature range under bias	T_{bias}	−10 to +80	°C

Notes) *1. With respect to V_{SS}
*2. −1.0 V for pulse width ≦ 50 ns

Read Operation

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 5.25V
Output Leakage Current	I_{LO}	–	–	2	μA	V_{out} = 5.25V/0.45V
V_{PP} Current	I_{PP1}	–	1	20	μA	V_{PP} = 5.5V
V_{CC} Current	I_{SB1}	–	–	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	–	1	20	μA	$\overline{CE}$ = V_{CC} ±0.3V
V_{CC} Current	I_{CC1}	–	–	30	mA	$\overline{CE}$ = V_{IL}, I_{out} = 0mA
	I_{CC2}	–	–	30	mA	f = 5 MHz, I_{out} = 0mA
	I_{CC3}	–	–	15	mA	f = 1 MHz, I_{out} = 0mA
Input Low Voltage	V_{IL}	–0.3*1	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	V_{CC}+1*2	V	
Output Low Voltage	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –400μA

Notes) *1. –1.0V for pulse width ≦ 50ns.
*2. V_{CC} + 1.5V for pulse width ≦ 20ns. If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC})

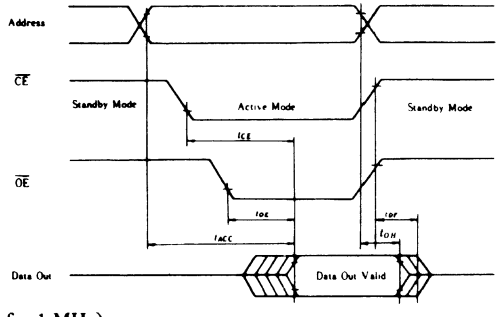
Item	Symbol	HN27C101P/FP-20		HN27C101P/FP-25		Unit	Test conditions
		Min	Max	Min	Max		
Address to output delay	t_{ACC}	–	200	–	250	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}
$\overline{CE}$ to output delay	t_{CE}	–	200	–	250	ns	$\overline{OE}$=V_{IL}
$\overline{OE}$ to output delay	t_{OE}	–	70	–	100	ns	$\overline{CE}$=V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	60	ns	$\overline{CE}$=V_{IL}
Address to output hold	t_{OH}	0	–	0	–	ns	$\overline{CE}$=$\overline{OE}$=V_{IL}

Note) t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Switching Characteristics

Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≦ 20ns
Output Load: 1 TTL Gate + 100pF
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V

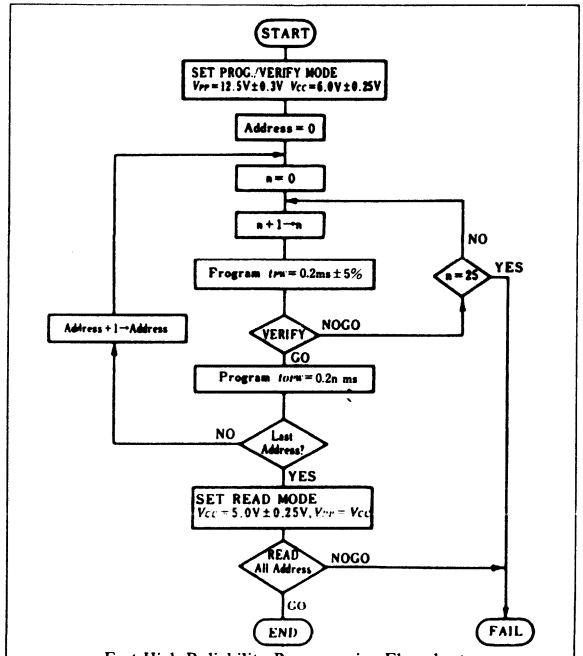


Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{in}	–	–	10	pF	V_{in} = 0V
Output Capacitance	C_{out}	–	–	15	pF	V_{out} = 0V

Fast High-Reliability Programming

This device can be applied the Fast High-Reliability Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Programming Characteristics ($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5\ V \pm 0.3V$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	μA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400μA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	40	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$ = Low.
*5. –0.6V for pulse width ≦ 20ns.
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

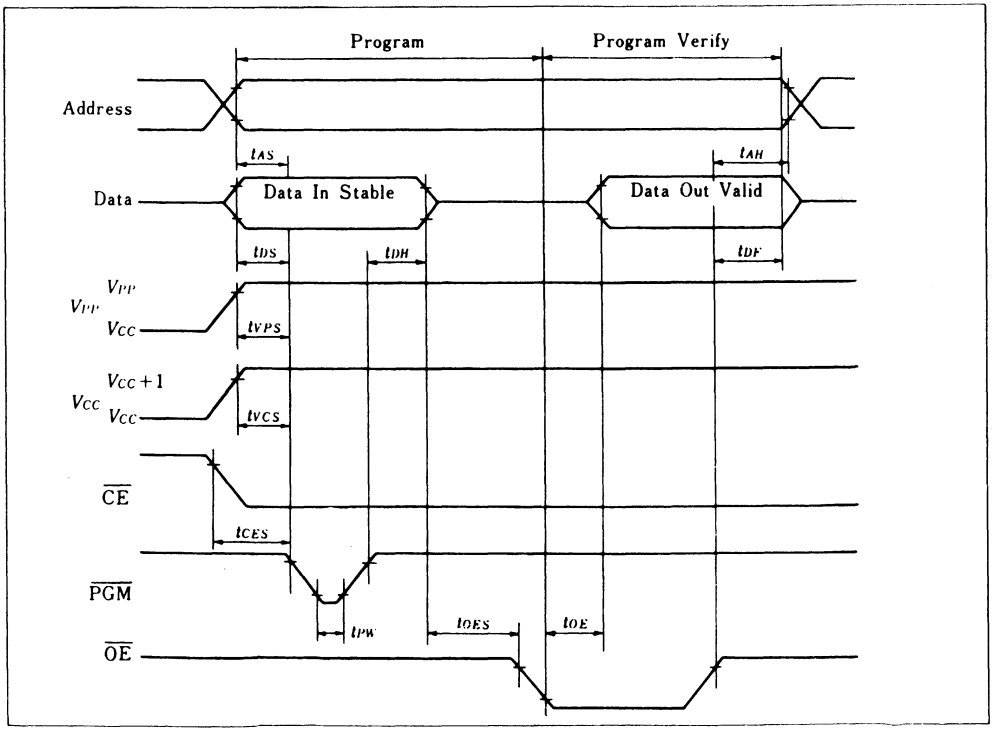
($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from OE	t_{OE}	0	–	150	ns	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Switching Characteristics

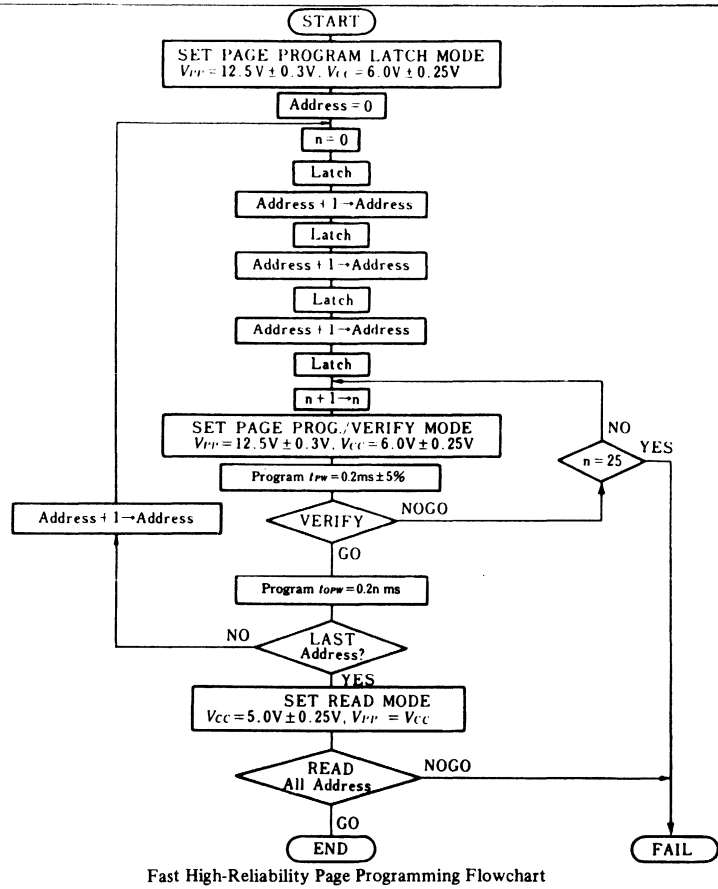
Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤ 20ns
Reference Levels for Measurement Timing:	Inputs; 0.8V and 2.0V Outputs; 0.8V and 2.0V



Fast High-Reliability Page Programming

This device can be applied the Fast High-Reliability Page Programming algorithm shown in following flowchart.

This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Programming Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	–	–	2	µA	V_{in} = 6.25V/0.45V
Output Low Voltage during Verify	V_{OL}	–	–	0.45	V	I_{OL} = 2.1mA
Output High Voltage during Verify	V_{OH}	2.4	–	–	V	I_{OH} = –400µA
V_{CC} Current (Active)	I_{CC}	–	–	30	mA	
Input Low Level	V_{IL}	–0.1*5	–	0.8	V	
Input High Level	V_{IH}	2.2	–	V_{CC}+0.5*6	V	
V_{PP} Supply Current	I_{PP}	–	–	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}

Notes) *1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
*2. V_{PP} must not exceed 13V including overshoot.
*3. An influence may be had upon device reliability if the device is installed or removed while V_{PP}=12.5V.
*4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{CE}$=Low.
*5. –0.6V for pulse width ≦ 20ns
*6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Programming Characteristics

($Ta = 25°C \pm 5°C$, $V_{CC} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$)

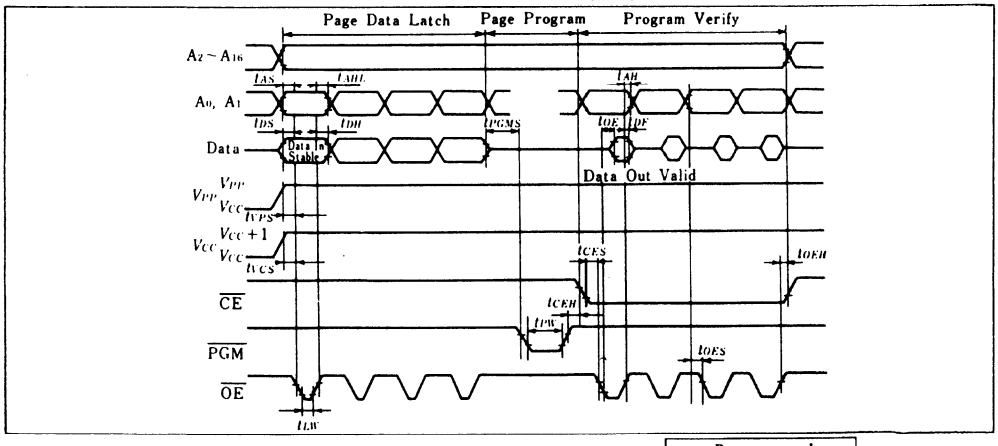
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2	–	–	μs	
$\overline{OE}$ Setup Time	t_{OES}	2	–	–	μs	
Data Setup Time	t_{DS}	2	–	–	μs	
Address Hold Time	t_{AH}	0	–	–	μs	
	t_{AHL}	2	–	–	μs	
Data Hold Time	t_{DH}	2	–	–	μs	
$\overline{OE}$ to Output Float Delay	t_{DF}*1	0	–	130	ns	
V_{PP} Setup Time	t_{VPS}	2	–	–	μs	
V_{CC} Setup Time	t_{VCS}	2	–	–	μs	
$\overline{PGM}$ Pulse Width during Initial Programming	t_{PW}	0.19	0.20	0.21	ms	
$\overline{PGM}$ Pulse Width during Over Programming	t_{OPW}*2	0.19	–	5.25	ms	
$\overline{CE}$ Setup Time	t_{CES}	2	–	–	μs	
Data Valid from $\overline{OE}$	t_{OE}	0	–	150	ns	
$\overline{OE}$ Pulse Width during Data Latch	t_{LW}	1	–	–	μs	
$\overline{PGM}$ Setup Time	t_{PGMS}	2	–	–	μs	
$\overline{CE}$ Hold Time	t_{CEH}	2	–	–	μs	
$\overline{OE}$ Hold Time	t_{OEH}	2	–	–	μs	

Notes) *1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
*2. Refer to the programming flowchart for t_{OPW}.

Switching Characteristics

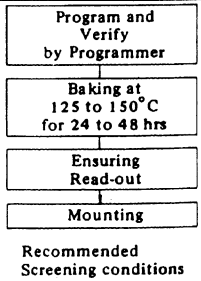
Test Condition

Input Pulse Levels: 0.45V to 2.4V
Input Rise and Fall Time: ≤ 20ns
Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
Outputs; 0.8V and 2.0V



Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

HN27C101AP Series
HN27C101AFP Series

131072-Word × 8-Bit CMOS One Time Electrically Programmable ROM

The HN27C101AP/AFP series are 131072-word × 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C101AP/AFP series are in the "1" state (output high).
Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32-pin plastic package, therefore, this device cannot be rewritten and erased.

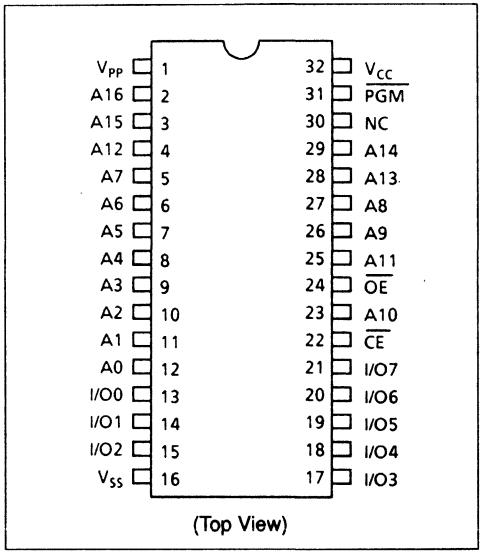
Features

- Single power supply: +5 V ± 10%
- Fast high-reliability programming mode and fast high-reliability page programming mode
  - Programming voltage: +12.5 V DC
  - Fast high-reliability page programming: 14 sec typ
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 50 mW/MHz typ (active)
  5 μW typ (standby)
- Pin arrangement: 32-pin JEDEC standard
- Device identifier mode: manufacturer code and device code
- Fully compatible with HN27C101P/FP series

Ordering Information

Type No.	Access time	Package
HN27C101AP-12	120 ns	600-mil 32-pin plastic DIP (DP-32)
HN27C101AP-15	150 ns	
HN27C101AP-20	200 ns	
HN27C101AP-25	250 ns	
HN27C101AFP-12	120 ns	32-pin plastic SOP (FP-32D)
HN27C101AFP-15	150 ns	
HN27C101AFP-20	200 ns	
HN27C101AFP-25	250 ns	

Pin Arrangement

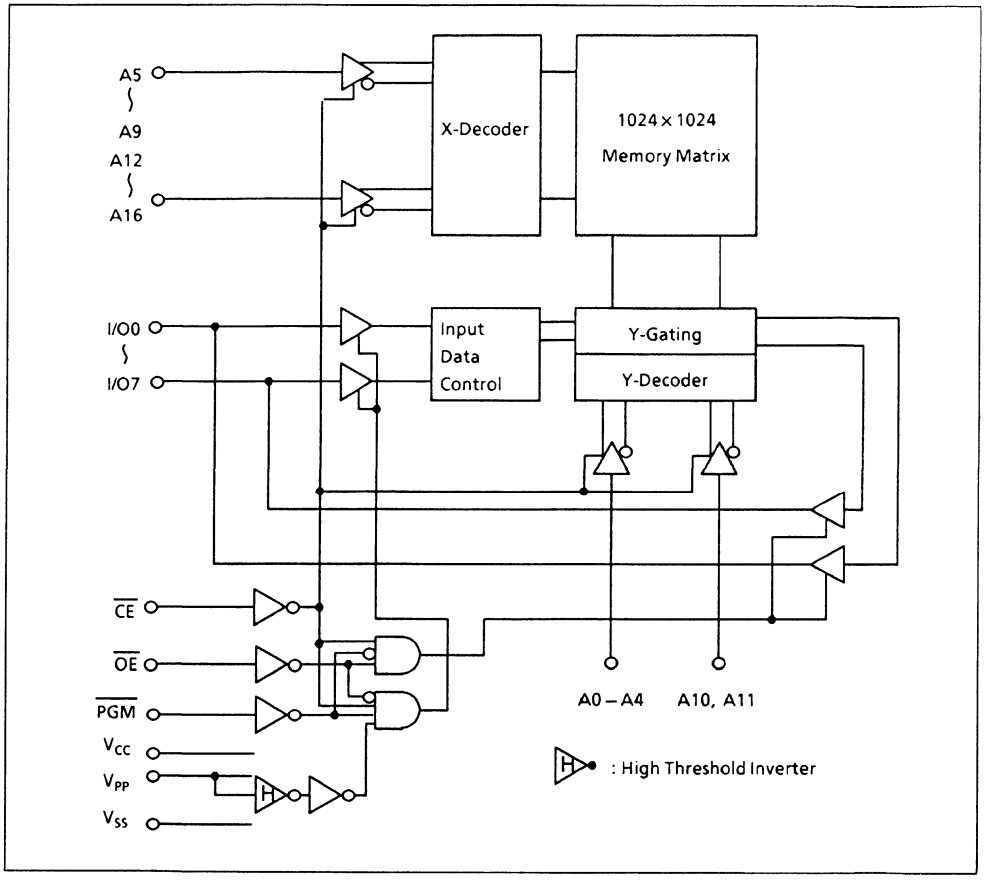


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	CE (22)	OE (24)	PGM (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	×	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	V_{IH}	×	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	×	×	×	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Din
Program verify	V_{IL}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Dout
Page data latch	V_{IH}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din

Mode Selection (cont)

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Page program	V_{IH}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
Program inhibit	V_{IL}	V_{IL}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
	V_{IL}	V_{IH}	V_{IH}				
	V_{IH}	V_{IL}	V_{IL}				
	V_{IH}	V_{IH}	V_{IH}				
Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code

Notes: 1. × = Don't care
2. V_H = 12.0 V ± 0.5 V

Absolute Maximum Ratings

Item	Symbol	Value	Unit
A11 input and output voltages*1	Vin, Vout	–0.6*2 to +7.0	V
A9 input voltage*1	V_{ID}	–0.6*2 to +13.5	V
V_{PP} voltage*1	V_{PP}	–0.6 to +13.5	V
V_{CC} voltage*1	V_{CC}	–0.6 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–10 to +80	°C

Notes: 1. Relative to V_{SS}
2. Vin, Vout and V_{ID} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	10	pF	Vin = 0 V
Output capacitance	Cout	—	—	15	pF	Vout = 0 V

Read Operation

DC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = 0 V to V_{CC}
V_{PP} current	I_{PP1}	—	1	20	µA	V_{PP} = 5.5 V
Standby V_{CC} current	I_{SB1}	—	—	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	1	20	mA	$\overline{CE}$ = V_{CC} ± 0.3 V
Operating V_{CC} current	I_{CC1}	—	—	30	mA	$\overline{CE}$ = V_{IL}, Iout = 0 mA
	I_{CC2}	—	—	30	mA	f = 5 MHz, Iout = 0 mA
		—	—	45	mA	f = 8.4 MHz, Iout = 0 mA
Input low voltage	V_{IL}	–0.3*1	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} +1.0*2	V	
Output low voltage	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
		V_{CC} –0.7	—	—	V	I_{OH} = –0.1 mA

Notes: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max = V_{CC} +1.5 V for pulse width ≤ 20 ns.
If V_{IH} is over the specified maximum value, read operation cannot be guaranteed.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, Ta = 0 to +70°C)

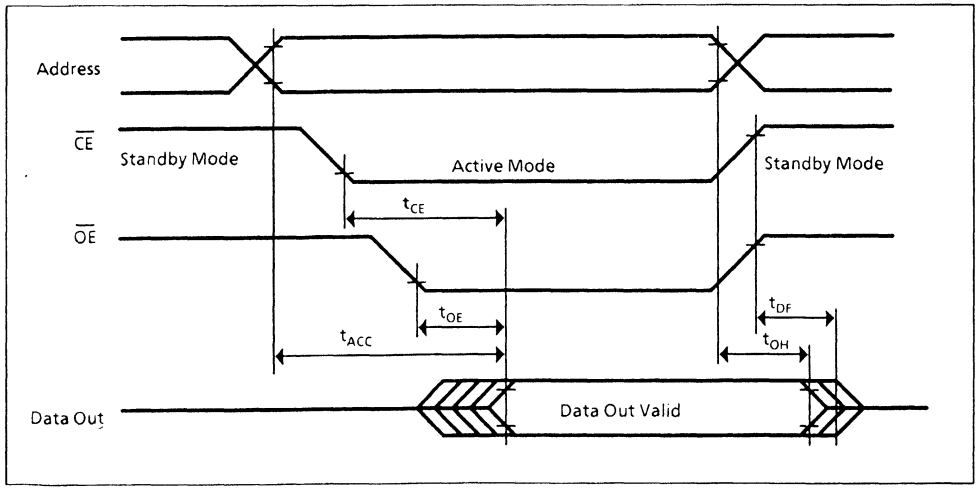
Test condition

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate +100 pF
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

		HN27C101AP/AFP									
		-12		-15		-20		-25			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	120	—	150	—	200	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}	—	120	—	150	—	200	—	250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	—	60	—	70	—	70	—	100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to output float	t_{DF}	0	50	0	60	0	50	0	60	ns	$\overline{CE}$ = V_{IL}
Address to output hold	t_{OH}	0	—	0	—	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

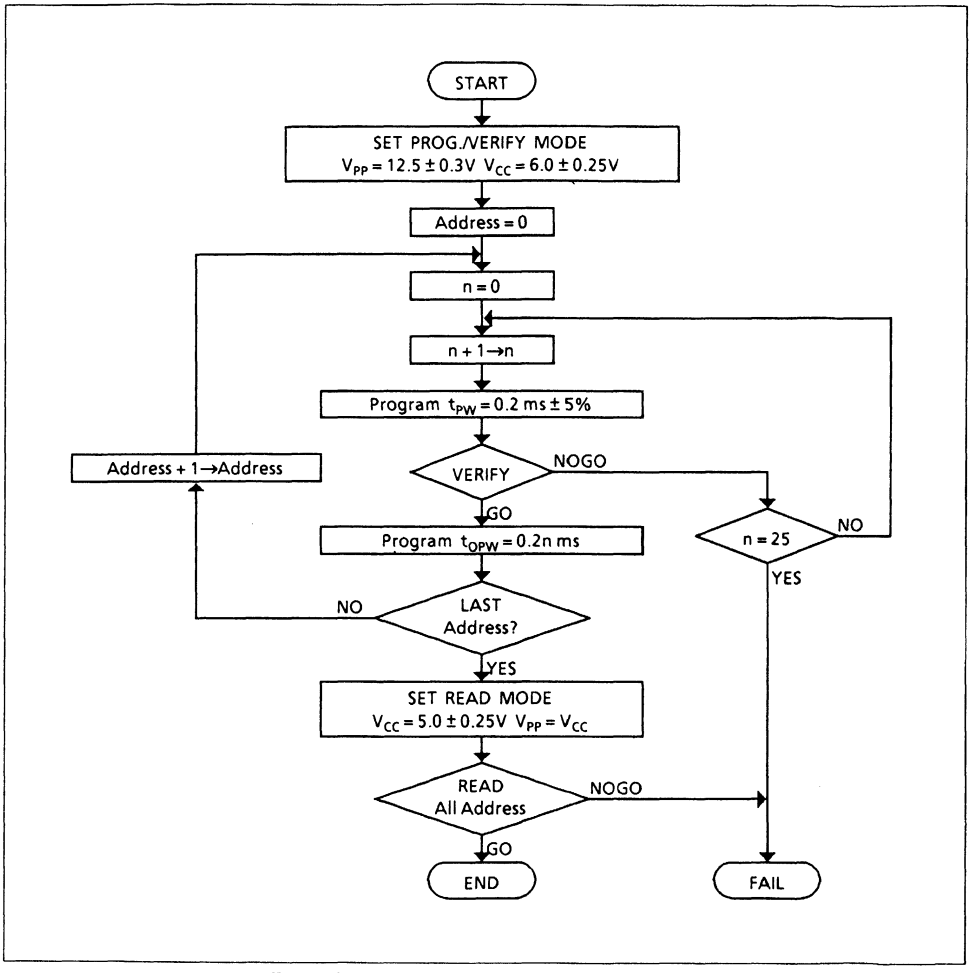
Note: t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Read Timing Waveform



Fast High-Reliability Programming

This device can be applied the programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	40	mA	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1*5	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5*6	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes:
1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns.
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

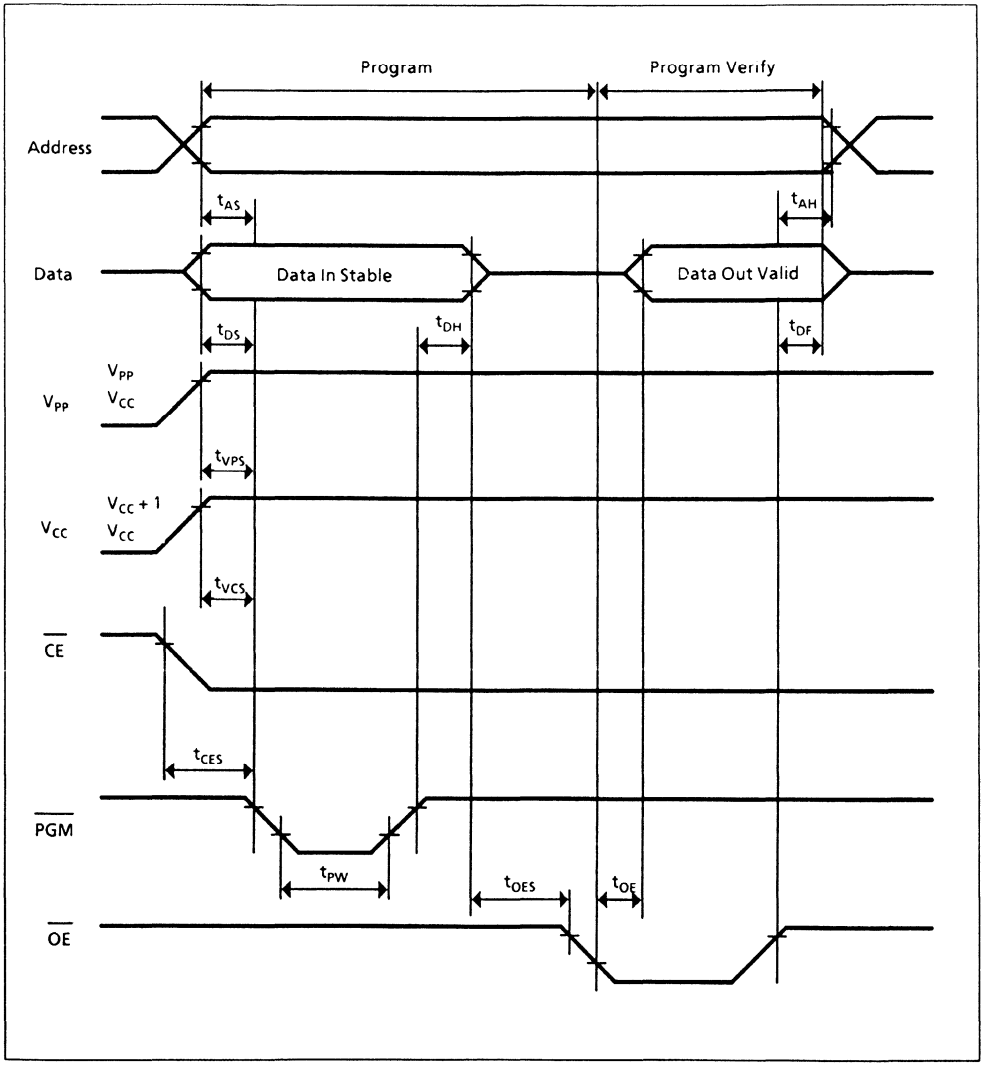
Test condition

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	2	—	—	µs	
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms	
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms	
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs	
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns	

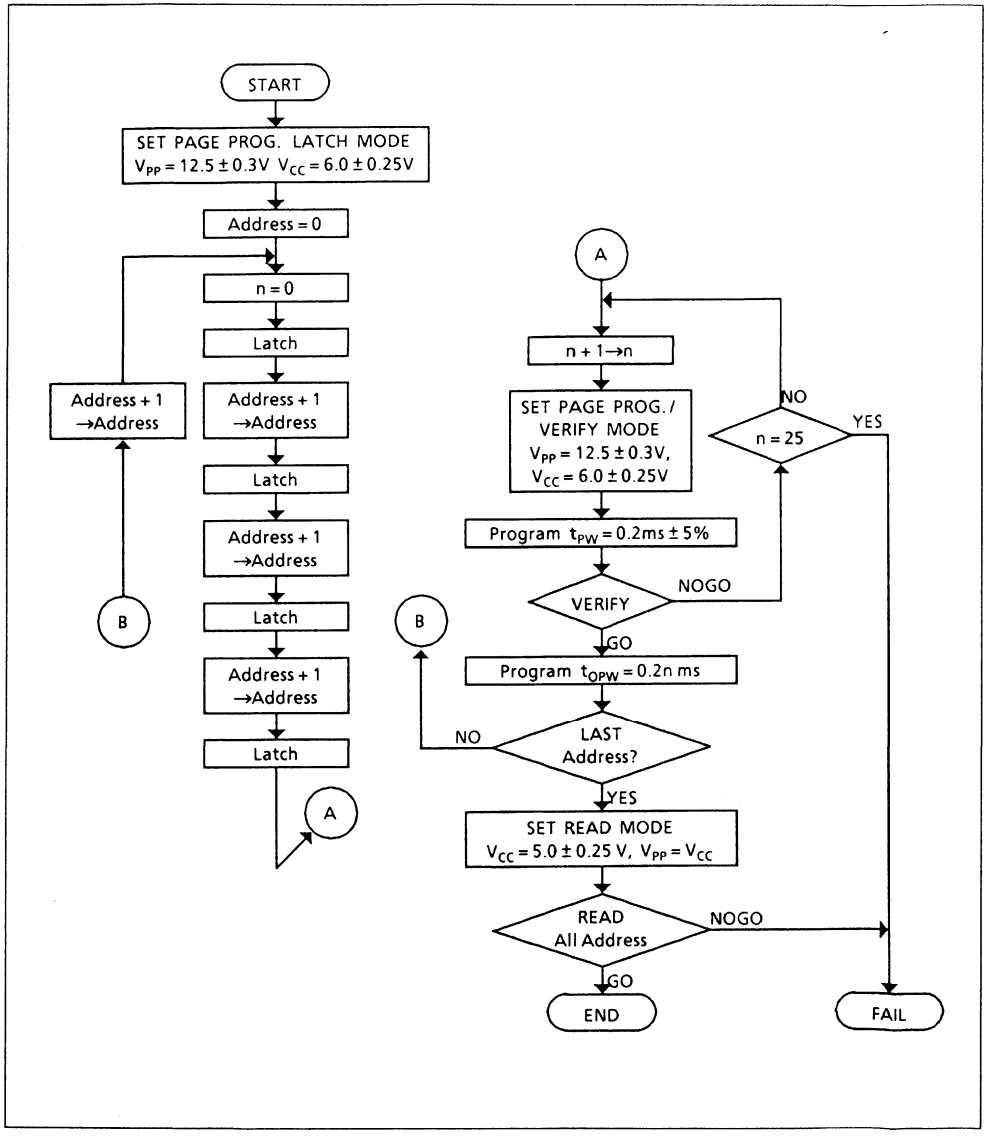
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Programming Timing Waveform



Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



Fast High-Reliability Page Programming Flowchart

DC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = 0 V to V_{CC}
V_{PP} supply current	I_{PP}	—	—	50	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IH}, $\overline{PGM}$ = V_{IL}
Operating V_{CC} current	I_{CC}	—	—	30	mA	
Input low level	V_{IL}	–0.1*5	—	0.8	V	
Input high level	V_{IH}	2.2	—	V_{CC} + 0.5*6	V	
Output low voltage during verify	V_{OL}	—	—	0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. V_{CC} must be applied before V_{PP} and removed after V_{PP}.
2. V_{PP} must not exceed 13.5 V including overshoot.
3. An influence may be had upon device reliability if the device is installed or removed while V_{PP} = 12.5 V.
4. Do not alter V_{PP} either V_{IL} to 12.5 V or 12.5 V to V_{IL} when $\overline{CE}$ = Low.
5. V_{IL} min = –0.6 V for pulse width ≤ 20 ns
6. If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.

AC Characteristics (Ta = 25°C ± 5°C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V)

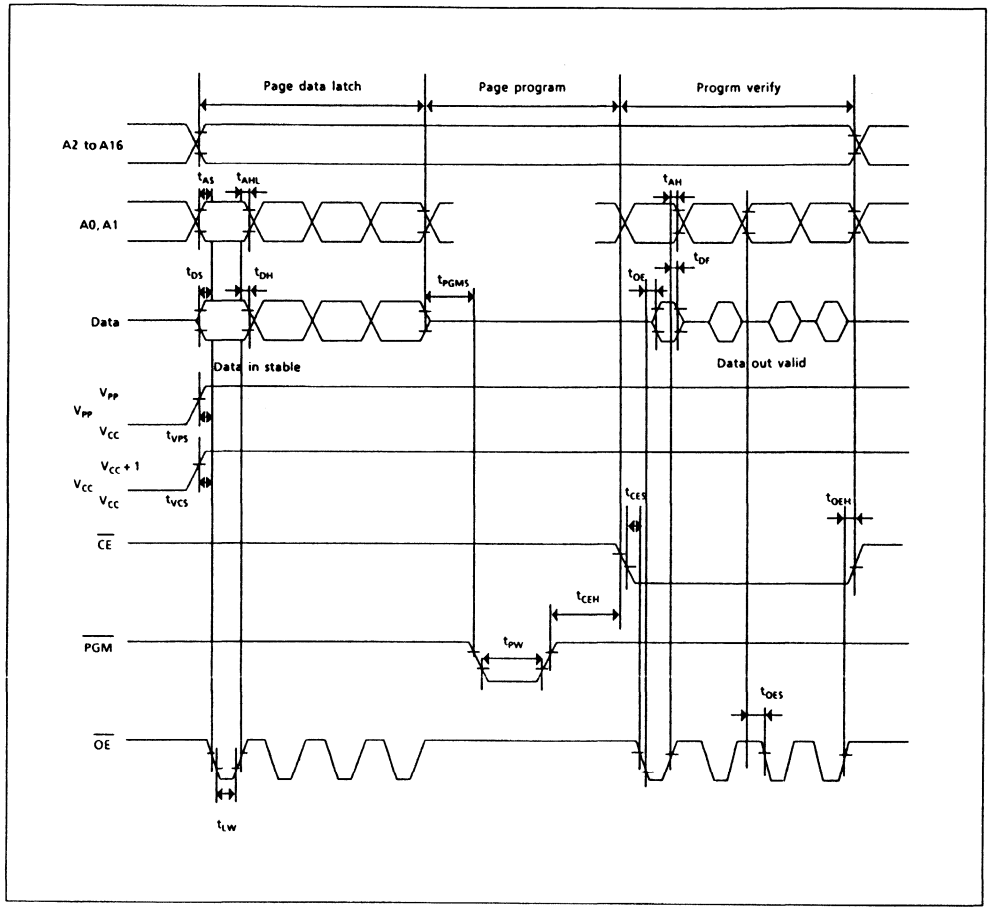
Test condition

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V
  Outputs; 0.8 V and 2.0 V

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2	—	—	µs
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs
Data setup time	t_{DS}	2	—	—	µs
Address hold time	t_{AH}	0	—	—	µs
	t_{AHL}	2	—	—	µs
Data hold time	t_{DH}	2	—	—	µs
$\overline{OE}$ to output float delay	t_{DF}*1	0	—	130	ns
V_{PP} setup time	t_{VPS}	2	—	—	µs
V_{CC} setup time	t_{VCS}	2	—	—	µs
$\overline{PGM}$ initial programming pulse width	t_{PW}	0.19	0.2	0.21	ms
$\overline{PGM}$ overprogramming pulse width	t_{OPW}*2	0.19	—	5.25	ms
$\overline{CE}$ setup time	t_{CES}	2	—	—	µs
Data valid from $\overline{OE}$	t_{OE}	0	—	150	ns
$\overline{OE}$ pulse width during data latch	t_{LW}	1	—	—	µs
$\overline{PGM}$ setup time	t_{PGMS}	2	—	—	µs
$\overline{CE}$ hold time	t_{CEH}	2	—	—	µs
$\overline{OE}$ hold time	t_{OEH}	2	—	—	µs

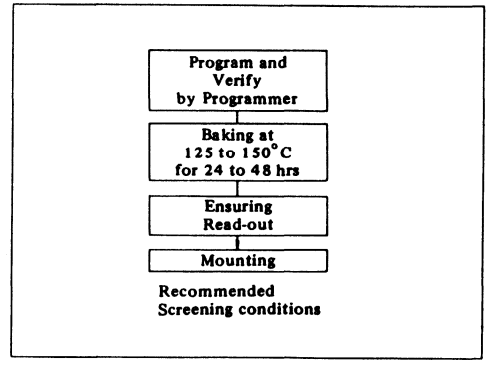
Notes: 1. t_{DF} is defined as the time at which the output achieves the open circuit condition and data is no longer driven.
2. Refer to the programming flowchart for t_{OPW}.

Fast High-Reliability Page Programming Timing Waveform



Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.



Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C101AP/AFP Identifier Code

Identifier	A0 (12)	A9 (26)	I/O7 (21)	I/O6 (20)	I/O5 (19)	I/O4 (18)	I/O3 (17)	I/O2 (15)	I/O1 (14)	I/O0 (13)	Hex Data
Manufacturer code	V_{IL}	V_H	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	V_H	0	0	1	1	1	0	0	0	38

Notes: 1. $V_H = 12.0\ V \pm 0.5\ V$
2. A1 – A8, A10 – A16, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$

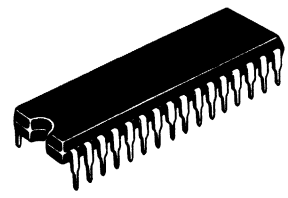
HN27C301P Series
HN27C301FP Series

131072-word x 8-bit CMOS One Time Electrically Programmable ROM

The HN27C301P Series are 131072-word x 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C301P/FP Series are in the "1" state (output high).

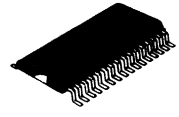
Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32 pin plastic package, therefore, this device cannot be rewritten and erased.

HN27C301P Series



(DP-32)

HN27C301FP Series



(FP-32D)

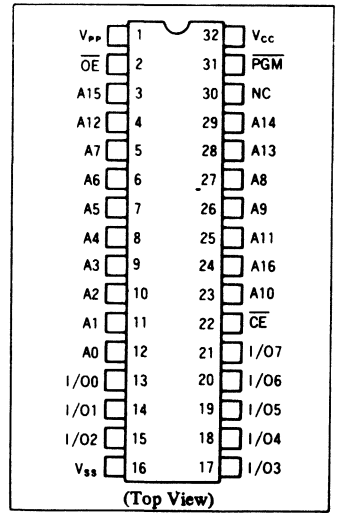
Features

- High speed
  - Access time . . . . . 200/250 ns (max.)
- Low power dissipation
  - Active mode 50 mW/MHz (typ.)
  - Standby mode 5 μW (typ.)
- Single power supply +5V ± 5%
- Fast High-Reliability program mode and Fast High-Reliability page program mode
  - Program voltage: +12.5V DC
  - Fast High-Reliability programming available
- Static . . . . . No clocks required
- Inputs and output TTL compatible during both read and program modes.
- Pin Arrangement: Replaceable 1-Mbit Mask ROM (28-pin type)

Ordering Information

Type No.	Access time	Package
HN27C301P-20	200ns	600 mil 32 pin
HN27C301P-25	250ns	Plastic DIP
HN27C301FP-20	200ns	32 pin
HN27C301FP-25	250ns	Plastic SOP

Pin Arrangement

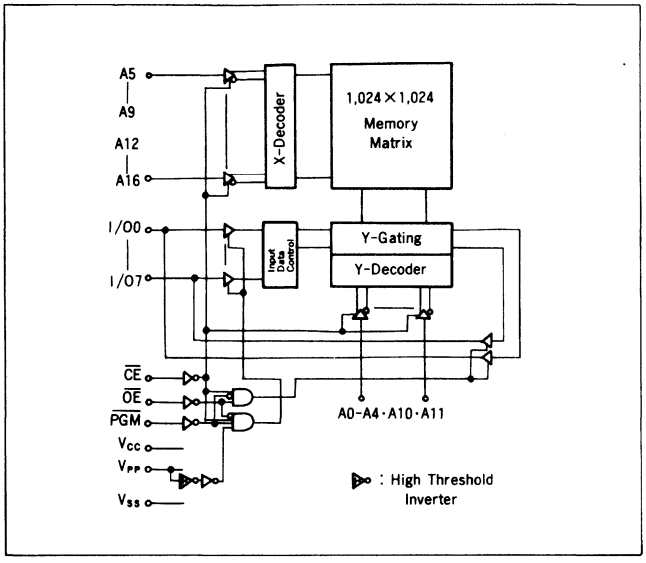


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/Output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Dout
Page Data Latch	V_{IH}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Din
Page Program	V_{IH}	V_{IH}	V_{IL}	V_{PP}	V_{CC}	High Z
Program Inhibit	V_{IL}	V_{IL}	V_{IL}	V_{PP}	V_{CC}	High Z
	V_{IL}	V_{IH}	V_{IH}			
	V_{IH}	V_{IL}	V_{IL}			
	V_{IH}	V_{IH}	V_{IH}			

Note) 1. X: Don't care.

Electrical Characteristics

Refer to the HN27C101P/FP data sheet.

HN27C301AP Series
HN27C301AFP Series

131072-Word × 8-Bit CMOS One Time Electrically Programmable ROM

The HN27C301AP/AFP series are 131072-word × 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C301AP/AFP series are in the "1" state (output high).
Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32-pin plastic package, therefore, this device cannot be rewritten and erased.

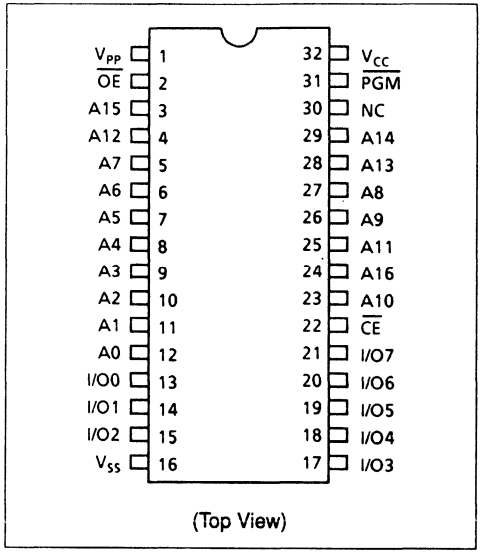
Features

- Single power supply: +5 V ± 10%
- Fast high-reliability programming mode and fast high-reliability page programming mode
  –Programming voltage: +12.5 V DC
  –Fast high-reliability page programming:
  14 sec typ
- High speed inputs and outputs TTL compatible during both read and write program modes
- Low power dissipation: 50 mW/MHz typ (active)
  5 µW typ (standby)
- Pin arrangement: replaceable mask ROM (32-pin)
- Device identifier mode: manufacturer code and device code

Ordering Information

Type No.	Access time	Package
HN27C301AP-12	120 ns	600-mil 32-pin plastic DIP (DP-32)
HN27C301AP-15	150 ns	
HN27C301AP-20	200 ns	
HN27C301AP-25	250 ns	
HN27C301AFP-12	120 ns	32-pin plastic SOP (FP-32D)
HN27C301AFP-15	150 ns	
HN27C301AFP-20	200 ns	
HN27C301AFP-25	250 ns	

Pin Arrangement

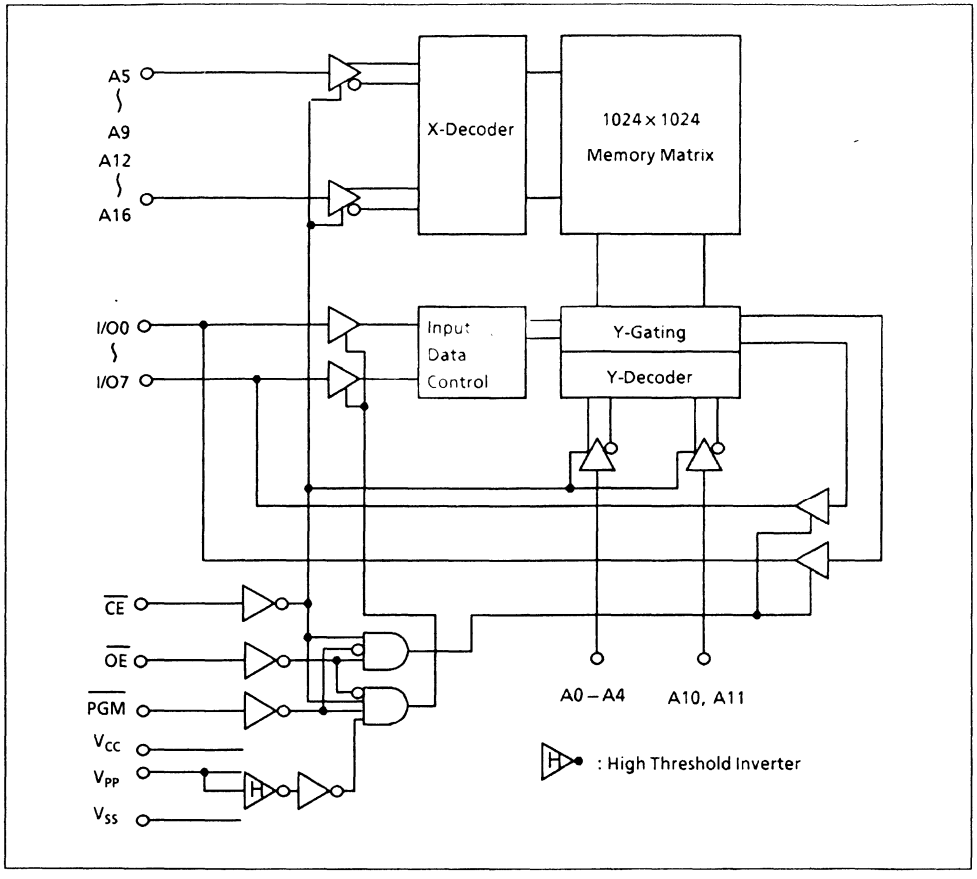


(Top View)

Pin Description

Pin name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
V_{CC}	Power supply
V_{PP}	Programming power supply
V_{SS}	Ground
$\overline{PGM}$	Programming enable
NC	No connection

Block Diagram



Mode Selection

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (2)	$\overline{PGM}$ (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Read	V_{IL}	V_{IL}	V_{IH}	×	V_{CC}	V_{CC}	Dout
Output disable	V_{IL}	V_{IH}	V_{IH}	×	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	×	×	×	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	Din
Program verify	V_{IL}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Dout
Page data latch	V_{IH}	V_{IL}	V_{IH}	×	V_{PP}	V_{CC}	Din

Mode Selection (cont)

Mode	$\overline{CE}$ (22)	$\overline{OE}$ (2)	$\overline{PGM}$ (31)	A9 (26)	V_{PP} (1)	V_{CC} (32)	I/O (13 – 15, 17 – 21)
Page program	V_{IH}	V_{IH}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
Program inhibit	V_{IL}	V_{IL}	V_{IL}	×	V_{PP}	V_{CC}	High-Z
	V_{IL}	V_{IH}	V_{IH}				
	V_{IH}	V_{IL}	V_{IL}				
	V_{IH}	V_{IH}	V_{IH}				
Identifier	V_{IL}	V_{IL}	V_{IH}	V_H	V_{CC}	V_{CC}	Code

Notes: 1. × = Don't care
2. V_H = 12.0 V ± 0.5 V

Electrical Characteristics

Refer to the HN27C101AP/AFP data sheet.

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

HN27C301AP/AFP Identifier Code

Identifier	A0 (12)	A9 (26)	I/O7 (21)	I/O6 (20)	I/O5 (19)	I/O4 (18)	I/O3 (17)	I/O2 (15)	I/O1 (14)	I/O0 (13)	Hex Data
Manufacturer code	V_{IL}	V_H	0	0	0	0	0	1	1	1	07
Device code	V_{IH}	V_H	1	0	1	1	1	0	0	1	B9

Notes: 1. V_H = 12.0 V ± 0.5 V
2. A1 – A8, A10 – A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}

ECL
RAM

HM10490 Series — Preliminary

65536-words x 1-bit Fully Decoded Random Access Memory

The HM10490 is ECL 10k compatible, 65536-words by 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

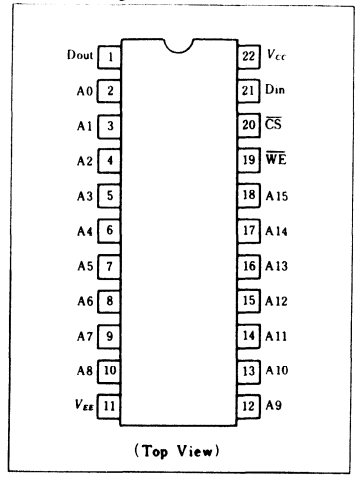
Features

- 65,536-words x 1-bit organization
- Fully compatible with 10k ECL level
- Address access time . . . . . 10/12ns (max.)
- Write pulse width . . . . . 6/8ns (min.)
- Low power dissipation . . . . . 570mW (typ.)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access Time	Package
HM10490-10	10 ns	300mil 22pin Cerdip (DG-22N)
HM10490-12	12 ns	

Pin Arrangement

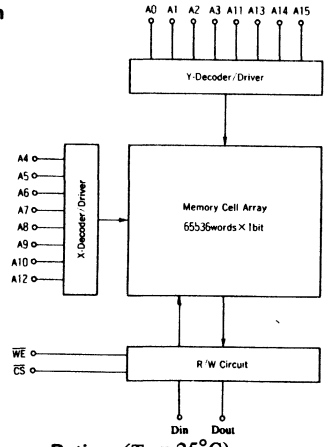


Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) ×: Irrelevant
*: Read Out Noninvert

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	℃
Storage Temperature	T_{stg}(Bias)*	−55 to +125	℃

*Under Bias (V_{EE}=−6Vmin)

Electrical Characteristics

DC Characteristics (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition	
Output Voltage	V_{OH}	-1000	—	-840	mV	V_{in} = V_{IHA} or V_{ILB}	0°C
		-960	—	-810			+25°C
		-900	—	-720			+75°C
	V_{OL}	-1870	—	-1665			0°C
		-1850	—	-1650			+25°C
		-1830	—	-1625			+75°C
Output Threshold Voltage	V_{OHC}	-1020	—	—	mV	V_{in} = V_{IHB} or V_{ILA}	0°C
		-980	—	—			+25°C
		-920	—	—			+75°C
	V_{OLC}	—	—	-1645			0°C
		—	—	-1630			+25°C
		—	—	-1605			+75°C
Input Voltage	V_{IH}	-1145	—	-840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		-1105	—	-810			+25°C
		-1045	—	-720			+75°C
	V_{IL}	-1870	—	-1490		Guaranteed Input Voltage Low for All Inputs	0°C
		-1850	—	-1475			+25°C
		-1830	—	-1450			+75°C
Input Current	I_{IH}	—	—	220	μA	V_{in} = V_{IHA}	0 to +75°C
	I_{IL}	0.5	—	170		$\overline{CS}$ — V_{in} = V_{ILB}	0 to +75°C
		-50	—	—		Others	
Supply Current	I_{EE}	-140	—	—	mA	All Inputs and Outputs Open.	0°C
		-140	—	—			+75°C

AC Characteristics (V_{EE} = -5.2V ±5%, Ta = 0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	HM10490-10 min	typ	max	HM10490-12 min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recoverry Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM10490-10 min	typ	max	HM10490-12 min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	6	—	—	8	—	—	ns	t_{WSA}=t_{WSA}min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	t_W=$t_W$min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

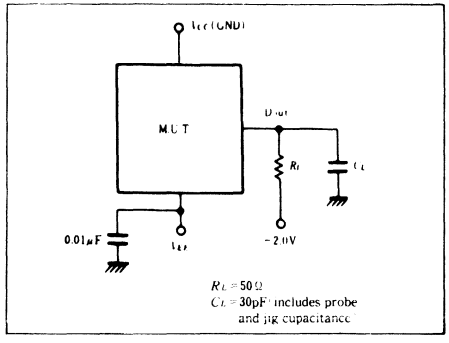
Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

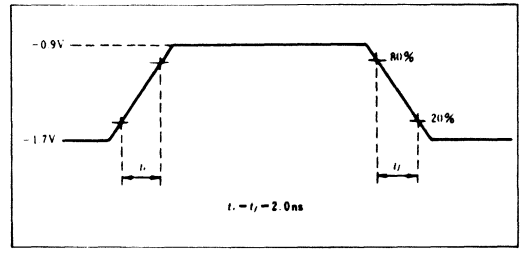
Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Input Capacitance	C_{in}	—	3	—	pF	
Output Capacitance	C_{out}	—	5	—	pF	

Test Circuit and Waveforms

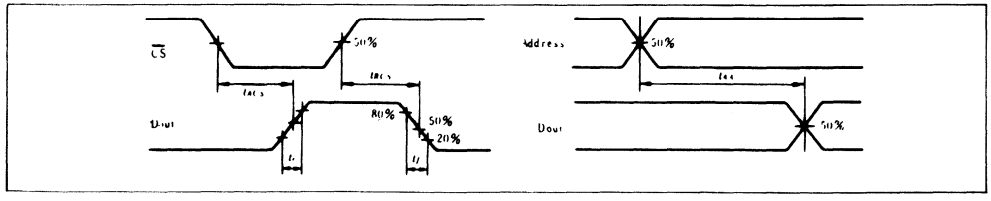
Loading Condition



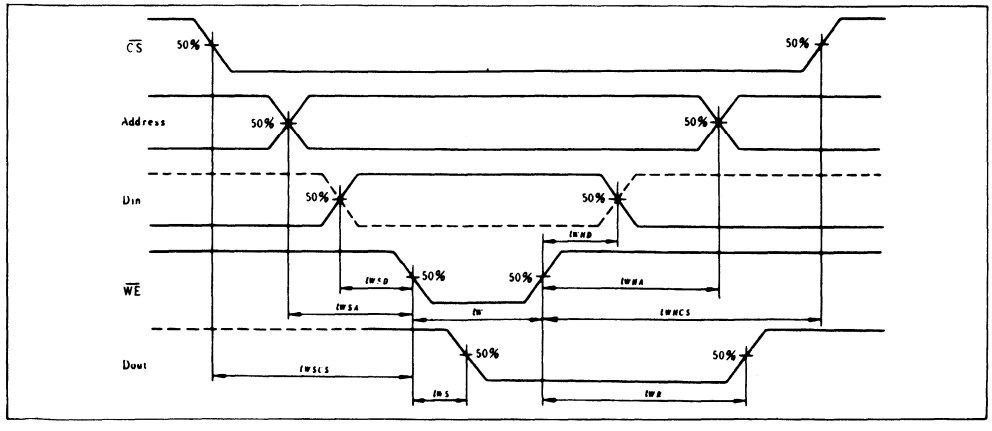
Input Pulse



Read Mode



Write Mode



HM10500-15 — Preliminary

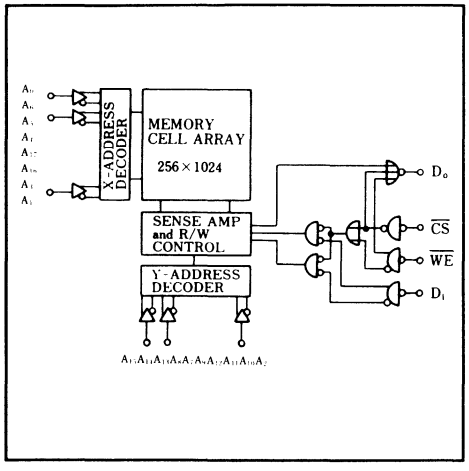
262144-words x 1-bit Fully Decoded Random Access Memory

HM10500-15 is ECL 10K compatible, 262144-words x 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

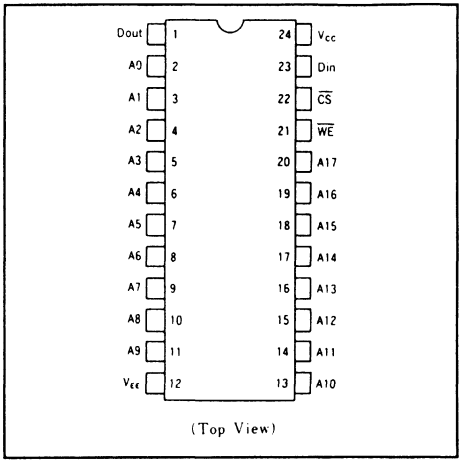
Features

- 262,144-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time : 15ns (max)
- Write pulse width : 10ns (min)
- Low power dissipation : 520mW (typ)
- Output obtainable by wired-OR (open emitter)

Block Diagram



Pin Arrangement



(Top View)

Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X : Irrelevant
* : Read Out Noninvert

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias (V_{EE} = −6Vmin)

Electrical Characteristics

DC Characteristics (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min (B)	typ	max (A)	Unit	Test Condition	
Output Voltage	V_{OH}	−1000	–	−840	mV	V_{in}=V_{IHA} or V_{ILB}	0°C
		−960	–	−810			+25°C
		−900	–	−720			+75°C
	V_{OL}	−1870	–	−1665			0°C
		−1850	–	−1650			+25°C
		−1830	–	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	–	–	mV	V_{in}=V_{IHB} or V_{ILA}	0°C
		−980	–	–			+25°C
		−920	–	–			+75°C
	V_{OLC}	–	–	−1645			0°C
		–	–	−1630			+25°C
		–	–	−1605			+75°C
Input Voltage	V_{IH}	−1075	–	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1055	–	−810			+25°C
		−1045	–	−720			+75°C
	V_{IL}	−1870	–	−1550		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	–	−1525			+25°C
		−1830	–	−1475			+75°C
Input Current	I_{IH}	–	–	220	μA	V_{in}=V_{IHA}	0 to +75°C
	I_{IL}	0.5	–	170		$\overline{CS}$ — V_{in}=V_{ILB}	0 to +75°C
		−50	–	–		Others	
Supply Current	I_{EE}	−180	–	–	mA	All Inputs and Outputs Open, Test Pin 12	Ta=0°C
		−180	–	–			Ta=75°C

AC Characteristics (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	–	–	15	ns	
Chip Select Recovery Time	t_{RCS}	–	–	10	ns	
Address Access Time	t_{AA}	–	–	15	ns	

HM10500-15

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	10	–	–	ns	t_{WSA}=2ns
Data Setup Time	t_{WSD}	2	–	–	ns	
Data Hold Time	t_{WHD}	3	–	–	ns	
Address Setup Time	t_{WSA}	2	–	–	ns	t_W=10ns
Address Hold Time	t_{WHA}	3	–	–	ns	
Chip Select Setup Time	t_{WSCS}	2	–	–	ns	
Chip Select Hold Time	t_{WHCS}	3	–	–	ns	
Write Disable Time	t_{WS}	–	–	10	ns	
Write Recovery Time	t_{WR}	–	–	18	ns	

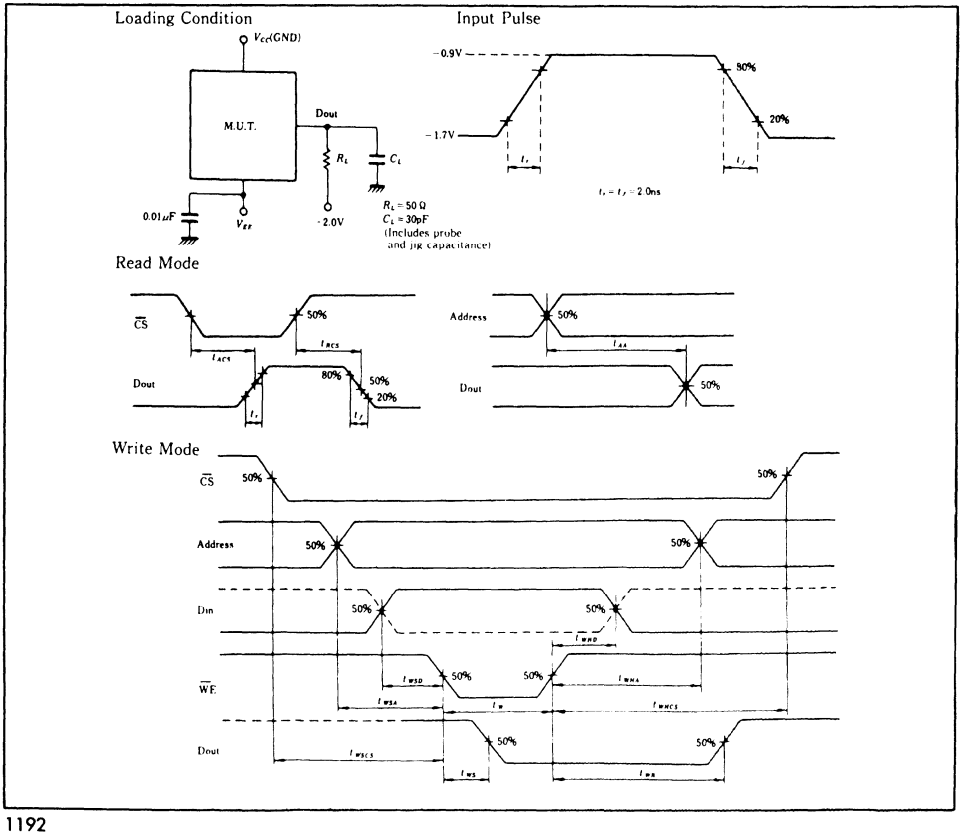
Rise/Fall Time

Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	–	2	–	ns	
Output Fall Time	t_f	–	2	–	ns	

Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	C_{in}	–	3	–	pF	
Output Capacitance	C_{out}	–	5	–	pF	

Test Circuit and Waveforms



HM10504 Series

65536-Word × 4-Bit Random Access Memory

The HM10504 is ECL 10K compatible, 65536-word by 4-bit read/write random access memory developed for high speed systems such as cache and control/buffer storage.

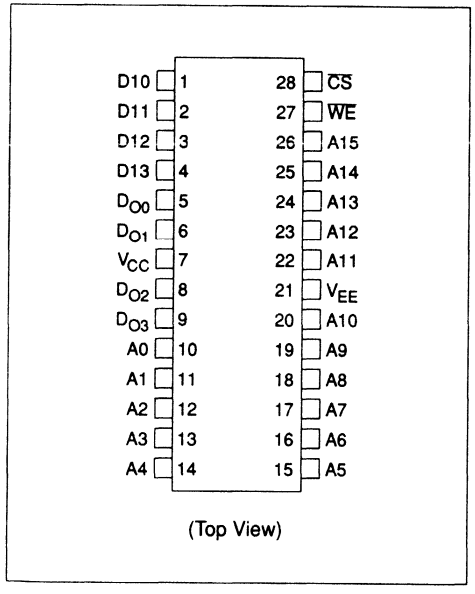
Features

- 65536-word × 4-bit organization
- Fully compatible with 10K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 10/12 ns (max)
- Write pulse width: 8 ns (min)
- Low power dissipation: 500 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM10504F-10	10 ns	28-pin ceramic flat (30-mil lead pitch)
HM10504F-12	12 ns	

Pin Arrangement

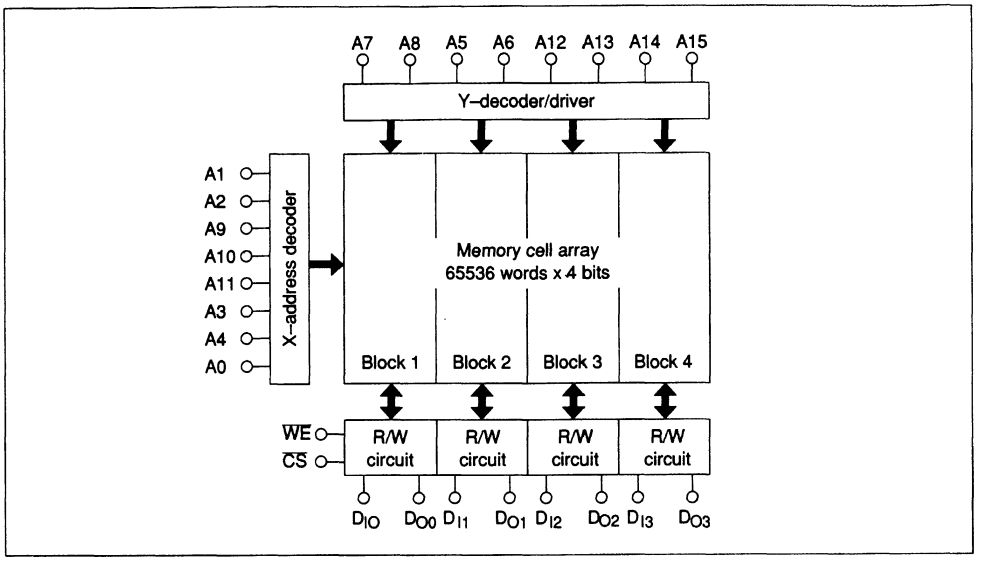


(Top View)

Pin Description

Pin name	Function
A0 – A15	Address input
$D_{I0} - D_{I3}$	Data input
$D_{O0} - D_{O3}$	Data Output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	× *1	× *1	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	× *1	Dout *2	Read

Notes: *1 Irrelevant
*2 Read out noninvert

Absolute Maximum Rating (Ta = 25°C)

Item	Sumbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to + 150	°C
Storage temperature	Tstg (Bias) *1	–55 to + 125	°C

Note: *1 Under bias (V_{EE} = –6 V min)

HM100490 Series — Preliminary

65536-words x 1-bit Fully Decoded Random Access Memory

The HM100490 is ECL 100k compatible, 65536-words by 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

- 65,536-words x 1-bit organization
- Fully compatible with 100k ECL level
- Address access time . . . . . 10/12ns (max.)
- Write pulse width . . . . . 6/8ns (min.)
- Low power dissipation . . . . . 500mW (typ.)
- Output obtainable by wired-OR (open emitter)

Ordering Information

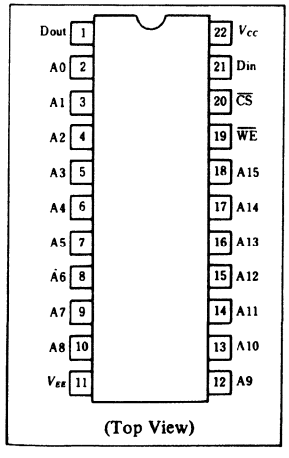
Type No.	Access Time	Package
HM100490-10	10ns	300-mil 22-pin Cerdip
HM100490-12	12ns	(DG-22N)

Function Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X: Irrelevant
*: Read Out Noninvert

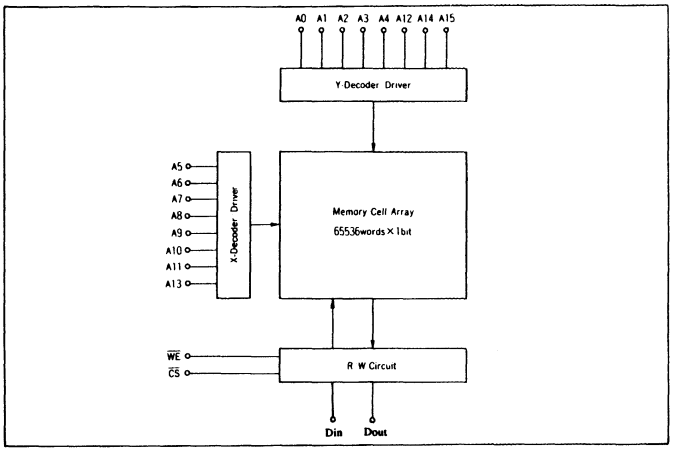
Pin Arrangement



(Top View)

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to −3.0	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

*Under Bias (V_{EE}=−6Vmin)

Electrical Characteristics

DC Characteristics

(V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	V_{in}=V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	V_{in}=V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Inputs Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	μA	V_{in}=V_{IHA}
	I_{IL}	0.5	—	170	μA	V_{in}=V_{ILB} $\overline{CS}$
		−50	—	—		Others
Supply Current	I_{EE}	−120	—	—	mA	All Inputs and Outputs Open

AC Characteristics

(V_{EE} = −4.5V ± 5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	HM100490-10			HM100490-12			Unit
		min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns
Address Access Time	t_{AA}	—	—	10	—	—	12	ns

Write Mode

Item	Symbol	HM100490-10 min	typ	max	HM100490-12 min	typ	min	Unit	Test Condition
Write Pulse Width	t_W	6			8			ns	$t_{WSA} = t_{WSA}$ min
Data Setup Time	t_{WSD}	2			2			ns	
Data Hold Time	t_{WHD}	2			2			ns	
Address Setup Time	t_{WSA}	2			2			ns	$t_W = t_W$ min
Address Hold Time	t_{WHA}	2			2			ns	
Chip Select Setup Time	t_{WSCS}	2			2			ns	
Chip Select Hold Time	t_{WHCS}	2			2			ns	
Write Disable Time	t_{WS}			6			8	ns	
Write Recovery Time	t_{WR}			12			14	ns	

Rise/Fall Time

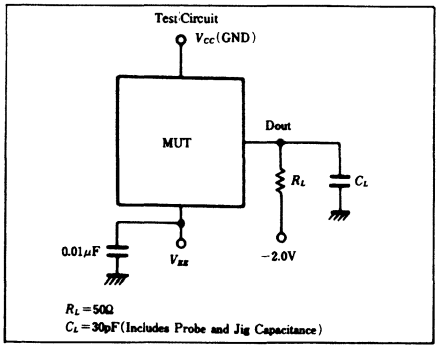
Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

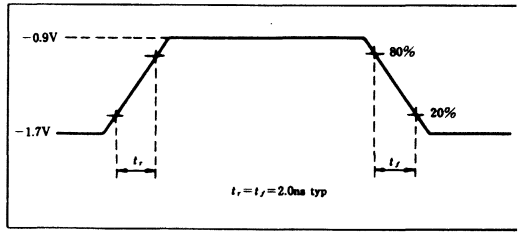
Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

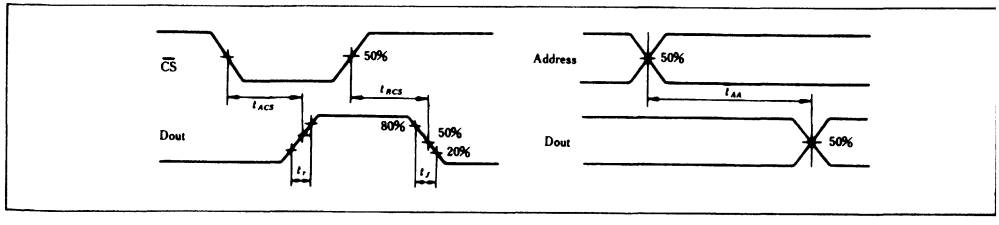
Loading Condition



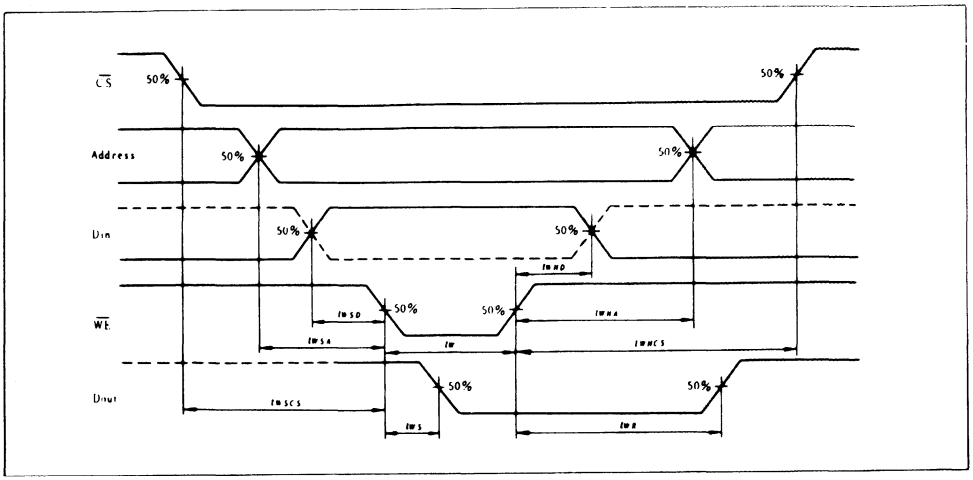
Input Pulse



Read Mode



Write Mode


CS
Address
Din
WE
Dout
50%
tWHD
tWSD
tWSA
tW
tWHA
tWHCS
tWSCS
tWS
tWR

HM101490 Series — Preliminary

65536-Words × 1-Bit Fully Decoded Random Access Memory

The HM101490 is ECL 100K compatible, 65536-words by 1-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

- 65536 × 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6/8 ns (min)
- Low power dissipation: 570 mV (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

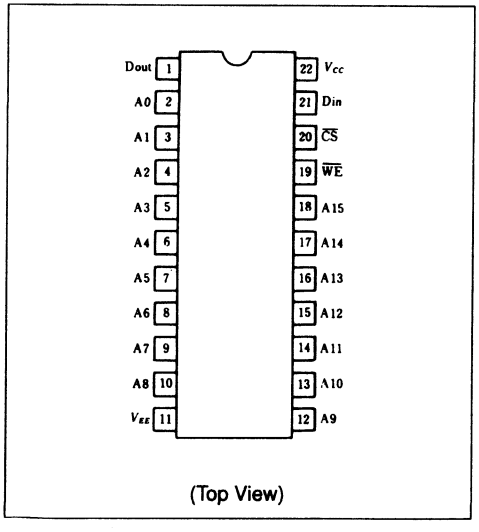
Type No.	Access time	Package
HM101490-10	10 ns	300 mil 22 pin cerdip (DG-22N)
HM101490-12	12 ns	

Function Table

Input				
$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	×	×	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes: ×: Irrelevant *: Read out noninvert

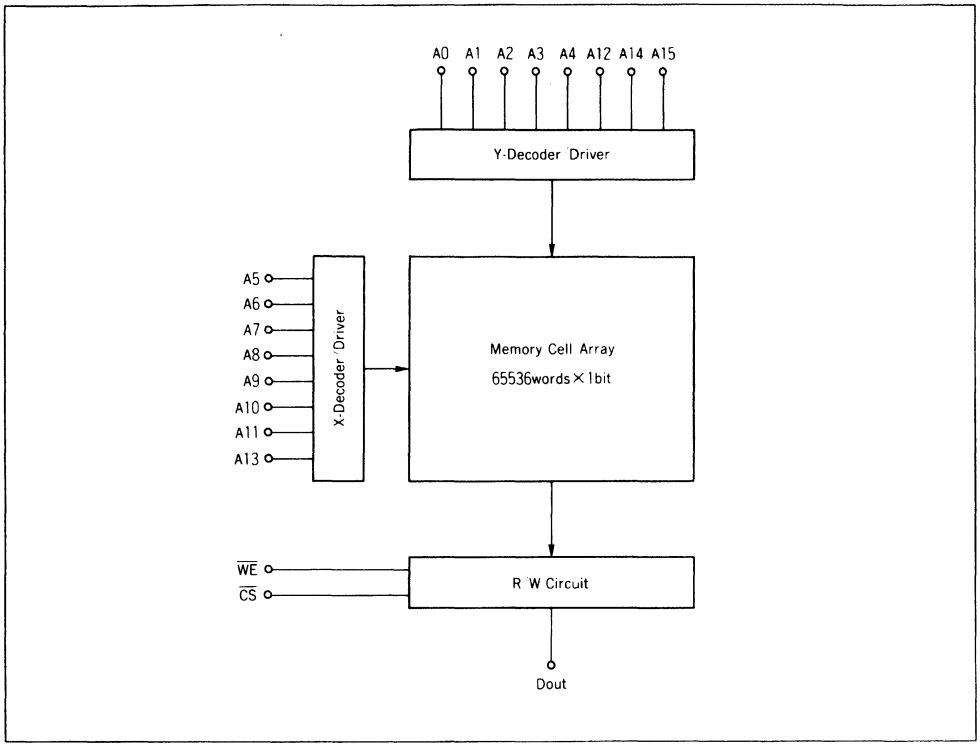
Pin Arrangement



(Top View)

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to –3.0	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: *1 Under Bias (V_{EE} = –6 V min)

Electrical Characteristics

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/Low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—	µA		Others
Supply current	I_{EE}	–140	—	—	mA	All inputs and outputs open	

AC Characteristics (V_{EE} = –5.2 V ± 5%, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

		HM101490-10			HM101490-12				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test conditions
Chip select access time	t_{ACS}	—	—	6	—	—	8	ns	
Chip select recovery time	t_{RCS}	—	—	6	—	—	8	ns	
Address access time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM101490-10 Min	Typ	Max	HM101490-12 Min	Typ	Max	Unit	Test conditions
Write pulse width	t_W	6	—	—	8	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	2	—	—	2	—	—	ns	
Data hold time	t_{WHD}	2	—	—	2	—	—	ns	
Address setup time	t_{WSA}	2	—	—	2	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	2	—	—	2	—	—	ns	
Chip select setup time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip select hold time	W_{HCS}	2	—	—	2	—	—	ns	
Write disable time	t_{WS}	—	—	6	—	—	8	ns	
Write recovery time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

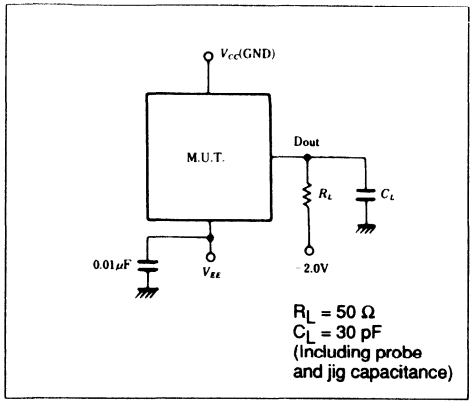
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Capacitance

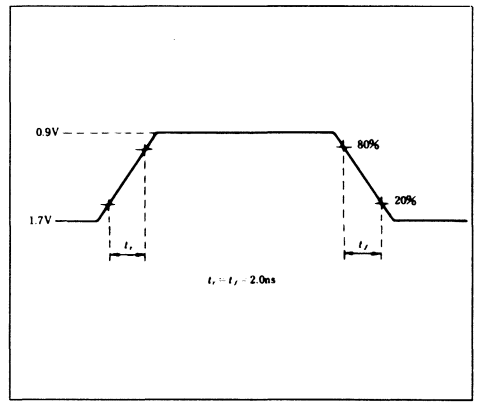
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

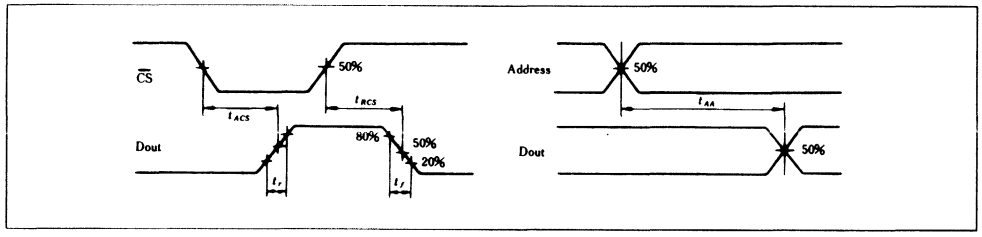
Loading Condition



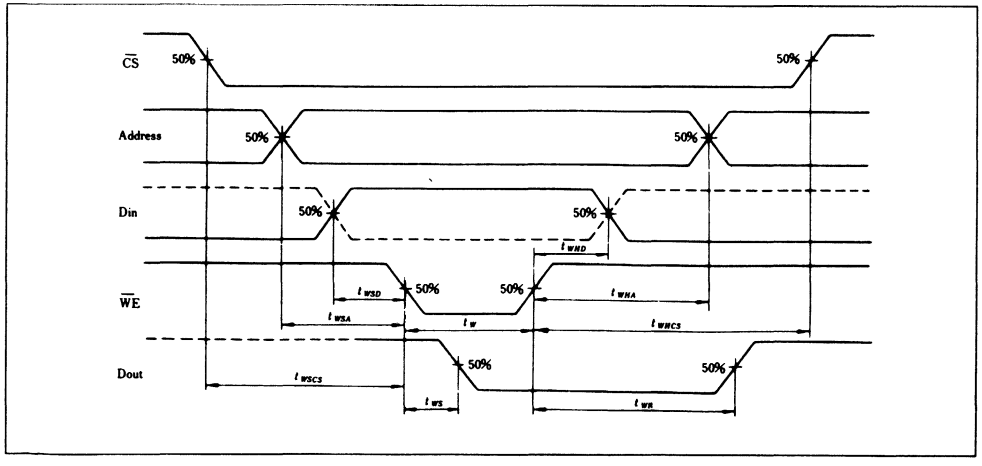
Input Pulse



Read Mode



Write Mode



HM10494 Series — Preliminary

16384-word × 4-bit Fully Decoded Random Access Memory

The HM10494 is ECL 10K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

- 16384-word × 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6/8 ns (min)
- Low power dissipation: 800 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

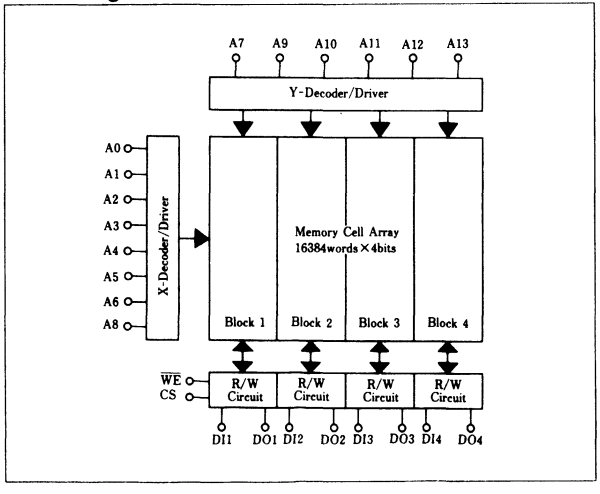
Type No.	Access Time	Package
HM10494-10	10 ns	400 mil 28-pin
HM10494-12	12 ns	Cerdip (DG-28N)
HM10494F-10	10ns	28-pin Ceramic
HM10494F-12	12ns	Flat (FG-28D)

Function Table

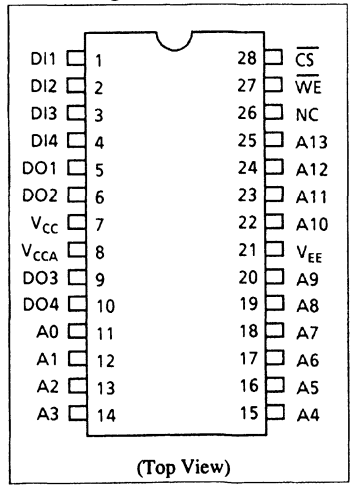
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature	Tstg (Bias)*1	−55 to +125	°C

Note: *1; Under Bias (V_{EE} = −6 Vmin)

Electrical Characteristics

DC Characteristics (V_{EE}=−5.2 V, R_L=50 Ω to −2.0 V, Ta*=0 to +75°C(air flow exceeding 2 m/sec), Tc*=0 to +75°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions	
Output Voltage	V_{OH}	−1000	—	−840	mV	Vin = V_{IHA} or V_{ILB}	0°C
		−960	—	−810			+25°C
		−900	—	−720			+75°C
	V_{OL}	−1870	—	−1665			0°C
		−1850	—	−1650			+25°C
		−1830	—	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	—	—	mV	Vin = V_{IHB} or V_{ILA}	0°C
		−980	—	—			+25°C
		−920	—	—			+75°C
	V_{OLC}	—	—	−1645			0°C
		—	—	−1630			+25°C
		—	—	−1605			+75°C
Input Voltage	V_{IH}	−1145	—	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1105	—	−810			+25°C
		−1045	—	−720			+75°C
	V_{IL}	−1870	—	−1490		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	—	−1475			+25°C
		−1830	—	−1450			+75°C
Input Current	I_{IH}	—	—	220	μA	Vin = V_{IHA}	0 to +75°C
	I_{IL}	0.5	—	170		Vin = V_{ILB} $\overline{CS}$	0 to +75°C
		−50	—	—		Vin = V_{ILB} Others	0 to +75°C
Supply Current	I_{EE}	−180	—	—	mA	All Inputs and Outputs Open	Ta = 0°C
		−180	—	—			Ta = 75°C

*Ceramic Flat .... Tc, Cerdip .... Ta

AC Characteristics (V_{EE}=−5.2 V ± 5%, Ta*=0 to +75°C(air flow exceeding 2 m/sec), Tc*=0 to +75°C)

Read Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

*Ceramic Flat .... Tc, Cerdip .... Ta

Write Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	tw	6	—	—	8	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	tw = tw min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

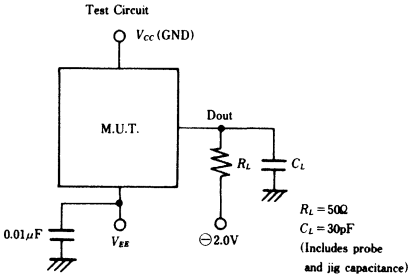
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

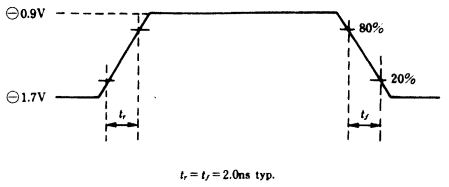
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	—	5/3	—	pF	$\overline{WE}$, $\overline{CS}$, DI1, DI2/others
Output Capacitance	Cout	—	3	—	pF	

Test Circuit and Waveforms

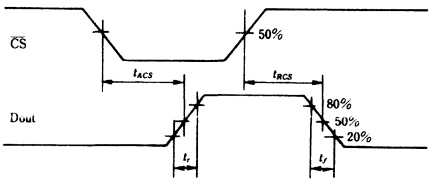
Loading Condition

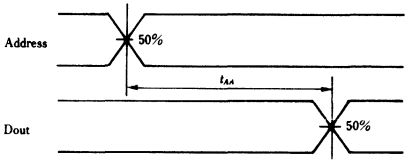


Input Pulse

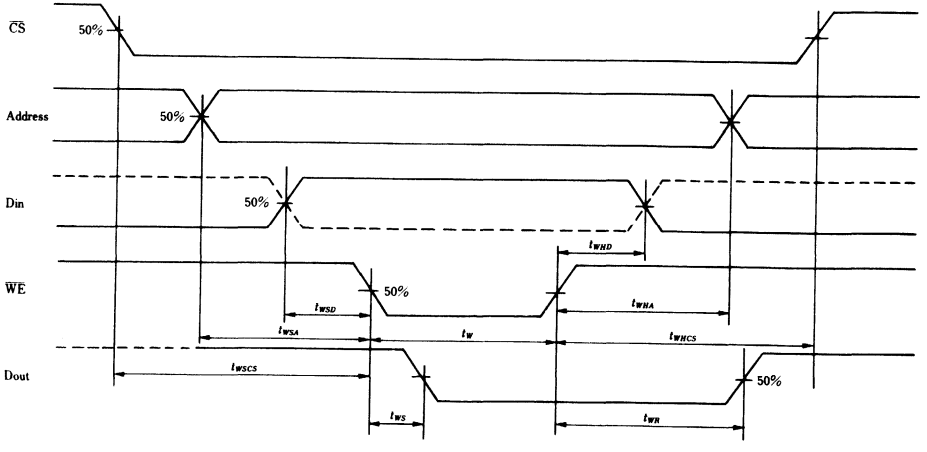


Read Mode





Write Mode



HM100494 Series — Preliminary

16384-word × 4-bit Fully Decoded Random Access Memory

The HM100494 is ECL 100K compatible, 16384-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage. The HM100494F-10/12 is encapsulated in ceramic flat package (28pin).

Features

- 16384-word × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6 ns (min)
- Low power dissipation: 650 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

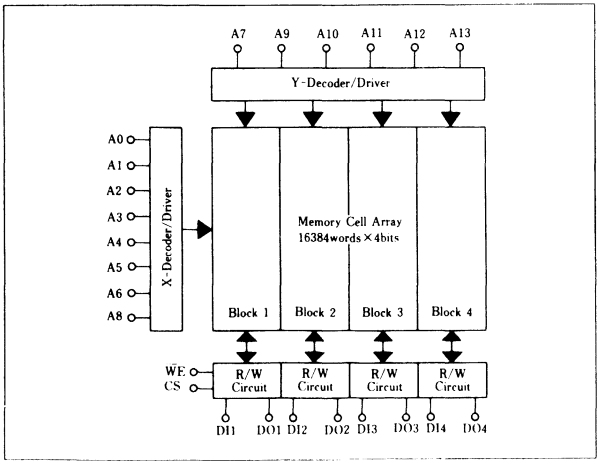
Type No.	Access Time	Package
HM100494F-10	10 ns	28-pin
HM100494F-12	12 ns	Ceramic Flat (FG-28D)

Function Table

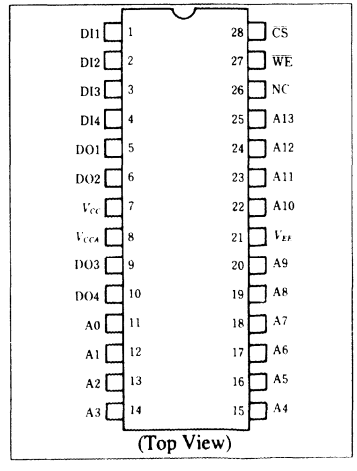
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature	Tstg (Bias)*1	−55 to +125	°C

Note: *1: Under Bias (V_{EE} = −6 Vmin)

Electrical Characteristics

DC Characteristics (V_{EE} = −4.5 V, R_L = 50Ω to −2.0 V, Tc = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Input Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		−50	—	—		Others
Supply Current	I_{EE}	−180	—	—	mA	All Inputs and Outputs Open

Note: Tc .... Ceramic Flat

AC Characteristics (V_{EE} = −4.5 V ± 5%, Tc = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM100494F-10			HM100494F-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Note: Tc .... Ceramic Flat

Write Mode

Item	Symbol	HM100494F-10			HM100494F-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	t_W	6	—	—	6	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	tw = tw min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

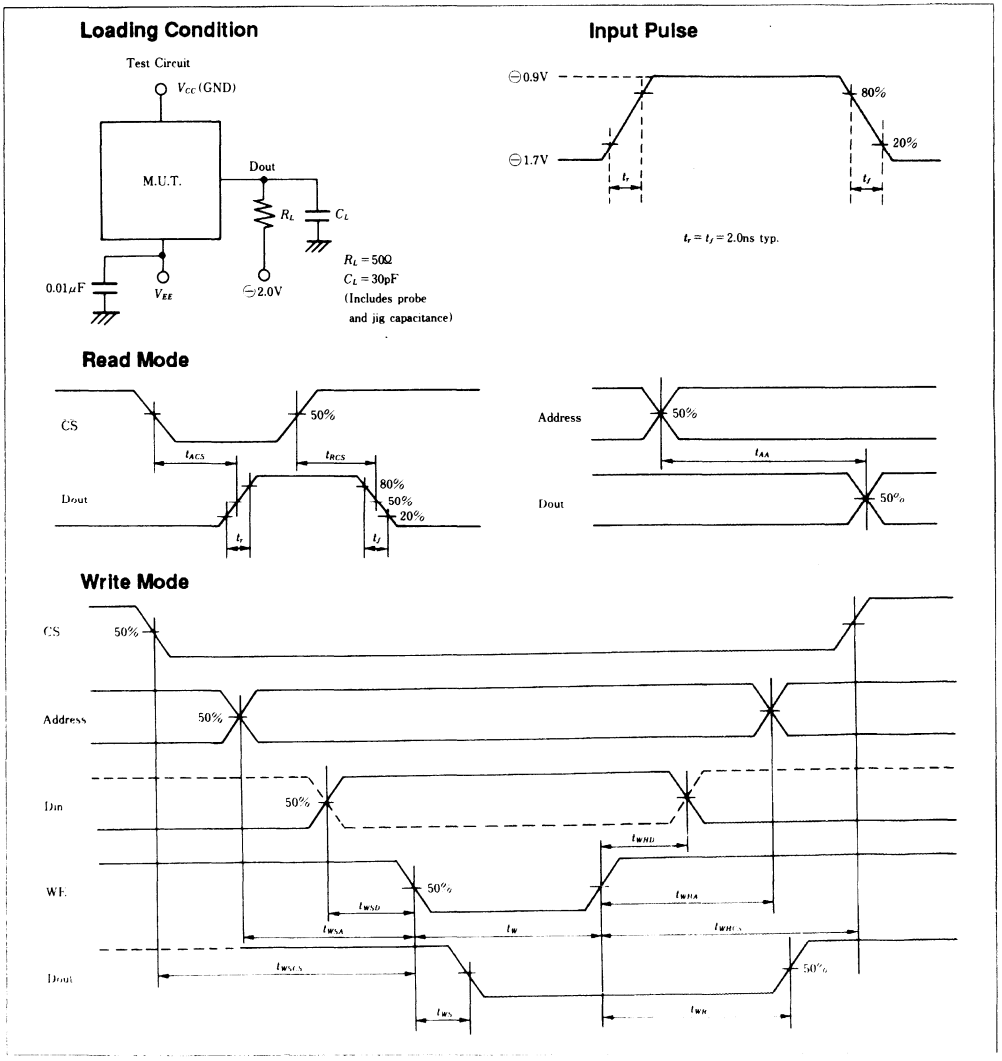
Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	Cin	—	5/3	—	pF	$\overline{WE}$, $\overline{CS}$, DI1, DI2/others
Output Capacitance	Cout	—	3	—	pF	

Test Circuit and Waveforms



HM101494 Series — Preliminary

16384-Word × 4-Bit Fully Decoded Random Access Memory

The HM101494 is ECL 100K compatible, 16384-word by 4-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

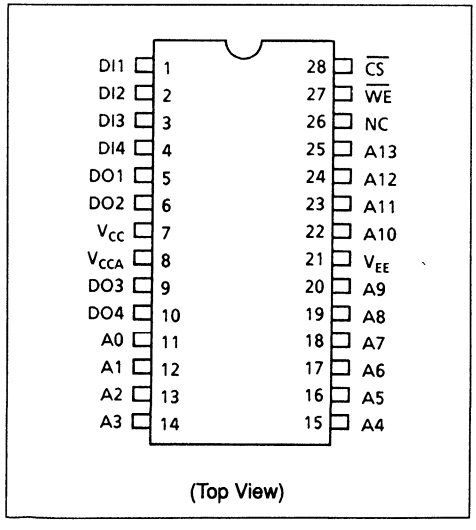
Features

- 16384 × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6/8 ns (min)
- Low power dissipation: 750 mV (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM101494-10	10 ns	400 mil 28 pin cerdip (DG-28N)
HM101494-12	12 ns	
HM101494F-10	10 ns	28 pin ceramic flat (FG-28D)
HM101494F-12	12 ns	

Pin Arrangement



(Top View)

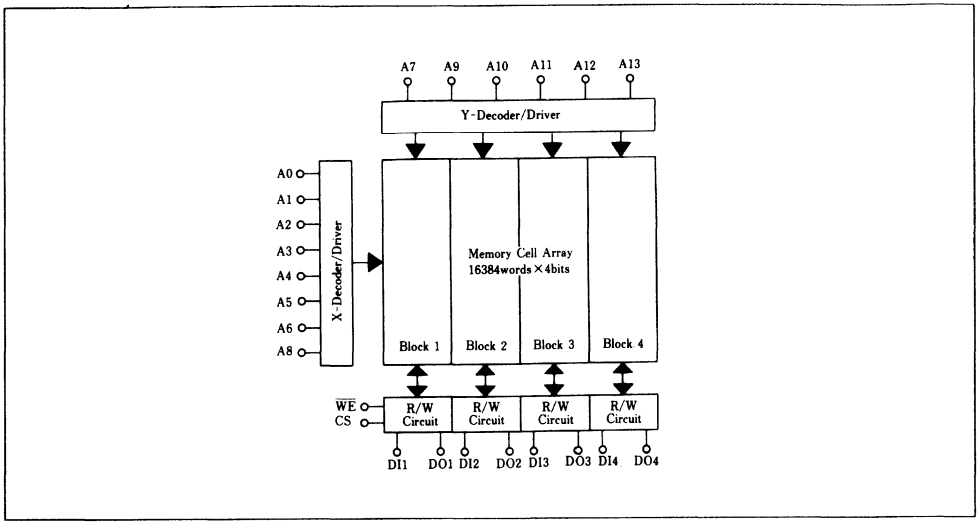
Function Table

Input				
$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	×	×	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes: ×: Irrelevant *: Read out noninvert

Note: The specifications of this device are subject to change wothout notice. Pease contact your nearest Hitachi's Sales Dept. regarging specificaitons.

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Notes: *1 Under bias (V_{EE} = –6 Vmin)
*2 Ceramic flat; Tc, Cerdip; Ta

Electrical Characteristics

DC Characteristics (V_{EE} = –5.2 V, R_L = 50Ω to –2.0 V, Ta*2 = 0 to +85°C (air flow exceeding 2 m/sec), Tc*2 = 0 to +85°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage High/Low for all inputs
	V_{IL}	–1810	—	–1475	mV	
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	$\overline{CS}$ Vin = V_{ILB}
		–50	—	—	µA	Others
Supply current	I_{EE}	–180	—	—	mA	All inputs and outputs open

AC Characteristics (V_{EE} = –5.2 V ± 5%, Ta*2 = 0 to +85°C (air flow exceeding 2 m/sec), Tc*2 = 0 to +85°C)

Read Mode

		HM101494-10			HM101494-12				
Item	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test conditions
Chip select access time	t_{ACS}	—	—	6	—	—	8	ns	
Chip select recovery time	t_{RCS}	—	—	6	—	—	8	ns	
Address access time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM101494-10 Min	Typ	Max	HM101494-12 Min	Typ	Max	Unit	Test conditions
Write pulse width	t_W	6	—	—	8	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data setup time	t_{WSD}	2	—	—	2	—	—	ns	
Data hold time	t_{WHD}	2	—	—	2	—	—	ns	
Address setup time	t_{WSA}	2	—	—	2	—	—	ns	$t_W = t_W$ min
Address hold time	t_{WHA}	2	—	—	2	—	—	ns	
Chip select setup time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip select hold time	t_{WHCS}	2	—	—	2	—	—	ns	
Write disable time	t_{WS}	—	—	6	—	—	8	ns	
Write recovery time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

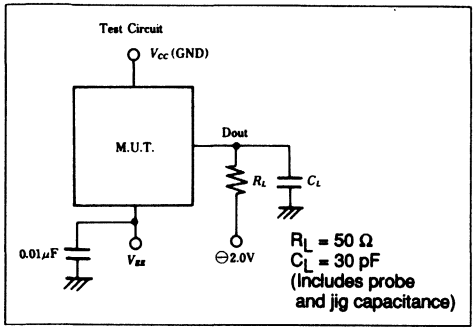
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Capacitance

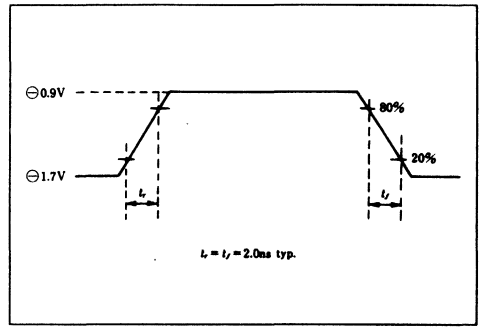
Item	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin	—	5	—	pF	$\overline{WE}$, $\overline{CS}$, D_{I1}, D_{I2}
		—	3	—	pF	Others
Output capacitance	Cout	—	3	—	pF	

Test Circuit and Waveforms

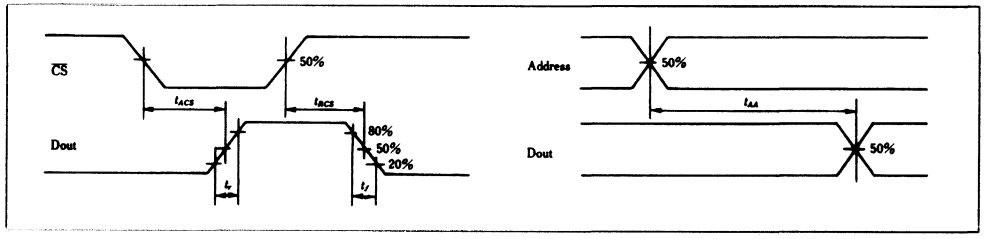
Loading Condition



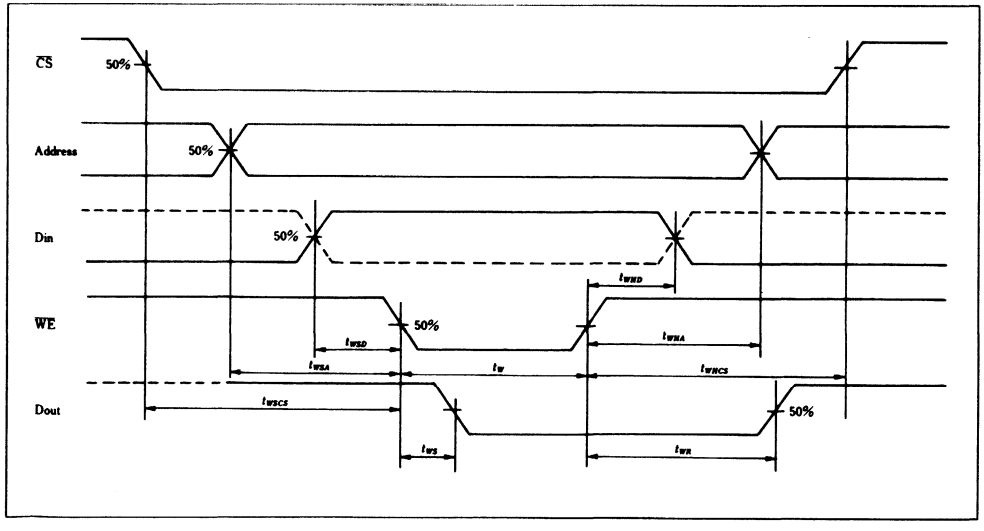
Input Pulse



Read Mode



Write Mode



HM100500-18 Series

262144-Word × 1-Bit Fully Decoded Random Access Memory

The HM100500-18 is ECL 100K compatible, 262144-word × 1-bit read/write random access memory developed for high speed systems such as main memories for super computers.

Features

- 262144-word × 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 18 ns (max)
- Write pulse width: 10 ns (min)
- Low power dissipation: 500 mV (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

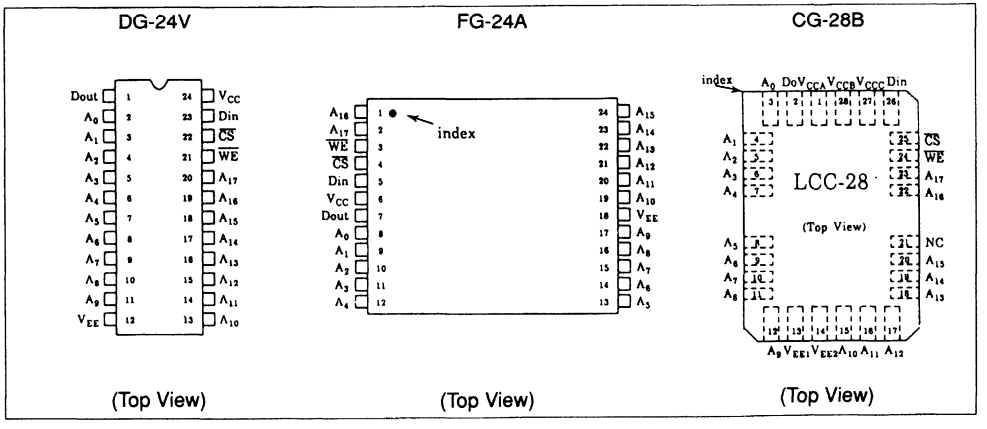
Type No.	Access time	Package
HM100500CG-18	18 ns	28-pin LCC (CG-28B)
HM100500-18	18 ns	24-pin DIP (DG-24V)
HM100500F-18	18 ns	24-pin FPG (FG-24A)

Function Table

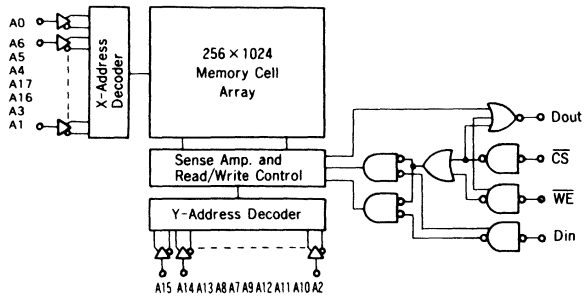
Input				
$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	×	×	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read out noninvert

Pin Arrangement



Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*1	–55 to +125	°C

Note: *1; Under bias (V_{EE} = –6 V min)

Electrical Characteristics

DC Characteristics (V_{EE} = –4.5V, R_L = 50 Ω to –2.0 V, Tc* = 0 to +85°C, Ta* = 0 to +85°C air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage high/low for all inputs
	V_{IL}	–1810	—	–1475	mV	

DC Characteristics (V_{EE} = –4.5V, R_L = 50 Ω to –2.0 V, Tc* = 0 to +85°C, Ta* = 0 to +85°C air flow exceeding 2 m/sec) (cont)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions	
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—			Others
Supply current	I_{EE}	–160	—	—	mA	All inputs and outputs open	

*Tc: Ceramic Flat, L_{CC}, Ta: Cerdip

AC Characteristics (V_{EE} = –4.5V ± 5%, Tc* = 0 to +85°C, Ta* = 0 to +85°C air flow exceeing 2 m/sec)

Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Chip select access time	t_{ACS}	—	—	18**	ns	
				15***	ns	
Chip select recovery time	t_{RCS}	—	—	18**	ns	
				10***	ns	
Address access time	t_{AA}	—	—	18	ns	

Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Write pulse width	t_W	10	—	—	ns	t_{WSA} = 2 ns
Data setup time	t_{WSD}	2	—	—	ns	
Data hold time	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	2	—	—	ns	t_W = 10 ns
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	2	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	15**	ns	
				10***	ns	
Write recovery time	t_{WR}	—	—	21	ns	

*: Tc; Ceramic Flat, L_{CC}, Ta; Cerdip **: HM100500CG ***: HM100500/F

Rise/Fall Time

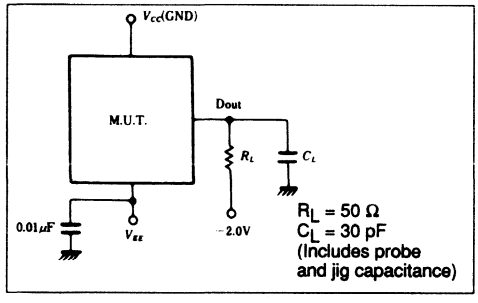
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Capacitance

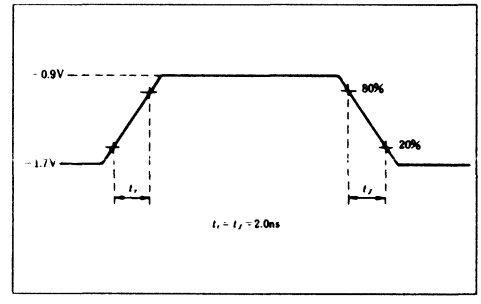
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

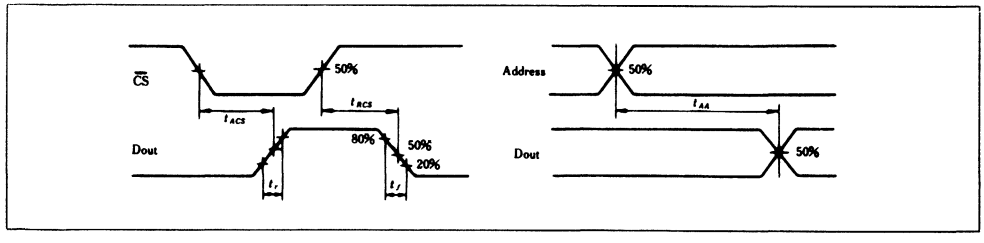
Loading Condition



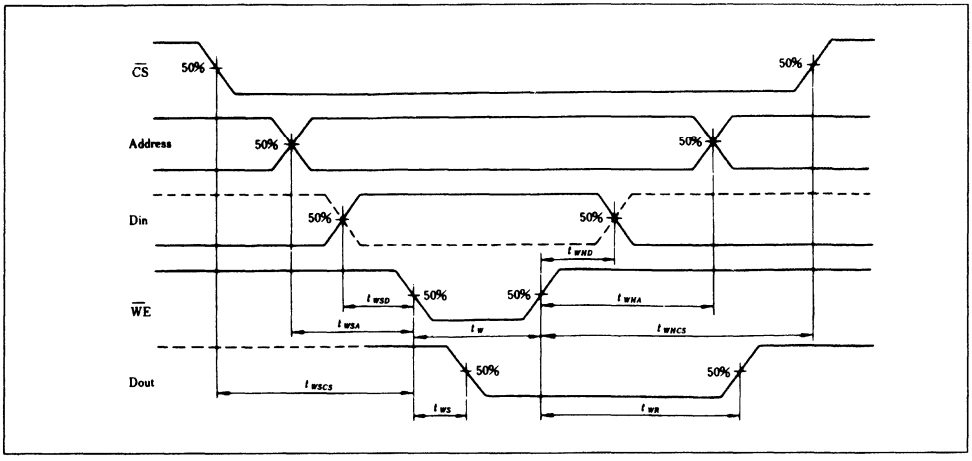
Input Pulse



Read Mode



Write Mode


$\overline{CS}$
Address
Din
$\overline{WE}$
Dout
50%
t_{WND}
t_{WSD}
t_{WHA}
t_{WSA}
t_W
t_{WHCS}
t_{WSCS}
t_{WS}
t_{WR}

HM101500-15 Series

262144-Word × 1-Bit Fully Decoded Random Access Memory

The HM101500-15 is ECL 100K compatible, 262144-word × 1-bits read/write random access memory developed for high speed systems such as main memories for super computers.

Features

- 262144-word × 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 15 ns (max)
- Write pulse width: 10 ns (min)
- Low power dissipation: 500 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type no.	Access time	Package
HM101500F-15	15 ns	24-pin FPG (FG-24A)

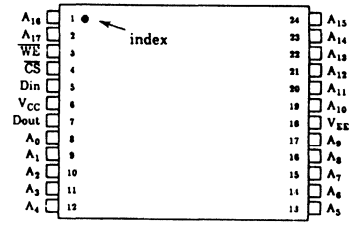
Truth Table

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes: ×; Irrelevant *; Read out noninvert

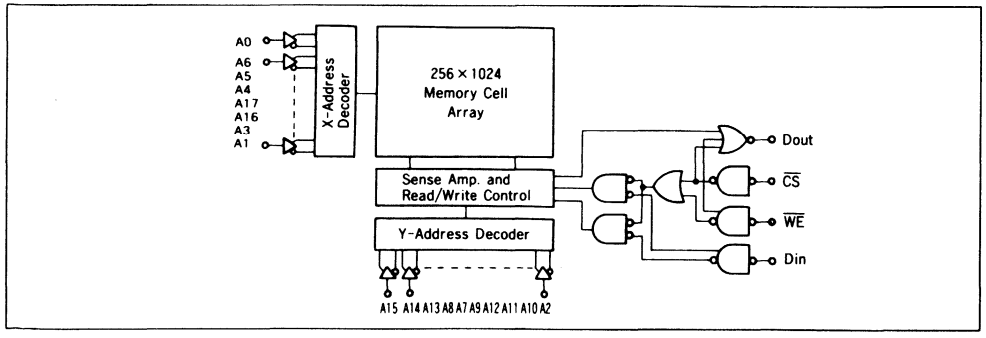
Pin Arrangement

HM101500F-15



(Top View)

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to +150	°C
Storage temperature	Tstg (Bias)*	–55 to +125	°C

Note: *; Under bias (V_{EE} = –6 V min)

Electrical Characteristics

DC Characteristics (V_{EE} = –5.2 V, R_L = 50 Ω to –2.0 V, Tc = 0 to +85°C)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test conditions	
Output voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}	
	V_{OL}	–1810	–1715	–1620	mV		
Output threshold voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}	
	V_{OLC}	—	—	–1610	mV		
Input voltage	V_{IH}	–1165	—	–880	mV	Guaranteed input voltage high/low for all inputs	
	V_{IL}	–1810	—	–1475	mV		
Input current	I_{IH}	—	—	220	µA	Vin = V_{IHA}	
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB}	$\overline{CS}$
		–50	—	—			Others
Supply current	I_{EE}	–200	—	—	mA	All inputs and outputs open	

AC Characteristics (VEE = –5.2 V ± 5%, Tc = 0 to +85°C)

Read Mode

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Chip select access time	t_{ACS}	—	—	15	ns	
Chip select recovery time	t_{RCS}	—	—	10	ns	
Address access time	t_{AA}	—	—	15	ns	

Write Mode

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Write pulse width	t_W	10	—	—	ns	t_{WSA} = 2 ns
Data setup time	t_{WSD}	2	—	—	ns	
Data hold time	t_{WHD}	3	—	—	ns	
Address setup time	t_{WSA}	2	—	—	ns	t_W = 10 ns
Address hold time	t_{WHA}	3	—	—	ns	
Chip select setup time	t_{WSCS}	2	—	—	ns	
Chip select hold time	t_{WHCS}	3	—	—	ns	
Write disable time	t_{WS}	—	—	10	ns	
Write recovery time	t_{WR}	—	—	18	ns	

Rise/Fall Time

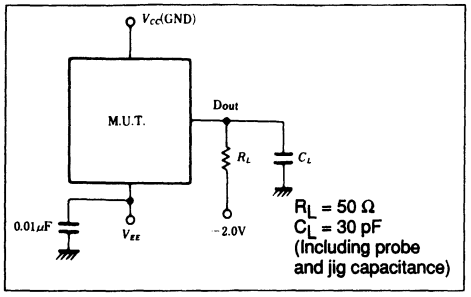
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output rise time	t_r	—	2	—	ns	
Output fall time	t_f	—	2	—	ns	

Capacitance

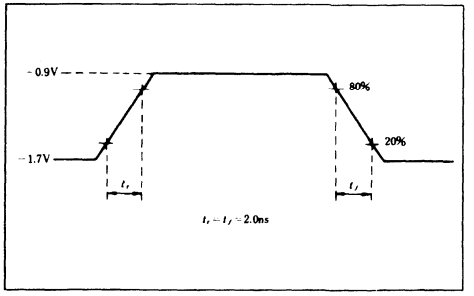
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	3	—	pF	
Output capacitance	Cout	—	5	—	pF	

Test Circuit and Waveform

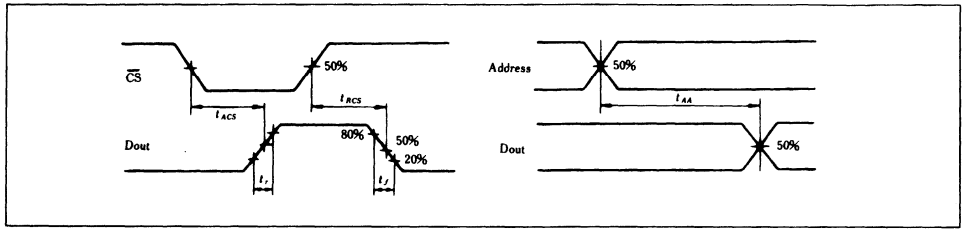
Loading Condition



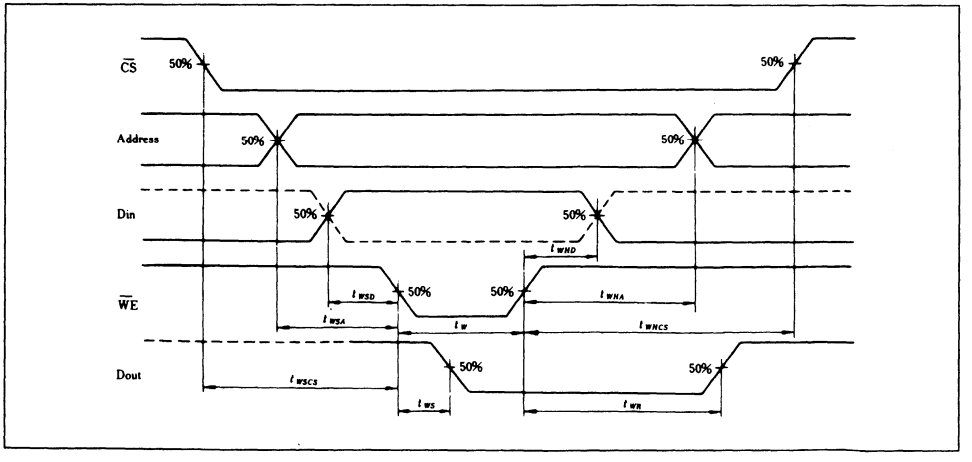
Input Pulse



Read Mode



Write Mode



HM100504 Series

65536-Word × 4-Bit Fully Decoded Random Access Memory

The HM100504 is ECL 100K compatible, 65536-word by 4-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

Features

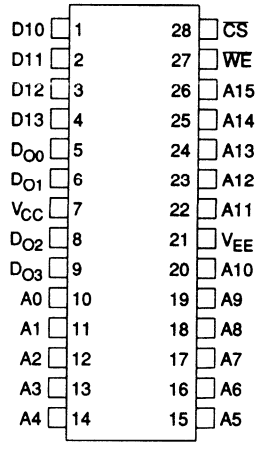
- 65536-word × 4-bit organization
- Fully compatible with 100K ECL level
- 0.8 µm Hi-BiCMOS process
- Address access time: 10/12 ns (max)
- Write pulse width: 8 ns (min)
- Low power dissipation: 500 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type no.	Access time	Package
HM100504F-10	10 ns	28-pin FPG (FG-28)
HM100504F-12	12 ns	

Pin Arrangement

HM100504F-10/12



(Top View)

Pin Description

Pin name	Function
A0 – A15	Address input
$D_{I0} - D_{I3}$	Data input
$D_{O0} - D_{O3}$	Data Output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Ground
V_{EE}	Supply voltage

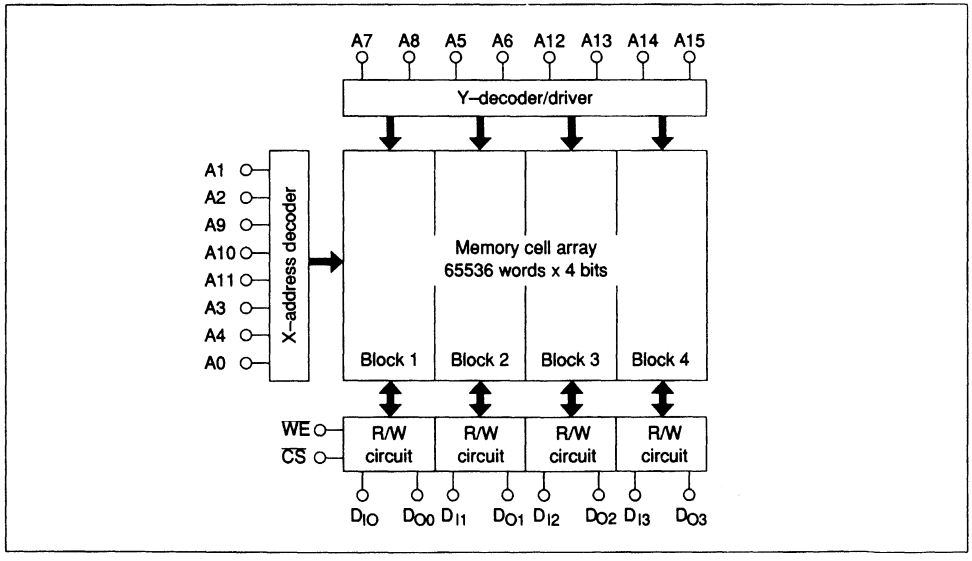
Truth Table

Input

$\overline{CS}$	$\overline{WE}$	Din	Output	Mode
H	×	×	L	Not selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes: ×; Irrelevant *; Read out noninvert

Block Diagram



Absolute Maximum Rating (Ta = 25°C)

Item	Sumbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Storage temperature	Tstg	–65 to + 150	°C
Storage temperature	Tstg (Bias)*1	–55 to + 125	°C

Note: *1 Under bias (V_{EE} = –6 V min)

HM100506LLJP

65536-Word × 4-Bit Self-Timed Random Access Memory

The HM100506LL is ECL 100K compatible, 65536-word by 4-bit synchronous Self-Timed random access memory developed for high speed systems such as cache and control/buffer storage.
This device has Input/Output latches which store address, data-in, write enable, chip select, and data out. All signals are controlled by the external clock.
The write pulse generates internally, and write operations are initiated by the rising edge of the clock.

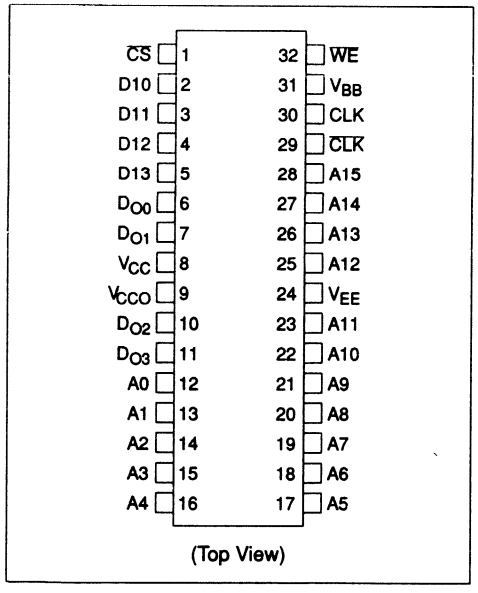
Features

- 65536-word × 4-bit organization
- Fully compatible with 100K ECL level
- 0.8 µm Hi-BiCMOS process
- Access time from address: 11 ns (max)
- Cycle time: 12 ns (min)
- Low power dissipation: 700 mW (typ)
- Inputs/Outputs latched on chip
- Internal write pulse generator
- Output obtainable by wired-OR (open emitter)

Ordering Information

Type No.	Access time	Package
HM100506LLJP11	11 ns	400-mil 32-pin plastic SOJ (CP-32D)

Pin Arrangement

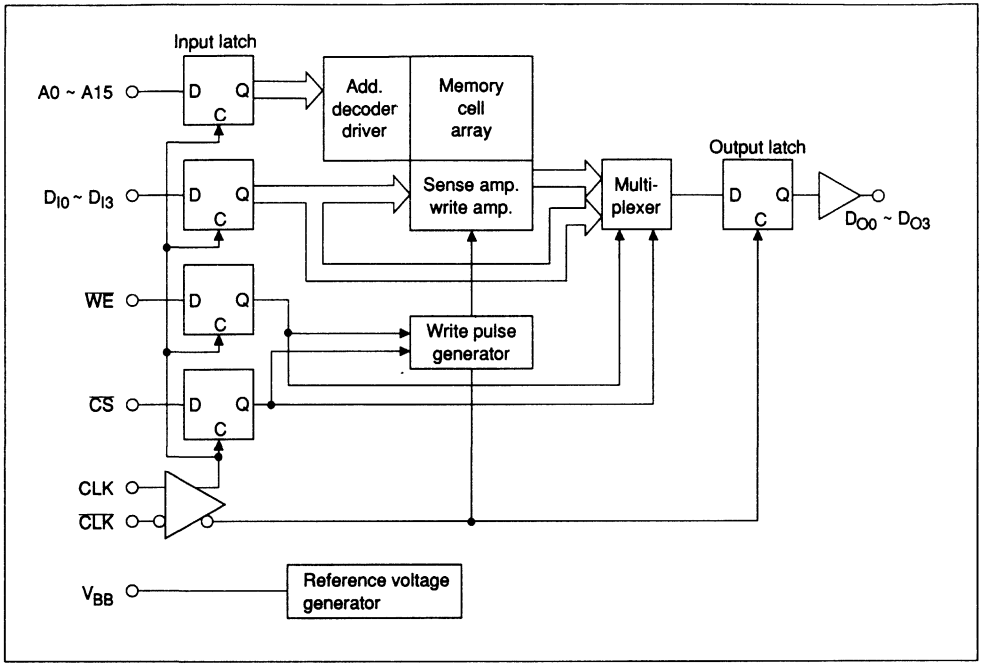


(Top View)

Pin Description

Pin name	Function
A0 – A15	Address input
$D_{I0} - D_{I3}$	Data input
$D_{O0} - D_{O3}$	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
CLK/$\overline{CLK}$	Clock input
V_{BB}	Referance voltage
V_{CC}/V_{CCO}	Ground
V_{EE}	Supply voltage

Block Diagram



Function Table

Input

$\overline{CS}$	$\overline{WE}$	Din	CLK/$\overline{CLK}$ *3	Output	Mode
H	× *1	× *1		L	Not selected
L	L	L		L	Write "0"
L	L	H		H	Write "1"
L	H	× *1		Dout *2	Read

Notes: *1 Irrelevant
*2 Read out noninvert
*3 Data out becomes valid after the rising (falling) edge of CLK ($\overline{CLK}$)

Absolute Maximum Rating (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{EE} to V_{CC}	+0.5 to –7.0	V
Input voltage	Vin	+0.5 to V_{EE}	V
Output current	Iout	–30	mA
Power dissipation	P_T	1.2	W
Operating temperature	Topr *2	0 to +85	°C
Storage temperature	Tstg	–55 to + 125	°C
Storage temperature	Tstg (Bias) *1, *2	–10 to + 85	°C

Notes: *1 Under bias (V_{EE} = –6 V min)
*2 Case temperature